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A Solar Power Generation System with a Seven-Level Inverter

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Abstract—
This paper proposes another sunlight based force era framework, which is made out of a dc/dc power converter and another seven-level inverter. The dc/dc power converter coordinates a dc–dc support converter and a transformer to change over the yield voltage of the sun powered cell cluster into two autonomous voltage sources with various relationships. This new seven-level inverter is arranged utilizing a capacitor determination circuit and a full-connect power converter, associated in course. The capacitor choice circuit changes over the two yield voltage wellsprings of dc–dc force converter into a three-level dc voltage, and the full-connect power converter further changes over this three-level dc voltage into a seven-level air conditioning voltage. Along these lines, the proposed sun oriented force era framework produces a sinusoidal yield current that is in stage with the utility voltage and is nourished into the utility. The remarkable elements of the proposed seven-level inverter are that just six force electronic switches are utilized, and stand out force electronic switch is exchanged at high recurrence whenever. A model is produced and tried to check the execution of this proposed sun oriented force era framework.

Keywords— Grid-connected; multilevel inverter; pulse-width modulated (PWM) inverter.

1. INTRODUCTION

The broad utilization of fossil energizes has brought about the worldwide issue of nursery emanations. Besides, as the supplies of fossil powers are drained later on, they will turn out to be progressively costly. Along these lines, sun based vitality is turning out to be more essential since it delivers less contamination and the expense of fossil fuel vitality is rising, while the expense of sunlight based exhibits is diminishing. Specifically, little limit circulated power era frameworks utilizing sunlight based vitality might be broadly utilized as a part of private applications soon. The force change interface is imperative to network joined sun based force era frameworks since it changes over the dc power created by a sunlight based cell cluster into air conditioning power and encourages this air conditioner force into the utility lattice. An inverter is essential in the force change interface to change over the dc energy to air conditioning power. Subsequent to the yield voltage of a sun oriented cell cluster is low, a dc–dc power converter is utilized as a part of a little limit sun oriented force era framework to support the yield voltage, so it can coordinate the dc transport voltage of the inverter. The force transformation productivity of the force change interface is essential to guarantee that there is no misuse of the vitality created by the sun oriented cell cluster. The dynamic gadgets and latent gadgets in the inverter deliver a force misfortune. The force misfortunes because of dynamic gadgets incorporate both conduction misfortunes and exchanging misfortunes. Conduction misfortune results from the utilization of dynamic gadgets, while the exchanging misfortune is corresponding to the voltage and the present changes for every exchanging and exchanging recurrence. A channel inductor is utilized to prepare the exchanging sounds of an inverter, so the force misfortune is relative to the measure of exchanging music.

1.1 MULTILEVEL INVERTER:

The voltage change in every exchanging operation for a multilevel inverter is diminished with a specific end goal to enhance its energy transformation effectiveness and the exchanging anxiety of the dynamic gadgets. The measure of exchanging music is additionally constricted, so the force misfortune brought on by the channel inductor is likewise decreased. Accordingly, multilevel inverter innovation has been the subject of much research in the course of recent years. In principle, multilevel inverters ought to be planned with higher voltage levels keeping in mind the end goal to

enhance the change productivity and to lessen symphonious substance and electromagnetic impedance (EMI). Traditional multilevel inverter topologies incorporate the diode cinched, the flying-capacitor, and the course H-span sorts. Diode-braced and flying capacitor multilevel inverters use capacitors to build up a few voltage levels. Be that as it may, it is hard to control the voltage of these capacitors. Since it is hard to make a lopsided voltage innovation in both the diode-braced and the flying capacitor topologies, the force circuit is confounded by the expansion in the voltage levels that is vital for a multilevel inverter.

1.2 SEVEN LEVEL INVERTER:

For a solitary stage seven-level inverter, 12 power electronic switches are required in both the diode-clipped and the flying-capacitor topologies. Awry voltage innovation is utilized as a part of the course H-span multilevel inverter to permit more levels of yield voltage, so the course H-span multilevel inverter is suitable for applications with expanded voltage levels. Two H-span inverters with a dc transport voltage of numerous connections can be associated in course to create a solitary stage seven-level inverter and eight force electronic switches are utilized. All the more as of late, different novel topologies for seven level inverters have been proposed. For instance, a solitary stage seven-level framework joined inverter has been created for a photovoltaic framework. This seven-level lattice associated inverter contains six force electronic switches.

Nonetheless, three dc capacitors are utilized to develop the three voltage levels, which brings about that adjusting the voltages of the capacitors is more unpredictable. a seven-level inverter topology, arranged by a level era part and an extremity era part, is proposed. There, just power electronic switches of the level era part switch in high recurrence, however ten force electronic switches and three dc capacitors are utilized. a particular multilevel inverter with another tweak system is connected to the photovoltaic framework joined generator. The particular multilevel inverter is like the course H-span sort. For this, another adjustment technique is proposed to accomplish dynamic capacitor voltage equalization. a multilevel dc-join inverter is displayed to conquer the issue of incomplete shading of individual photovoltaic sources that are associated in arrangement. The dc transport of a full-connect inverter is designed by a few individual dc squares, where every dc piece is made out of a sun based cell, a force electronic switch, and a diode. Controlling the force hardware of the dc pieces will bring about a multilevel dc-join voltage to supply a full-connect inverter and to at the same time defeat the issues of halfway shading of individual photovoltaic sources.

LITERATURE SURVEY

2.1. N. A. Rahim, K. Chaniago, and J. Selvaraj created an"Single stage seven-level framework associated inverter for photovoltaic framework". The proposed sun oriented force era framework is made out of a dc–dc power converter and a seven-level inverter. The seven-level inverter contains just six force electronic switches, which rearranges the circuit setup. Moreover, stand out force electronic switch is exchanged at high recurrence whenever to create the seven-level yield voltage. This decreases the exchanging power misfortune and enhances the influence efficiency(2011).

2.2. J.- M. Shen, H. L. Jou, and J. C. Wu created "Novel transformer-less network associated power converter with negative establishing for photovoltaic era framework." In this framework, the proposed power converter are just two force electronic switches of the force converter are worked at high exchanging recurrence all the while (one is a dc–dc power converter and the other is a dc–ac inverter).(2012).

2.3. Jinn-Chang Wu and Chia-Wei Chou have proposed "Sunlight based force era framework with seven level inverter". In this proposed framework, a seven-level inverter with just six force electronic switches and stand out force electronic switch is exchanged at high recurrence which is suitable for sunlight based force era framework. The proposed inverter structure creates a sinusoidal yield current

that is in stage with the utility voltage and is encouraged into the utility. This strategy utilizes three reference flag and single triangular transporter sign to produce PWM signals for the switches. ACHB enhances the proficiency. It work at the major recurrence, decreasing the exchanging misfortunes. In addition, the THD is exceedingly decreased, along these lines yield channels can be disposed of .(2014)

3. WORKING PRINCIPLE

3.1. Control Block:

The proposed sun oriented force era framework comprises of a dc– dc power converter and a seven-level inverter. The seven-level inverter changes over the dc power into amazing air conditioning power and bolsters it into the utility and manages the voltages of capacitors C1 and C2. The dc–dc power converter supplies two free voltage sources with numerous connections and performs most extreme force point following (MPPT) so as to concentrate the greatest yield power from sun based cell array.

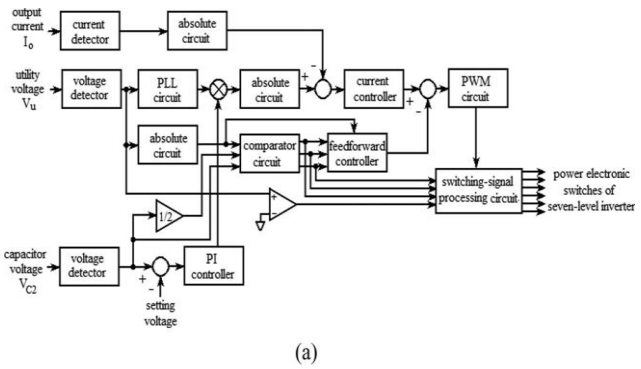

Figure 3.1(a) : Control block of seven-level inverter

Fig. 3.1(a) demonstrates the control square chart for the seven-level inverter. The control object of the seven-level inverter is its yield current, which ought to be sinusoidal and in stage with the utility voltage. The utility voltage is identified by a voltage finder, and after that sent to a stage lock circle (PLL) circuit so as to create a sinusoidal sign with solidarity abundancy. The voltage of capacitor C2 is identified and after that contrasted and a setting voltage. The contrasted result is sent with a PI controller. At that point, the yields of the PLL circuit and the PI controller are sent to a multiplier to create the reference signal, while the yield current of the seven-level inverter is recognized by a present locator. The reference signal and the distinguished yield current are sent to total circuits and afterward sent to a subtractor, and the yield of the subtractor is sent to a present controller. The distinguished utility voltage is likewise sent to an outright circuit and after that sent to a comparator circuit, where indisputably the utility voltage is contrasted and both half and entire of the identified voltage of capacitor C2 , keeping in mind the end goal to decide the scope of the working voltage. The comparator circuit has three yield signals, which relate to the operation voltage ranges, (0, Vdc/3), (Vdc/3, 2Vdc/3), and (2Vdc/3, Vdc). The food forward control takes out the unsettling influences of the utility voltage, Vdc/3 and 2Vdc/3. The supreme estimation of the utility voltage and the yields of the contrasted circuit are sent with a food forward controller to create the food forward sign.

At that point, the yield of the present controller and the food forward sign are summed and sent to a PWM circuit to create the PWM signal. The distinguished utility voltage is additionally contrasted and zero, keeping in mind the end goal to get a square flag that is synchronized with the utility voltage. At long last, the PWM signal, the square flag, and the yields of the contrasted circuit are sent with the exchanging signal handling circuit to create the control signals for the force electronic switches of the seven-level inverter. The present controller controls the yield current of the seven level inverter, which is a sinusoidal sign of 60 Hz. Subsequent to the food forward control is utilized as a part of the control circuit, the present controller can be a straightforward enhancer, which gives great following execution. the addition of the present controller decides the transmission capacity and the relentless state mistake. The increase of the present controller must be as expansive as could be allowed with a specific end goal to guarantee a quick reaction and a low unfaltering state blunder. In any case, the increase of the present controller is constrained in light of the fact that the data transfer capacity of the force converter is restricted by the exchanging recurrence.

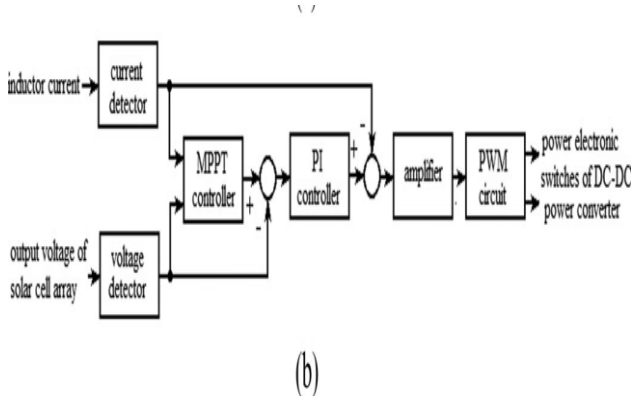

Fig. 3.1(b) : Control block of dc–dc power converter.

Fig.3.1(b) demonstrates the control piece outline for the dc–dc power converter. The data for the DC-DC power converter is the yield of the sunlight based cell exhibit. A swell voltage with a recurrence that is twofold that of the utility shows up in the voltages of C1 and C2 , when the seven-level inverter encourages genuine force into the utility. The MPPT capacity is debased if the yield voltage of sun based cell cluster contains a swell voltage. Along these lines, the swell voltages in C1 and C2 must be obstructed by the dc–dc power converter to give enhanced MPPT. Appropriately, double control circles, an external voltage control circle and an inward current control circle, are utilized to control the dc–dc power converter. Subsequent to the yield voltages of the DC-DC power converter involves the voltages of C1 and C2 , which are controlled by the seven-level inverter, the external voltage control circle is utilized to direct the yield voltage of the sunlight based cell cluster. The inward current control circle controls the inductor current with the goal that it approaches a steady present and hinders the swell voltages in C1 and C2 . The annoyance and perception strategy is utilized to give MPPT . The yield voltage of the sunlight based cell exhibit and the inductor current are identified and sent to a MPPT controller to decide the sought yield voltage for the sun oriented cell cluster. At that point the identified yield voltage and the craved yield voltage of the sun oriented cell cluster are sent to a subtractor and the distinction is sent to a PI controller. The yield of the PI controller is the reference sign of the internal current control circle. The reference signal and the distinguished inductor current are sent to a subtractor and the distinction is sent to a speaker to finish the internal current control circle. The yield of the enhancer is sent to the PWM circuit. The PWM circuit creates an arrangement of corresponding signs that control the force electronic switches of the dc–dc power converter.

3.2. SEVEN LEVEL INVERTER:

Fig.3.2(a)shows the setup of the proposed sun oriented force era framework. The proposed sun oriented force era framework is made out of a sun oriented cell cluster, a dc–dc power converter, and another seven-level inverter. The sun oriented cell cluster is associated with the dc–dc power converter, and the dc–dc power converter is a support converter that joins a transformer with a turn proportion of 2:1. The dc–dc power converter changes over the yield force of the sun based cell cluster into two autonomous voltage sources with different connections, which are supplied to the seven-level inverter. This new seven-level inverter is made out of a capacitor determination circuit and a full-connect power converter, associated in a course. The force electronic switches of capacitor choice circuit decide the release of the two capacitors while the two capacitors are being released independently or in arrangement. On account of the numerous connections between the voltages of the dc capacitors, the capacitor choice circuit yields a three-level dc voltage. The full-connect power converter further changes over this three-level dc voltage to a seven-level air conditioning voltage that is synchronized with the utility voltage. Thusly, the proposed sunlight based force era framework creates a sinusoidal yield current that is in stage with the utility voltage and is nourished into the utility, which delivers a solidarity power variable. As can be seen, this new seven-level inverter contains just six force electronic switches, so the force circuit is simplified.

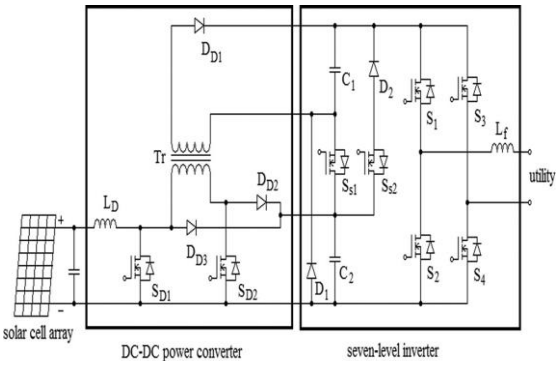

Fig.3.2(a) :- Configuration of the proposed solar power generation system.

The seven-level inverter is made out of a capacitor determination circuit and a full-connect power converter, which are associated in course. The operation of the seven level inverter can be partitioned into the positive half cycle and the negative half cycle of the utility. For simplicity of examination, the force electronic switches and diodes are thought to be perfect, while the voltages of both capacitors C1 and C2 in the capacitor determination circuit are consistent and equivalent to Vdc/3 and 2Vdc/3, individually. Subsequent to the yield current of the sun based force era framework will be controlled to be sinusoidal and in stage with the utility voltage, the yield current of the seven-level inverter is likewise positive in the positive half cycle of the utility. The operation of the seven-level inverter in the positive half cycle of the utility can be further partitioned into four modes.

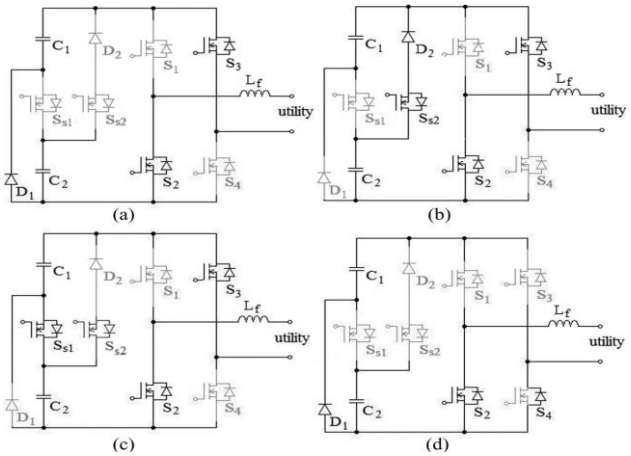

Fig. 3.2.(b) Operation of the seven-level inverter in the positive half cycle,
(a) mode 1, (b) mode 2, (c) mode 3, and (d) mode 4.

Mode 1: Both *SS*1 and *SS*2 of the capacitor selection circuit are OFF, so *C*1 is discharged through *D*1 and the output voltage of the capacitor selection circuit is *V*dc/3. *S*1 and *S*4 of the full-bridge power converter are ON. At this point, the output voltage of the seven-level inverter is directly equal to the output voltage of the capacitor selection circuit, which means the output voltage of the seven-level inverter is *V*dc/3.

Mode 2: In the capacitor selection circuit, *SS*1 is OFF and *SS*2 is ON, so *C*2 is discharged through *SS*2 and *D*2 and the output voltage of the capacitor selection circuit is 2*V*dc/3. *S*1 and *S*4 of the full-bridge power converter are ON. At this point, the output voltage of the seven-level inverter is 2*V*dc/3.

Mode 3: In the capacitor selection circuit, *SS*1 is ON. Since *D*2 has a reverse bias when *SS*1 is ON, the state of *SS*2 cannot affect the current flow. Therefore, *SS*2 may be ON or OFF, to avoiding switching of *SS*2. Both *C*1 and *C*2 are discharged in series and the output voltage of the capacitor selection circuit is *V*dc. *S*1 and *S*4 of the full-bridge power converter are ON. At this point, the output voltage of the seven-level inverter is *V*dc.

Mode 4: Both *SS*1 and *SS*2 of the capacitor selection circuit are OFF. The output voltage of the capacitor selection circuit is *V*dc/3. Only *S*4 of the full-bridge power converter is ON. Since the output current of the seven-level inverter is positive and passes through the filter inductor, it forces the anti parallel diode of *S*2 to be switched ON for continuous conduction of the filter inductor current. At this point, the output voltage of the seven level inverter is zero.

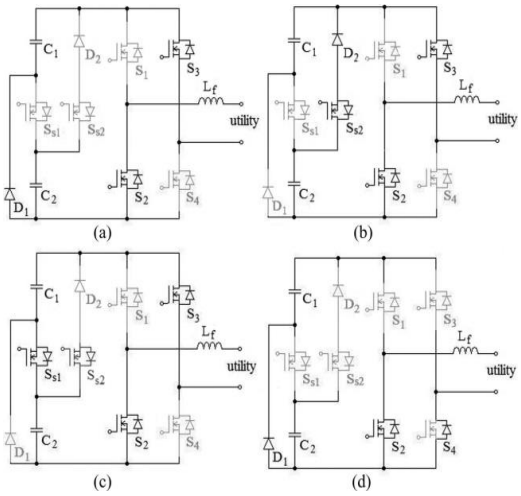

Fig. 3.2.(c)Operation of the seven-level inverter in the negative half cycle: (a) mode 5 (b) mode 6 (c) mode 7 and (d) mode 8.

Consequently, in the positive half cycle, the yield voltage of the seven level inverter has four levels: Vdc, 2Vdc/3, Vdc/3, and 0. In the negative half cycle, the yield current of the seven-level inverter is negative. The operation of the seven-level inverter can likewise be further separated into four modes. A correlation with the operation of the capacitor determination circuit in the negative half cycle is the same as that in the positive half cycle. The distinction is that S2 and S3 of the full-connect power converter are ON amid modes 5, 6, and 7, and S2 is additionally ON amid mode 8 of the negative half cycle. In like manner, the yield voltage of the capacitor choice circuit is upset by the full-connect power converter, so the yield voltage of the seven-level inverter likewise has four levels:−Vdc, −2Vdc/3, −Vdc/3, and 0. In synopsis, the yield voltage of the seven-level inverter has the voltage levels: Vdc, 2Vdc/3, Vdc/3, 0, −Vdc/3, −2Vdc/3,

3.3 DC–DC POWER CONVERTER

Fig.3.3(a), The DC–DC power converter incorporates a boost converter and a current fed forward converter. The boost converter is composed of an inductor *LD* , a power electronic switch *SD*1 , and a diode, *DD*3 . The boost converter charges capacitor *C*2 of the seven-level inverter. The current-fed forward converter is composed of an inductor *LD* , power electronic switches *SD*1 and *SD*2 , a transformer, and diodes *DD*1 and*DD*2 . The current-fed forward converter charges capacitor *C*1 of the seven-level inverter. The inductor *LD* and the power electronic switch *SD*1 of the current-fed forward converter are also used in the boost converter.

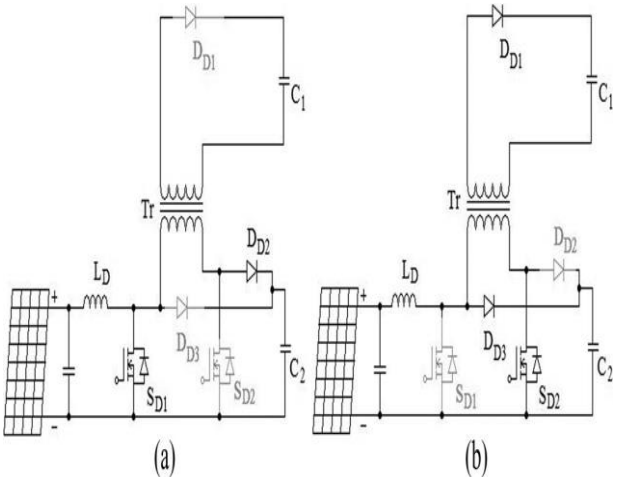

Fig. 3.3. Operation of dc–dc power converter: (a) *SD*1 is on and (b) *SD*1 is off.

Fig. 3.3 (a) shows the operating circuit of the dc–dc power converter when *SD*1 is turned ON. The solar cell array supplies energy to the inductor *LD* . When *SD*1 is turned OFF and *SD*2 is turned ON, its operating circuit is shown in Fig.3.3(b). Accordingly, capacitor *C*1 is connected to capacitor *C*2 in parallel through the transformer, so the energy of inductor *LD* and the solar cell array charge capacitor *C*2 through *DD*3 and charge capacitor *C*1 through the transformer and *DD*1 during the off state of *SD*1 . Since capacitors *C*1 and *C*2 are charged in parallel by using the transformer, the voltage ratio of capacitors *C*1 and *C*2 is the same as the turn ratio (2:1) of the transformer. Therefore, the voltages of *C*1 and *C*2 have multiple relationships. The boost converter is operated in the continuous conduction mode (CCM).

The voltage of *C*2 can be represented as

$Vc2 = [1/(1 - DVs)]$ ..... (1)

where *VS* is the output voltage of solar cell array and *D* is the duty ratio of *SD*1 .

The voltage of capacitor *C*1 can be represented as

$Vc1 = 1/[2(1 - D)Vs]$ ..... (2)

It should be noticed that the current of the charging inductance of the transformer increments when SD2 is in the ON state. Ordinarily, the forward converter needs a third demagnetizing twisting so as to discharge the vitality put away in the polarizing inductance back to the force source. Be that as it may, in the proposed dc–dc power converter, the vitality put away in the charging inductance is conveyed to capacitor C2 through DD2 and SD1 when SD2 is killed. Subsequent to the vitality put away in the charging inductance is exchanged forward to the yield capacitor C2 and not back to the dc source, the force proficiency is moved forward. What's more, the force circuit is streamlined on the grounds that the charging circuits for capacitors C1 and C2 are coordinated. Capacitors C1 and C2 are charged in parallel by utilizing the transformer, so their voltages consequently have various connections. The control circuit is additionally improved.

4. EXPERIMENTAL RESULTS

To verify the performance of the proposed solar power generation system, a prototype was developed with a controller based on the DSP chip TMS320F28035. The power rating of the prototype is 500 W, and the prototype was used for a single-phase utility with 110Vand 60 Hz.
inverter when the output power of solar power generation
system is 500 W.

TABLE I
STATES OF POWER ELECTRONIC SWITCHES FOR A SEVEN-LEVEL INVERTER

	S_{S1}	S_{S2}	S_1	S_2	S_3	S_4
positive half cycle						
$\|v_u\| < V_{dc}/3$	off	off	PWM	off	off	on
$2V_{dc}/3 > \|v_u\| > V_{dc}/3$	off	PWM	on	off	off	on
$\|v_u\| > 2V_{dc}/3$	PWM	on	on	off	off	on
negative half cycle						
$\|v_u\| < V_{dc}/3$	off	off	off	on	PWM	off
$2V_{dc}/3 > \|v_u\| > V_{dc}/3$	off	PWM	off	on	on	off
$\|v_u\| > 2V_{dc}/3$	PWM	on	off	on	on	off

Thus, a feedforward control ought to be utilized to dispose of the unsettling influence, and the addition Gf ought to be 1/kpwm. In the negative half cycle, the seven-level inverter is exchanged between modes 5 and 8, to yield a voltage of – Vdc/3 or 0, when the outright estimation of the utility voltage is littler than Vdc/3. In like manner, S3 is exchanged in PWM. The seven level inverter is exchanged in modes 6 and 5 to yield a voltage of −2Vdc/3 or −Vdc/3 when the utility voltage is in the extent (−Vdc/3, −2Vdc/3).Within this voltage range, SS2 is exchanged in PWM. The seven-level inverter is exchanged in modes 7 and 6 to yield a voltage of −Vdc or −2Vdc/3, when the utility voltage is in the reach (−2Vdc/3, −Vdc). At this voltage range, SS1 is exchanged in PWM and SS2 stays in the ON state to abstain from exchanging of SS2 . The rearranged model for the seven-level inverter in the negative half cycle is the like that for the positive half cycle.

Subsequent to just six force electronic switches are utilized as a part of the proposed seven-level inverter, the force circuit is fundamentally improved contrasted and a customary seven-level inverter. The conditions of the force electronic switches of the seven-level inverter, as nitty gritty beforehand, are abridged in Table I. It can be seen that one and only power electronic switch is exchanged in PWM inside of every voltage range and the adjustment in the yield voltage of the seven-level inverter for every exchanging operation is Vdc/3, so exchanging power misfortune is lessened. just three semiconductor gadgets are directing in arrangement in modes 1, 3, 4, 5, 7, and 8 and four semiconductor gadgets are leading in arrangement in modes 2 and 6. This is better than the routine multi-level inverter

topologies, in which no less than four semiconductor gadgets are leading in arrangement.

In this way, the conduction loss of the proposed seven-level inverter is additionally lessened marginally. The downside of the proposed seven-level inverter is that the voltage rating of the full-connect converter is higher than that of traditional multilevel inverter topologies. The spillage current is an imperative parameter in a sunlight based force era framework for transformer less operation. The spillage current is reliant on the parasitic capacitance and the negative terminal voltage of the sun oriented cell cluster appreciation toground. To diminish the spillage current, the channel inductor Lf ought to be supplanted by a symmetric topology.

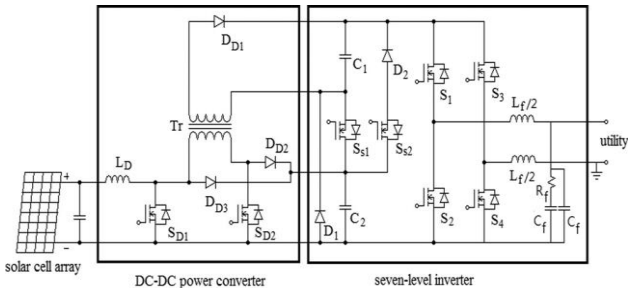

Fig. 4.1. Configuration of the proposed solar power generation system for suppressing the leakage current.

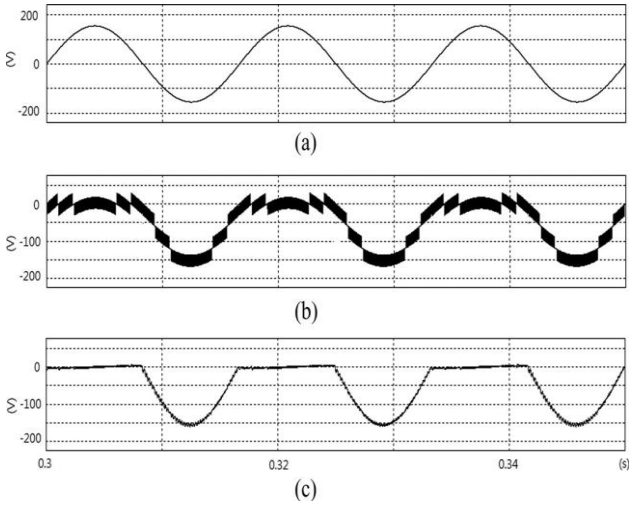

Fig. 4.2 Simulation results of the proposed solar power generation system: (a) utility voltage, (b) negative terminal voltage for adding the symmetric filter inductor,and (c) negative terminal voltage for adding the symmetric filter inductorand the extra filter *Cf –Rf –Cf* .

Solar based force era framework is redrawn as Fig. 4.1 and Fig.4.2 demonstrates the reproduction after effects of the proposed sunlight based force era framework. Fig. 4.2(b) is the negative terminal voltage of the sun powered cell exhibit for the seven-level inverter with the symmetric channel inductor of 0.95 mH. As seen in Fig.4.2(b), this voltage contains a high-recurrence swell. The crest to-crest estimation of the high recurrence swell is around 30 V, which is much littler than that of a full-connect inverter with unipolar exchanging. This high-recurrence swell will bring about a spillage current of sun based cell exhibit. On the off chance that the spillage current of sun based cell exhibit is too high to ever be acknowledged, an additional channel Cf –Rf –Cf , as appeared in Fig. 6, can be included. Subsequent to the exchanging of S4 is synchronized with the utility voltage, the additional channel Cf –Rf –Cf is just included inthe power-electronic leg (S1, S2). Fig. 4.2(c) demonstrates the negative terminal voltage of a sun based cell exhibit for the seven-level inverterwith the symmetric channel inductor and the additional filterCf –Rf –Cf of 1 μF–25 Ω–1 μF. As seen in Fig.4.2(c), the high-recurrence swell is lessened viably, so the spillage current can be further reduced.

TABLE II
PARAMETERS OF THE PROTOTYPE

DC-DC power converter	
input voltage	70V
inductor	1mH
PWM frequency	15360Hz
seven-level inverter	
capacitor C_1, C_2	1000μF
filter inductor	1.9 mH
PWM frequency	15360Hz

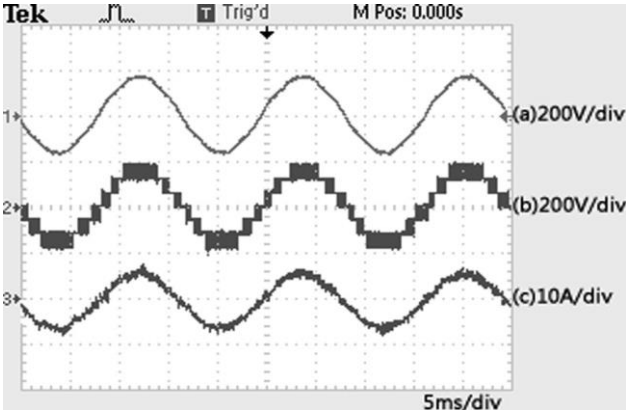

Fig. 4.3 Experimental results for the ac side of the seven-level inverter: (a) utility voltage, (b) output voltage of seven-level inverter, and (c) output current of the seven-level inverter.

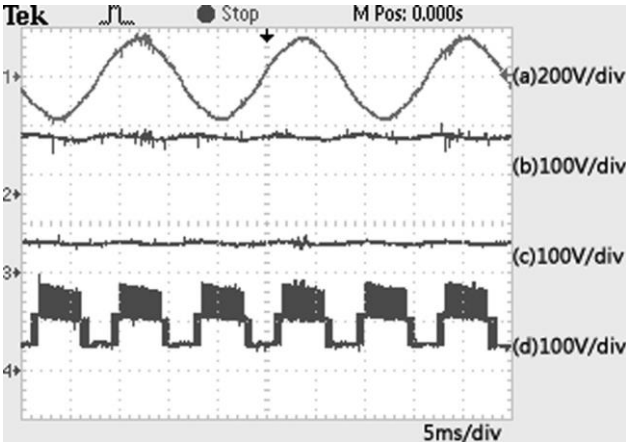

Fig. 4.4 Experimental results for the dc side of the seven-level inverter: (a) utility voltage, (b) voltage of capacitor C2, (c) voltage of capacitor C1, and (d) output voltage of the capacitor selection circuit.

Air conditioning side of the seven-level inverter. Fig. 4.3(b) demonstrates that the yield voltage of the seven-level inverter has seven voltage levels. The yield current of the seven-level inverter, appeared in Fig. 4.3(c), is sinusoidal and in stage with the utility voltage, which implies that the matrix associated power transformation interface nourishes an unadulterated genuine energy to the utility. The aggregate symphonious contortion (THD) of the yield current of the seven-level inverter is 3.6%. Fig. 4.4 demonstrates the exploratory results for the dc side of the seven-level inverter. Fig. 4.4(b) and (c) demonstrate that the voltages of capacitors C2 and C1 of the capacitor choice circuit have different connections and are kept up at 60 and 120 V, separately. Fig. 4.4(d) demonstrates that the yield voltage of the capacitor choice circuit has three voltage levels (60, 120, and 180 V).

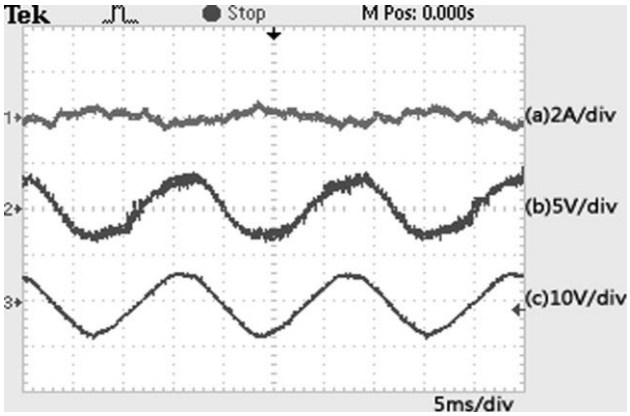

Fig. 4.5. Experimental results of the dc–dc power converter: (a) ripple current of inductor, (b) ripple voltage of capacitor C2, and (c) ripple voltage of capacitor C1.

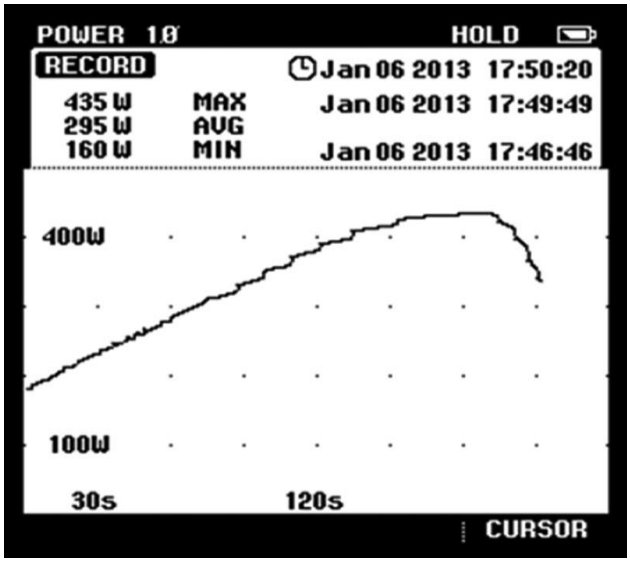

Fig. 4.6. Output power scan of the solar cell array.

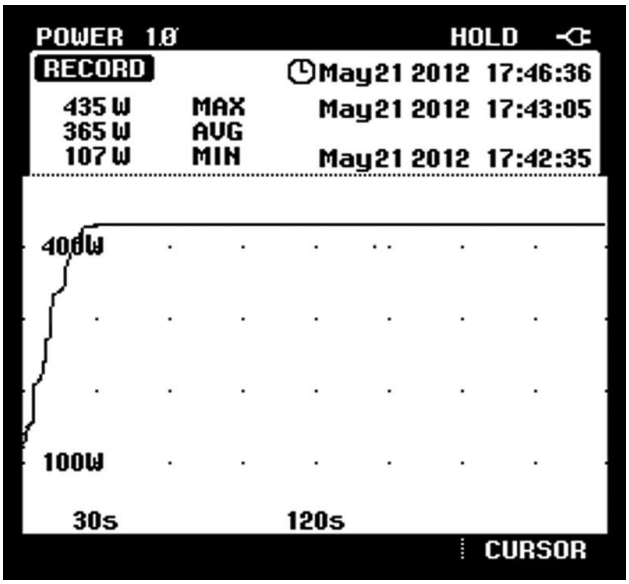

Fig. 4.7. Experimental results for the MPPT performance of the proposed solar power generation system.

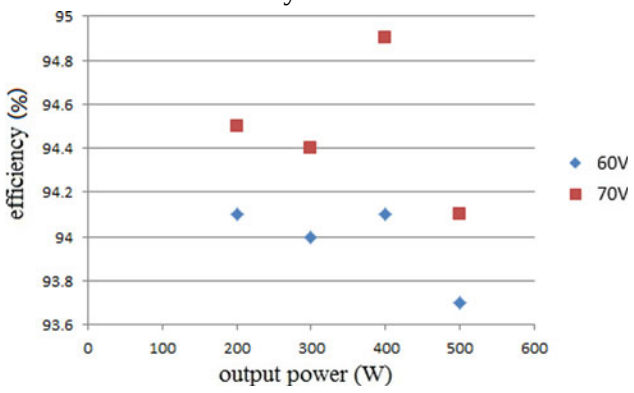

Fig. 4.8. Experimental results for the power efficiency of the proposed solar power generation system.

CONCLUSION:

This seminar proposes a solar power generation system to convert the dc energy generated by a solar cell array into ac energy that is fed into the utility. This reduces the switching power loss and improves the power efficiency. The proposed solar power generation system can effectively trace the maximum power of solar cell array.

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