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On-Chip Permutation Mesh Network for MPSOCs Network-on-Chip

P Vinaya Sri Lakshmi
1 Assoc.Prof, ECE Department, Swami Vivekananda Institute of Technology, Hyderabad.
Email : vinayasrilakshmi@gmail.com

Abstract-

Conversion of 2D NoC into three dimensional 3D NoC has been proposed and the 3D Networks-on-Chip (3D NoCs) have been attracted an interest to solve on-chip communication demands for future multipurpose systems. In this paper, a brief idea of 3D NoCs optimization techniques of modeling and evaluation of alternate Noc topologies, routing algorithms and mapping techniques are presented to achieve optimized area and power.

***Index Terms*— Network on chip; area; power; On chip communication.**

I. INTRODUCTION

Technology scaling has allowed Systems-on-Chip (SoCs) designs to grow continuously in count of components and complexity. This significantly leads to some very challenging problems, such as power dissipation and resource management. Particularly, the interconnection network starts to play an important role in determining the performance and power of the entire chip . These challenges have led conventional bus-based-systems that are not reliable architectures for SoC, due to lack of scalability and parallelism integration, high latency and power consumption, in addition to their low throughput .

Network-on-Chip (NoC) was introduced as a promising paradigm that can respond to these issues based on a simple and scalable architecture. NoC connects the processors, memories and other custom designs using switches that distributes packets on a hop-by-hop basis which increase the bandwidth and performance. At the same time, applications of future are getting more and more complex, demanding a scalable architecture to ensure a sufficient bandwidth between memories and cores, as well as communication between different cores on the same chip.

This made the conventional 2D-NoC not suitable for future large-scale systems. One of the limitations is the higher diameter that 2D-NoC suffers with a large network size. The diameter is an main parameter for NoC systems, since a large network diameter effects a negative impact on the worst case routing latency in the network. By considering all these factors, optimizing NoC-based architecture becomes necessary, and several works have been conducted.

One of the proposed method is to extend the 2D-Network-on-Chip to the third dimension. In the past years, 3D-ICs have been attracted an attention as the potential solution to resolve the interconnect bottleneck. Due to the reduced average interconnect length, 3D-ICs produce higher performance and somewhat lowers interconnect power consumption. 3D ICs also make circuitry more resistant to noise , and enable the realization of mixed technology . Combining the NoC structure
with the 3D architecture attempts a rising 3D-NoC architecture. This merger provides a new solution for NoC designs to satisfy the high requirements of future large scale applications.

II. MULTI STAGE INTERCONNECT NETWORK

In an NoC the Processing elements(PE) are connected to each other . NoC consists of network interfaces(NI), links and routing nodes . NI connects the interconnection environment and the PE domain and decouples the computation from communication channels.

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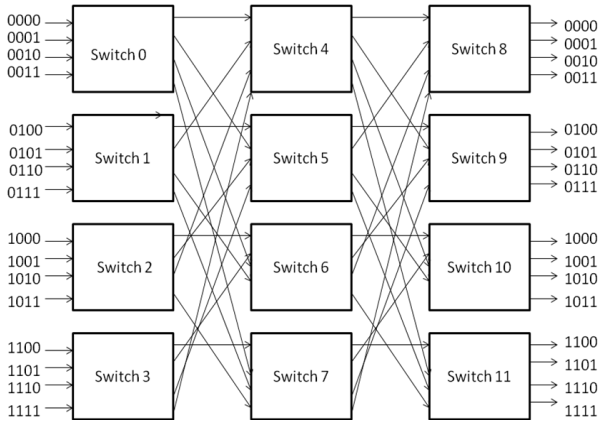

Fig 1:On-chip network topology

Routing nodes, are called routers, that arbitrates the data between the source and destination PEs through the links.

The design of multistage on chip network switching topology with a pipelined circuit of dynamic path, and the dynamic setup path scheme enables runtime path arrangement for arbitrary traffic permutations. The circuit-switching endeavours a promising of permuted data. The proposed design involves configuration and programming of Arbiter in switch circuit.

[1] MESH TOPOLOGY

Mesh network is a family of multistage networks, applied to build scalable multiprocessors with thousands of nodes in macro systems. A three-stage mesh network is defined as $c(m,n,p)$, where n represents the number of inputs for p of first-stage switches and m is the number of second-stage switches. In order to provide a parallelism degree of 16 for practical MPSoCs,a topology is proposed to use $c(4,4,4)$ for the designed network. This network has a readjustable property that can realize all possible alternatives between its input and outputs.

The choice of the three-stage Mesh network with a reserved number of middle-stage switches is to minimize implementation cost, but still it enables a reproperty for the network.

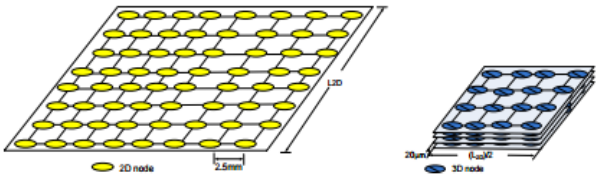

Fig 2: 2D and 3D mesh networks

Signals	Function	
Request (Req.)	00 Idle	01 Back
Answer (Ans.)	01 Ack	11 nAck

Bit format representation in handshake signals in switch

[2] SWITCH NETWORK

Each switch consists of four bidirectional port and the 4 ports are connected to corresponding neighboring switches, and the port which remains is connected to the on-chip IP through a wrapper.

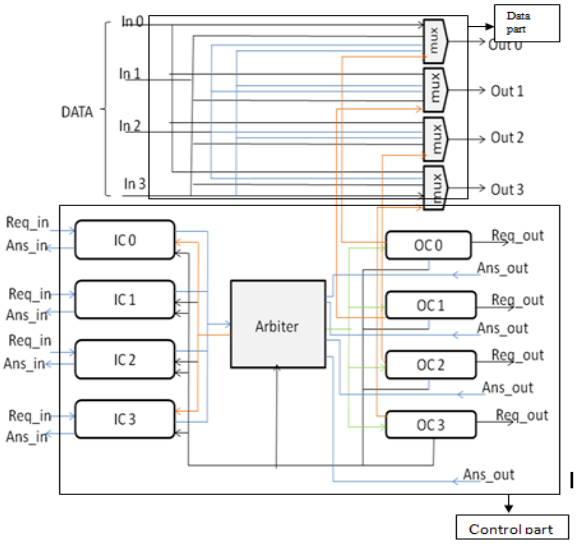

Fig 3: Common switch architecture

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Common switch architecture has following components

- 4- Input Controls (IC's)
- 4-Output controls (OC's)
- 1-Arbiter and
- Encoder and decoder.

The switch architecture consists of components that can be divided into two function groups.

• The data path contains, CROSBAR with internal transceivers to provide a direct-forwarding (wave-pipelining) source-synchronous data.

• The control part consists of IC's, OC's, and ARBITER. Each and every pair of Ctrl In and Ctrl Out performs handshaking activity.

[3] ARBITRATION SCHEMES

The switching schemes consist of arbiter and this arbiter comprises of different schemes. They are

(i) round robin priority scheme.
(ii) weighted/dynamic priority scheme.
(iii) Fixed priority scheme.

A. ROUND ROBIN SCHEME

Round robin scheme is one of the algorithms employed in computing in networks. As the name indicates, the time slices are assigned to each process in equal blocks with circular order, handles all processes same. Round-robin scheduling is simple, easy to implement, and free from starvation. Round-robin method can also be applied to other scheduling problems, like data packet scheduling in computer networks. This algorithm name derived from the round-robin principle from other fields.

B. DYNAMIC PRIORITY SCHEME

In weighted priority, all tasks or devices will get access those who place the request for grant to communicate with other device. By overcoming drawbacks of above two schemes, i.e. the inefficiency of round robin and starvation of fixed priority, this scheme provides better results so that the efficiency is increased.

C. FIXED PRIORITY ARBITRATION SCHEME

Fixed priority scheme is a scheduling system used in real time systems**.** With fixed priority scheduling, the scheduler ensures that at any given time, the processor executes the highest priority task of all the tasks that are currently ready to execute. The pre-emptive scheduler has a clock interrupt task which provides the scheduler with options to switch after the task had given a period to execute the time slice.

The scheduling system has the advantage of making sure that no task hogs the processor for any time more than the time slice. However, this scheduling scheme is vulnerable to process or thread lockout. Since priority is given to higher one, the lower-priority tasks could wait an indefinite amount of time.

[4] INPUT CONTROL (IC)

The IC is the key component to perform the backtracking probing task. These include functions such as the processing history of backtracking and dynamically constructing a table of possible output ports for probing (i.e., route-probing table). As shown in FSM, when a request with the incoming probe header arrives, IC's move into the probing state and correlate the current switch address and the destination address (i.e., performs address decoding) to find possible outputs for probing.

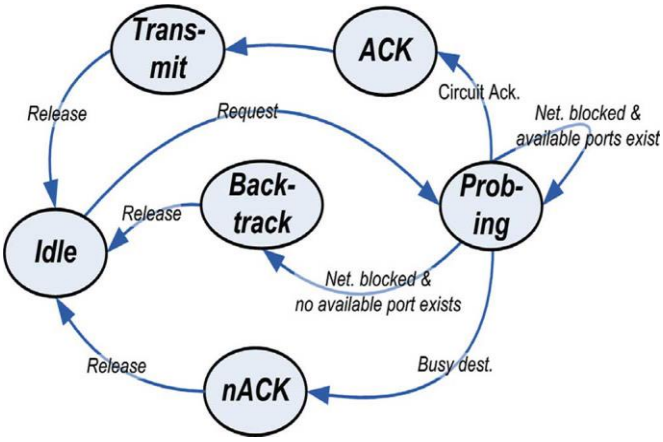

Fig 4: State diagram for FSM implementation

The above figure depicts a simplified FSM diagram for the operation of IC's with the states to guide backtracking probing operation. IC's are triggered by the rising edge of the probing clock when the process arrives the probe header. Meanwhile, the ARBITER is triggered by the falling edge of the clock. The OC is implemented as a retiming stage for the control signals of the ARBITER

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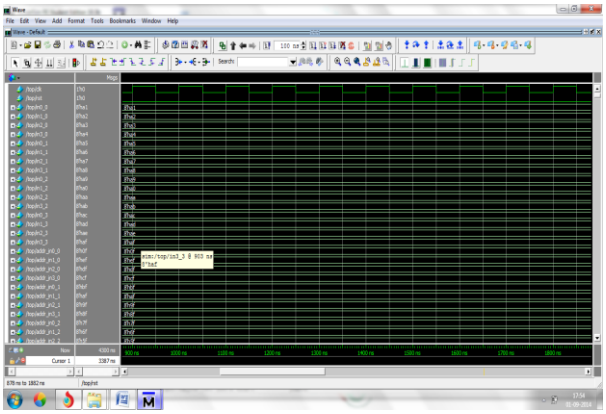
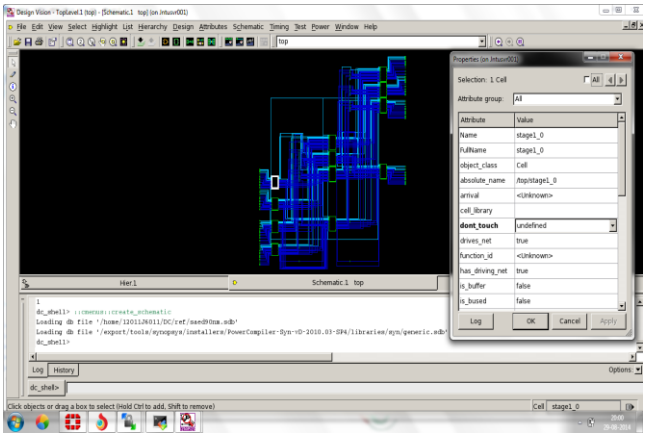
and for the handshake signals (i.e., Req and Ans) with a downstream switch. The implementation of the switch ensures that an arriving probe header always executes in every probe cycle. For example, it is assumed that a probe header arrives at input 4. If there are no desirable and profitable outputs available, the IC's will immediately (after one probing clock cycle) move from the probing state into the backtrack state to force the probe header to backtrack. Then, the probe header backtracks to the upstream switch through its reserved link and releases this link in the next probing clock cycle

III. RESULTS

Simulation Result of OCP



Schematic View of OCP



IV. CONCLUSION

On-chip network which is designed, supports the traffic alternatives in MPSoC applications. By using the circuit-switching approach, combined with dynamic path-setup scheme under a Mesh network topology, the proposed design offers an arbitrary traffic permutation in runtime with compact implementation overhead.

By using Mesh Network Topology we can operate network at a range of 100MHz frequency with a bandwidth of 30Gbps approximately.

By using Circuit Switching technique we can have a dedicated path delay from source Node to Destination Node. Link once established is serviced till all amount transactions is carried out.

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