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# Implementation of Low Power High Speed 32 bit ALU using FPGA

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## ABSTRACT-

*Digital design is an amazing and very broad field. The applications of digital design are present in our daily life, including computers, calculators, video cameras etc. The VHDL (VHSIC Hardware Description Language) has become an essential tool for designers in the world of digital design. This paper presents implementation of a 32-bit Arithmetic Logic Unit (ALU) using VHDL. Here the behavioral VHDL model of ALU is designed to perform 14 operations which includes logical, arithmetic and shift operations. The VHDL implementation and functionality test of the 32-bit ALU is done by using the Modelsim 5.4a tool.*

## 1. INTRODUCTION

The Arithmetic Logic Unit (ALU) is a fundamental building block of the Central Processing Unit (CPU) of a computer. Even one of the simplest microprocessor contains one ALU for purposes such as maintaining timers. We can say that ALU is a core component of all central processing unit within in a computer and is an integral part of the execution unit. ALU is capable of calculating the results of a wide variety of basic arithmetical and logical computations. The ALU takes as input the data to be operated on (called operands) and a code from the control unit indicating which operation to perform. The output is the result of the computation. The ALU implemented will perform the following operations:

Arithmetic operations (addition, subtraction, increment , decrement , transfer) .
Logic operations (AND, NOT, OR, EX-OR)
Shift operations (LSR,LSL).

A digital system can be represented at different levels of abstraction .. The highest level of abstraction is the **behavioral** level that describes a system in terms of what it does (or how it behaves) rather than in terms of its components and interconnection between them.Here the 32-bit ALU is implemented by using the behavioral modeling style to describe how the operation of ALU is being processed. This is accomplished by using a hardware description language VHDL.

The behavioral style makes use of a process statement. A process statement is the main construct in behavioral modeling that allows using sequential statements to describe the behavior of a system over time. Process is declared within an architecture and is a *concurrent* statement. However, the statements inside a process are executed *sequentially*.

## 2. 32 BIT ALU

32 bit ALU consists of an arithmetic unit, a logic unit, a shift unit, clock gating unit and an output multiplexer.

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### 2.1. 32 Bit Arithmetic Unit

The Arithmetic unit performs 7 operations such as addition, addition with carry, subtraction, subtraction with borrow, increment, decrement, transfer. The circuit consists of a 32 bit parallel adder and thirty two numbers of single bits 4:1 multiplexer. A and B is a 32 bit input and the output is 33 bit result, there is 2 common selection lines S0 and S1, Cin is carry input of the parallel adder and the carry out is Cout.

Fig-1: 32 Bit Arithmetic Unit

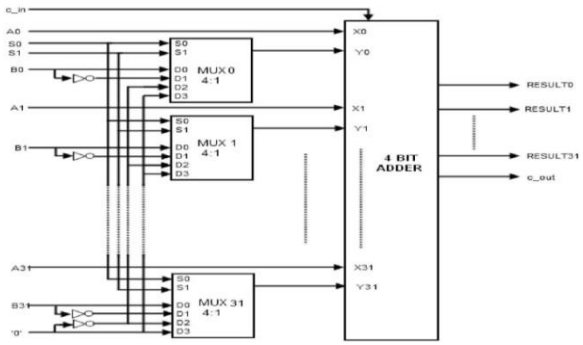


Table-1: Operation performed on Arithmetic Unit

| S1 | S0 | Cin | Result | Operation |
|---|---|---|---|---|
| 0 | 0 | 0 | A+B | Addition |
| 0 | 0 | 1 | A+B+1 | Addition with Carry |
| 0 | 1 | 0 | A+ $\overline{B}$ | Subtraction |
| 0 | 1 | 1 | A+ $\overline{B}$+1 | Subtraction with Borrow |
| 1 | 0 | 0 | A-1 | Decrement |
| 1 | 0 | 1 | A | Transfer |
| 1 | 1 | 0 | A | Transfer |
| 1 | 1 | 1 | A+1 | Increment |

### 2.2. 32 Bit Logic Unit

The Logic unit does the following tasks logical AND, logical OR, logical XOR, logical NOT and complement operation. The logic unit consists of four gates and a 4:1 multiplexer. The output of the gates is applied to the data inputs of the multiplexer. Using selection lines S0 and S1 one the data inputs of the multiplexer is selected as the output.

Fig-2: 32 Bit Logic Unit

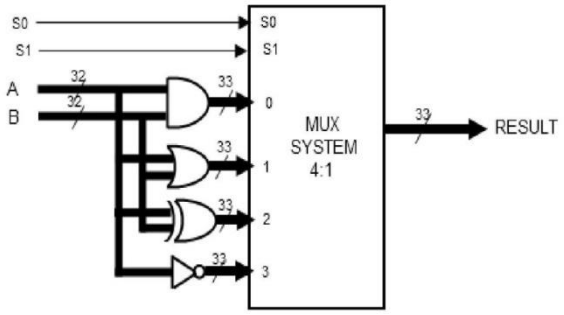


Table-2: Operation performed on Logic Unit

| S0 | S1 | Result | Operation |
|---|---|---|---|
| 0 | 0 | A.B | AND |
| 0 | 1 | A+B | OR |
| 1 | 0 | A $\oplus$ B | XOR |
| | | | |

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| | | | |
|---|---|---|---|
| 1 | 1 | Not A | Compliment A |

gives result which is original number multiplied by two similarly shifting n times to the left gives result which is equivalent to the original number multiplied by $2^n$ and Shift Right shifts one bit to the right gives result which is original number multiplied by two similarly n times to the right gives result which is equivalent to original number divide by $2^n$. For a shift unit of 32-bit, the output will be of 33-bit with 33th bit to be the outgoing bit.

Fig-3: 32 Bit Shift Unit

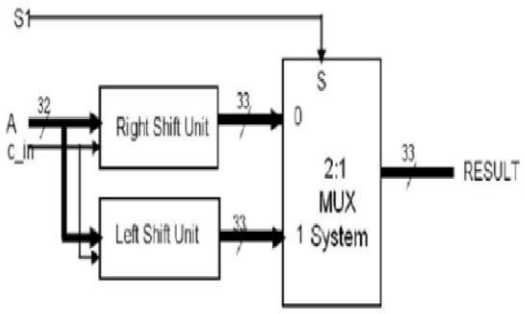


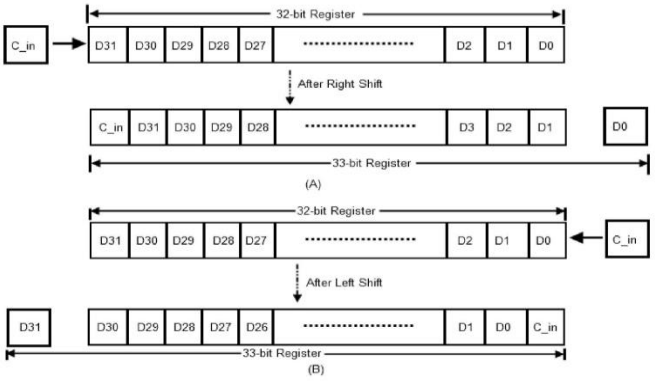

Table-3: Operation performed on Shift Unit

| S | Operation |
|---|---|
| 0 | Right Shift A |
| 1 | Left Shift A |

Fig-4: (a) 32-bit Right Shift Operation
(b) 32-bit Left Shift Operation

### 2.3. 32 Bit Shift Unit

Shift unit is used to perform logical shift operations. Shift left shifts one bit to the left




### 2.4. 32 Bit Arithmetic and Logical Unit

The approach used here is to split the ALU into three modules, one Arithmetic, one Logic and one Shift module. The arithmetic, logic and shifter units introduced earlier can be combined into ALU with common selection lines. The shift micro-operations are often performed in a separate unit, but sometimes the shifter unit made part of overall ALU. Since the ALU is composed of three units, namely Arithmetic, Logic and Shifter Units. For 32-bit ALU a 33 bit 4:1 MUX is needed. A particular arithmetic or logic or shift operation is selected according to the selection inputs $S_0$ and $S_1$. The final output of the ALU is determined by the set of multiplexers with selection lines $S_2$ and $S_3$. The function table for the

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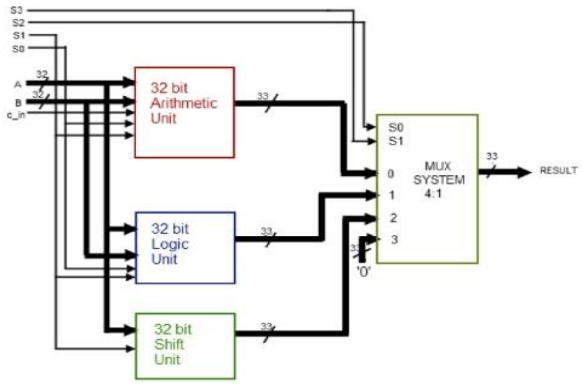
ALU is shown in the Table. 1. The table lists 14 micro-operations: 8 for arithmetic, 4 for logic and 2 for shifter unit. For shifter unit, the selection line $S_1$ is used to select either left or right shift micro-operation.

Fig-5: 32 Bit ALU Unit




| S3 | S2 | S1 | S0 | Cin | Result | Operation |
|---|---|---|---|---|---|---|
| 0 | 0 | 0 | 0 | 0 | A + B | Addition |
| 0 | 0 | 0 | 0 | 1 | A + B + 1 | Addition with carry |
| 0 | 0 | 0 | 1 | 0 | A + $\overline{B}$ | Subtraction |
| 0 | 0 | 0 | 1 | 1 | A + $\overline{B}$ + 1 | Subtraction with borrow |
| 0 | 0 | 1 | 0 | 0 | A - 1 | Decrement |
| 0 | 0 | 1 | 0 | 1 | A | Transfer |
| 0 | 0 | 1 | 1 | 0 | A | Transfer |
| 0 | 0 | 1 | 1 | 1 | A + 1 | Increment |
| 0 | 1 | 0 | 0 | X | A •B | AND |
| 0 | 1 | 0 | 1 | X | A + B | OR |
| 0 | 1 | 1 | 0 | X | A $\oplus$ B | XOR |
| 0 | 1 | 1 | 1 | X | $\overline{B}$ | Complement |
| 1 | 0 | 0 | X | X | LSR A | Shift Right |
| 1 | 0 | 1 | X | X | LSL A | Shift Left |

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## 3. SIMULATIONS AND IMPLEMENTATION

The 32 Bit ALU with clock gating is designed in VHDL using Xilinx ISE 12.4 design suite. The simulation is done using Modelsim Simulator with a clock period of 1 us. After the design is synthesized on a Spartan 3E device the design is implemented. The process of simulation uses a testbench to test the design whether it behaves correctly by stimulating it with artificial input and monitoring the output. The simulation is carried out by using the Modelsim 5.4a tool and having the testbench and the behavioral design code for 32-bit ALU in the same project folder.

### 3.1 Simulation Waveforms

Fig-6: Simulated Waveform for Arithmetic Unit

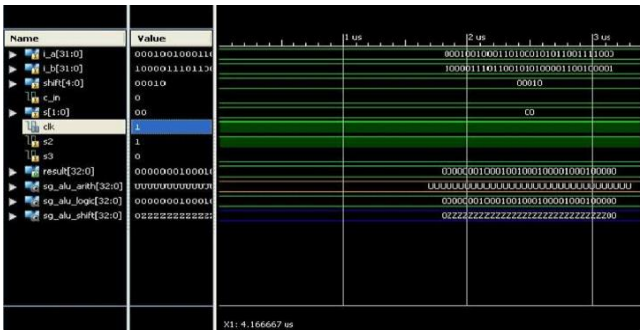



Fig-7: Simulated Waveform for Logic Unit

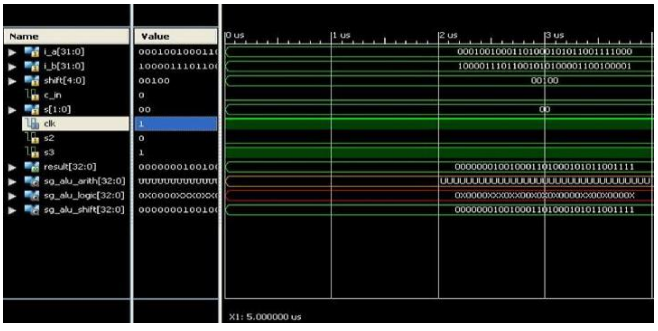
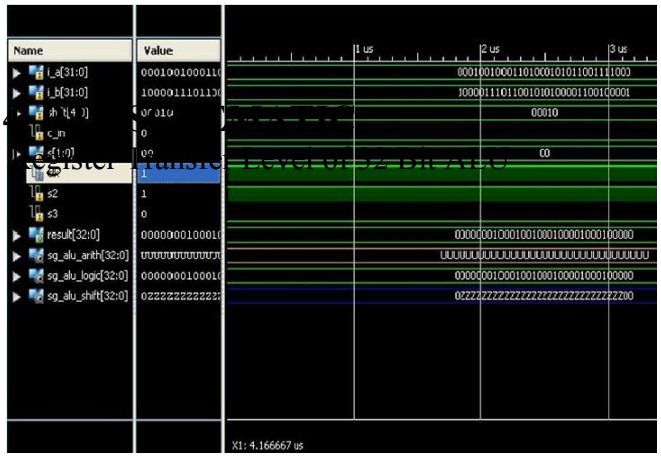
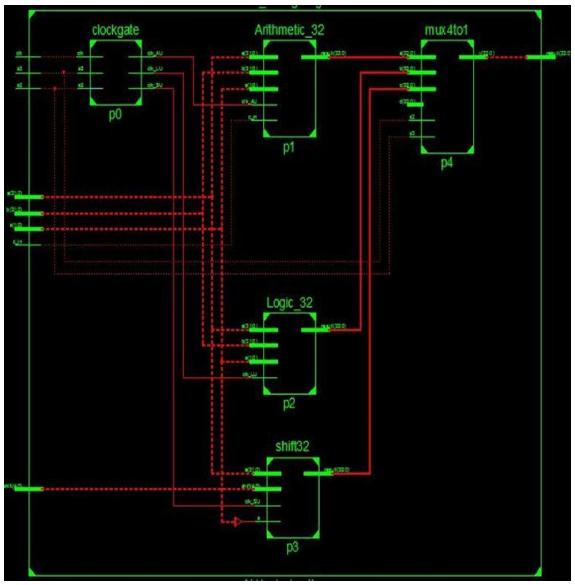



Fig-8: Simulated Waveform for Shift Unit




## 5. CONCLUSION

In our project "Design and Implementation of a 32-bit ALU on Xilinx FPGA using VHDL" we have designed and implemented a 32 bit ALU. Arithmetic Logic Unit is the part of a computer that performs all arithmetic computations, such as addition and subtraction, increment, decrement, shifting and all sorts of basic logical operations. The ALU is one component of the CPU (Central Processing Unit).

Here, using VHDL we have designed a 32 bit ALU which can perform the various arithmetic operations of Addition, Subtraction, Increment,

Decrement, Transfer, logical operations such as AND, OR, XOR, NOT and also the shift operation.
All the above mentioned operations are then verified to see whether they match theoretically or not. The above given waveforms show that they match completely thereby verifying our results.

## 6. Acknowledgement

It is our immense pleasure to find an opportunity to express our deep gratitude and sincerest thank to **Asst. Prof. Rupali Singh (SRM, Modinagar), Asst. Prof Meenakshi Sanadhya (SRM, Modinagar ) and Asst. Prof Arun Kumar (SRM, Modinagar)** for giving most valuable suggestion, helpful guidance and encouragement in completion of our project and providing us all possible assistance. They have been extremely motivating and helped during the execution of this project work that has led us to the successful completion of our project titled: "Design and Synthesis of a 32-bit ALU on Xilinx ISE v9.1i using VHDL". We highly appreciate the efforts and numerous suggestions that they structured our work with their valuable tips and accorded to us in every respect of our work. At last, we humbly extend our sincere appreciation to other faculty also who help and encouraged us in some way or during our working project environment.

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