A Novel Bandwidth management EDT scan-based test And TAM test application time and scheduling

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Abstract

This paper presents several techniques employed to resolve problems surfacing when applying scan bandwidth management to large industrial multicore system-on-chip (SoC) designs with embedded test data compression. These designs pose significant challenges to the channel management scheme, flow, and tools. This paper introduces several test logic architectures that facilitate preemptive test scheduling for SoC circuits with embedded deterministic test-based test data compression. The same solutions allow efficient handling of physical constraints in Realistic applications. Finally, state-of-the-art SoC test scheduling algorithms are architected accordingly by making provisions for: 1) setting up time-effective test configurations; 2) optimization of SoC pin partitions; 3) allocation of core-level channels based on scan data volume; and 4) more flexible core-wise usage of automatic test equipment channel resources. A detailed case study is illustrated herein with a variety of experiments allowing one to learn how to tradeoff different architectures and test-related factors.

Keywords: Bandwidth management; embedded deterministic test (EDT); scan-based test; test access mechanism (TAM); test application time; test compression; test scheduling.

1. Introduction

Bandwidth management is clearly a complex and evolving concern for most, if not all, network operators around the globe. A recent survey of over 400 European network operators found that blocking of voice-over-IP and peer-to-peer traffic is commonplace today. This survey also identified a very wide variety of traffic management practices, implementation methods and policy justifications. The rapid introduction of new Internet applications and services makes it hard for network operators to predict or robustly categorize uses of the network. Meanwhile, users want their Internet service to 'just work'. Building on an earlier briefing panel and associated report into the evolving landscape of Internet bandwidth, the Internet Society convened an invitational roundtable meeting of network operators, technologists, researchers and public policy experts with an interest in broadband regulation and deployment. This report documents the Internet Society Technology Roundtable meeting on the topic of bandwidth management that took place on October 11th and 12th 2012 in London, England.

At the macro scale there is a good story to tell about new fiber deployments, and more open and competitive cable consortia. However, dark fiber

availability is a local concern for some as fiber infrastructure operators seek to provide higher margin services. Content Delivery Networks are part of a larger architectural shift toward localized content delivery and content aggregation services. This shift yields benefits for network users in terms of quality of experience. Content aggregators are helping to meet the growing demand for Internet content but there still remain huge spikes in traffic related to new releases of software and other kinds of popular content that are creating new challenges for network capacity planners and performance engineers. Latency management is the key to understanding the causes and solutions to many of the performance problems witnessed on today's broadband access networks. There are opportunities for development and research stemming from this fact in terms of new algorithms, an improved access network router ecosystem and greater consumer and network operator awareness of the long-term costs of poor engineering and cheap products in this critical region of the end-to-end network path.

2. Related Work

2.1 Existing Method:

Today's multicore chip architectures require no trivialtest solutions imposed by the relentless miniaturizationof semiconductor devices, which have become much fasterand less power hungry than their predecessors. This trend hasgiven rise to the growing popularity of system-on-chip (SoC)designs because of their ability to encapsulate many disparate types of complex IP cores running at different clock rates with different power requirements and multiple power supplyvoltage levels. Many SoC-based test schemes proposed sofar utilize dedicated instrumentation, including test access mechanisms (TAMs) and test wrappers. TAMs are typically used to transfer test data between the SoCpins and embedded cores, whereas test wrappers form the interface between the core and SoC environment. Solutions involving both TAMs and wrappers accomplish such tasks as optimizing test interface architecture or control logic [20] while addressing routing and layout constraints or hierarchy of cores scheduling test procedures and minimizing power consumption Techniques proposed in and [attempt to minimize SoC test time. The integrated scheme of reduces the test time by optimizing dedicated TAMs and pin-count aware test scheduling. Packet-switched networks-on-chip can replace dedicated TAMs in testing of SoC by delivering test data through an on-chip communication infrastructure

2.2 Proposed Method:

ATE channel bandwidth management for SoC designs canplay a key role in increasing test data compression with no visible impact on test application time. The approach presented in encompasses: 1) a solver capable of using input and output channels dynamically; 2) test scheduling algorithms; and 3) TAM design schemes, all devised for the embedded deterministic test (EDT) environment [24]. It is assumed that all cores in the SoC are either heterogeneous modules, or wrapped testable units, and they come with their individual EDT-based compression logic, whichis subsequently interfaced with ATE through an optimizednumber of channels. As a result, test scheduling and TAMs can assign a fraction of the ATE interface capacity to each core. It increases compression ratios and allows tradeoffs between the test application time, volume of test data, test pin count, and interface design

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complexity. The scheme of is applicable to any SoC-based test data reduction scheme Capable of working with a varying number of in and output channels.

3. Implementation

The SoC test environment (Fig. 1) of this paper comprises two switching networks, as introduced in [13]. An external ATE In channel i (ICi) feeds an In-switching network that reroutes compressed test data to different cores (in the remaining parts of this paper a given core k is denoted as Ck)

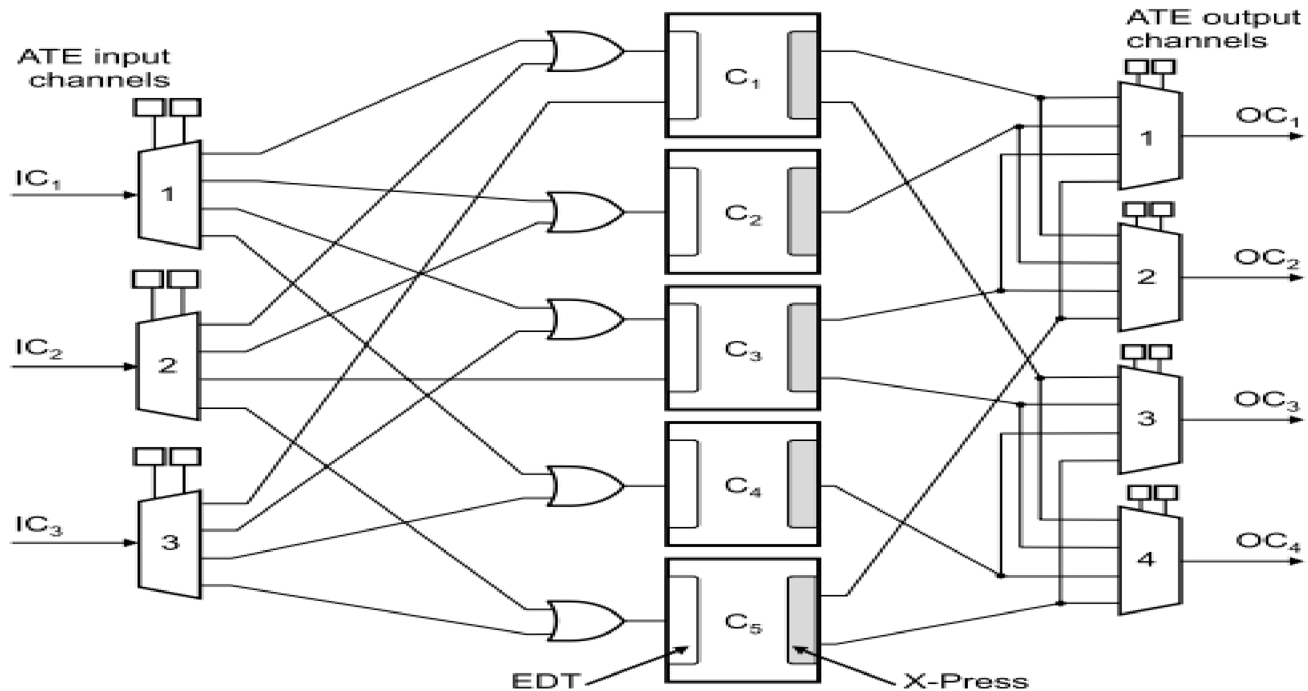

Fig 1: SoC test environment with on-chip compression.

based on the control data produced by a test scheduler. Since the scan routing paths from the chip-level test pins to the core-level test pins are dynamically selected by patterns, this interconnection network is also referred to as a dynamic scan router (DSR). Identical modules may share the same test data in the broadcast mode. In addition to individual EDT decompressors, each core features X-masking logic protecting its response compactor against unknown states and connectingthe core with an output-switching network. This network allows the compressed output streams from successive cores to reach an output channel i (OCi), and to be sent back to the ATE. In order to facilitate test pattern reuse, test wrappers isolate all cores so that they are independent of each other.

As shown in Fig. 1, the In DSR consists of demultiplexers whose number matches the number of ATE In channels. Given a group of test patterns, each demultiplexer connects the corresponding channel to one of several destination cores, as indicated by the content of address register. The number of ATE In channels cannot be smaller than the capacity of the largest single core in terms of its EDT In. Clearly, in the worst case, we can still test the largest cores, one at a time. Typically, low-order In of each core

are used more frequently than others [13]. Hence, OR gates are deployed to assure that these In can receive data from more than a single ATE channel to increase flexibility of a test scheduler.

Given the ATE In channels, the associated demultiplexers, and all cores with OR gates driving their EDT In, the actual connections between these terminals are arranged as follows. The EDT In (alternatively, OR gate In, if any) are connected with the demultiplexers in such a way that n EDT In of a given core are linked with n different ATE In channels, and each ATE channel serves approximately the same number of cores. This method yields the actual size of the In demultiplexers and their control registers. Some final adjustments within a single module are also possible to simplify the resultant DSR layout and avoid costly and long connections.

The output DSR (Fig. 1) interfaces all core outputs with the ATE by reducing the number of test response streams so that they fit into the number of output ATE channels. It is made up of a number of multiplexers such that each multiplexer serves to connect several cores with a designated ATE output channel. Again, the address registers specify which cores are to be observed for a given group of test patterns. The output channel mapping is carried out in a manner similar to that of the In DSR. Note that all core outputs feature a user-defined fan-out in order to increase flexibility of selecting observation points connected to the multiplexers. It is also assumed that all core outputs need to be observed when tested.

It is worth noting that a flexible use of ATE channels results in increased compression and elevated encoding efficiency. Moreover, testing many cores in parallel by dynamically allocating ATE channels to different cores in accordance with their needs may shorten test application time. Finally, having individual decompressors running in appropriate time slots makes it easier to reduce the number of external channels compared with the total number of EDT In featured by all cores together. In preparation for the actual test session, the following steps are carried out (a detailed description of this procedure can be found in [13]).

- For each core, automatic test pattern generation (ATPG)- produced test cubes are passed to a solver that merges and encodes them to arrive with final compressed test patterns; furthermore, the solver determines the minimal number of EDT In channels needed to compress a given test pattern.
- For each test pattern at the core level, information regarding the minimal number of EDT In channels is paired with data concerning the required EDT output channels.
- All test patterns are clustered to form groups (classes) of patterns having identical both In channels and observation points.
- Upon completion of the above operations for each core, all classes are passed to a test scheduler; given architecture of both test access networks and various constraints (ATE channels, DSR architecture, power consumption, and others), it yields the final allocation of ATE In/output channels to selected cores when applying successive test patterns.

4. Experimental Work

The experimental results are summarized in Table 1 for eight test cases, out of which four correspond to a fixed core-level channel count scenario where a given core is always assigned SoC pins to all of its EDT channels regardless of the actual test pattern requirements, whereas the next four cases represent a scalable core-level channel count scenario with the minimal number of SoC pins allocated to a given core for a particular test pattern. Furthermore, we consider four test setups, as described in Section III: two of them use the IJTAG architecture with a shift clock being 10 and 20 times slower than the scan shift clock, whereas the remaining two solutions deploy dedicated control chains and control bits attached to test patterns, respectively. In all experiments, the total number of internal wires within all (eight) DSRs, as shown in Fig. 1, was equal to 1795 (In) and 4200 (outputs). Furthermore, the same DSRs deployed exclusively in demultiplexers and output multiplexers driven by 4-bit address registers. In other words, the amount of control data per either In or output channel, whenever it needs to be provided, is equal to 4 bit.

For each test case, successive columns of Table 1 report the following performance-related statistics of the proposed schemes:

1) The total number of test patterns and the resultant number of base classes;

2) The channel fill rate indicating the actual usage of the ATE channels; it assumes the value of 1 only if all channels are used uninterruptedly till the end of test;

3) the test application time reported as the total number of shift cycles needed to deliver all test data in terms of the actual test patterns and the accompanying control bits; moreover the data to control ratio of both quantities is also reported here;

4) The test time reduction ratio relative to the original shift cycles.

Test scheduling	Test setup	Test patterns	Base classes	Channel fill rate	Data cycles $\times 10^6$	Control cycles $\times 10^6$	DCR [%]	Test time reduction [x]
Stuck-at faults								
Fixed channel count	IJTAG x10	42,931	24	0.67	18.89	0.48	2.5	2.21
	IJTAG x20	45,688	15	0.65	20.10	0.59	3.0	2.06
	Dedicated control chains	42,232	46	0.68	18.58	0.06	0.3	2.29
	Control bits per pattern	42,232	46	0.68	18.58	0.38	2.0	2.25
Scalable channel count	IJTAG x10	37,952	63	0.64	16.70	1.25	7.5	2.38
	IJTAG x20	39,765	46	0.63	17.49	1.83	10.4	2.21
	Dedicated control chains	35,436	126	0.68	15.59	0.09	0.6	2.73
	Control bits per pattern	35,436	126	0.68	15.59	0.30	2.0	2.69
Transition faults								
Fixed channel count	IJTAG x10	193,787	33	0.63	85.27	0.75	0.8	2.37
	IJTAG x20	194,488	23	0.61	85.57	1.05	1.2	2.35
	Dedicated control chains	192,708	41	0.65	84.79	0.21	0.2	2.40
	Control bits per pattern	192,708	41	0.65	84.79	1.93	2.3	2.35
Scalable channel count	IJTAG x10	150,224	72	0.63	66.10	2.22	3.4	2.98
	IJTAG x20	154,154	104	0.60	67.82	3.08	4.5	2.88
	Dedicated control chains	141,474	196	0.67	62.24	0.23	0.3	3.26
	Control bits per pattern	141,474	196	0.67	62.24	1.41	2.3	3.20

Table 1: Experimental Results.

EXPERIMENTAL RESULTS - II

Routing configuration	Setup	Wires in + out	Test patterns	Base classes	Data cycles $\times 10^6$	Control cycles $\times 10^6$	DCR [%]	Test time reduction [x]
Evenly distributed	3	1,656 + 3,150	39,637	142	17.44	0.10	0.59	2.44
	4	2,208 + 4,200	33,370	144	14.68	0.10	0.66	2.89
	5	2,760 + 5,250	32,007	122	14.08	0.09	0.61	3.02
Priority-based	3, 2, 1	1,278 + 2,863	36,421	131	16.03	0.09	0.59	2.65
	4, 3, 2	1,830 + 3,913	30,204	139	13.29	0.09	0.69	3.19
	5, 4, 3	2,382 + 4,963	28,340	116	12.47	0.08	0.64	3.41

Table 2: Experimental Results.

As indicated in Table 1, it appears that one can reduce up to 3.26 times the test application time compared with the baseline and still be able to deliver all necessary test patterns, thus preserving the original test quality. In particular, the largest test application time reduction is observed for test scenarios based on per pattern dynamic channel allocation while employing dedicated chains to deliver all required control test data. These results are even more evident for transition fault test sets. Further experimental results, not presented in Table 1, reveal an intrinsic relation between the ratio of In and output channels and the resultant test time reduction. The test time reduction clearly depends on the aforementioned ratio, and hence its careful selection, as shown in Section IV, may guarantee the shortest test application time. Additional results, reported in Table 2, try to capture the impact of a priority-based routing (as described in Section IV-C) on test time reduction. The experiments were run for stuck-at fault test sets by deploying scalable channel counts and dedicated control scan chains. The proposed test scheduling techniques have produced test scenarios for six test cases. In the first three ones, all core In are connected by means of demultiplexers to the same number (given by the Setup column) of different ATE channels. The next three cases correspond to a priority-based configuration with the connecting wires allocated individually per core In and for every group of cores (as shown again by the Setup column, which lists the number of wires used by each core In of each group). For example, in the first case (3, 2, and 1), there are three groups in total (A, B, and C), and each core In in A, B, and C is connected with 3, 2, and 1 ATE channels, respectively. For each test case, Table V reports performance statistics similar to those of Table 1. As can be seen, the test time can be significantly reduced if appropriate interconnection networks are used. For example, compare the last test cases reported for both scenarios. It appears that the test application time for the priority-based configuration is reduced up to 3.41 times, i.e., it outperforms the corresponding solution for the baseline configuration by 12% with the number of connecting wires reduced from 2760 to 2382.

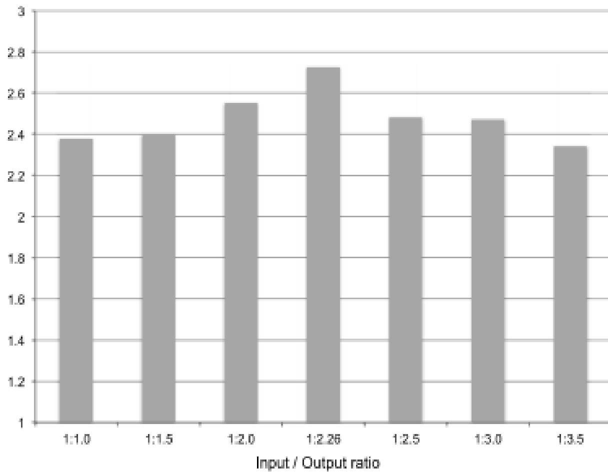

Fig 2: Test time reduction.

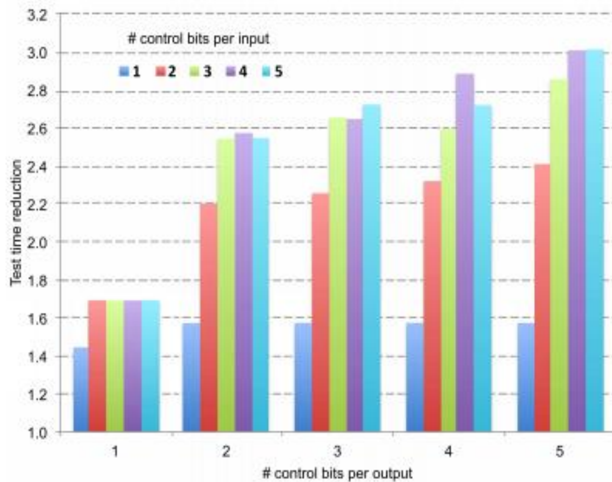

Fig 3: SoC complexity versus test time reduction.

5. Conclusion

As Moore's law continues to provide smaller devices, designs with a range of core counts, capability per core, and energy per core make a dramatic impact on SoC design and test procedures. As shown in this paper, the I/O resources provided by a tester can be dynamically allocated to selected cores, whereas the total number of channels in use may remain unchanged. This paradigm clearly calls for efficient schemes minimizing the overall test application time, while taking into account physical constraints, in particular, SoC pin allocations. Assuming that all SoC cores are wrapped testable units, this paper studies several practical issues regarding SoC-based testing that deploys on-chip test data compression with the ability to dynamically use ATE channels. The proposed solutions include methods used to deliver control data and test scheduling algorithms minimizing the overall test application time. Experimental results obtained for a large industrial SoC design confirm feasibility of the proposed schemes and their ability to trade-off the number of test pins, design complexity of the TAM, and test application time.

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