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Digital and parallel distributed arithmetic parallel-prefix adder residue number system for reverse converter

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Abstract

In this brief, the design of reverse converter using parallel prefix adder based multiplier for residue number system is proposed. Nowadays the parallel prefix adders are not used even though it provides significant delay reduction and high speed operation because of higher power consumption. The novel specific hybrid parallel prefix adder components that compensate the delay and power consumption in the existing system is applied to design the reverse converter. Different parallel adder structures are analyzed among that the Brent Kung prefix network is used for the parallel prefix addition because of the minimum fanout. In the proposed system the high speed parallel prefix adder is designed for modulo (4n+1) addition for n=5 and thereby designing the multiplier by using the shifting operation in the same design.

Keywords: Digital arithmetic; parallel-prefix adder (PPX); residue number system (RNS); parallel distributed arithmetic convolution architecture; reverse converter.

1. Introduction

The Residue Number System plays a significant role in the battery based and portable devices because of its low power features and its competitive delay. The Residue number system reverse converter is designed with parallel prefix addition by using new components methodology for higher speed operation[1].The RNS consists of two main components forward and the reverse converter that are integrated with the existing digital system. The forward converter performs the operation of converting the binary number to the modulo number whereas the reverse converter performs the operation of reverse converting the modulo number to the binary number which is the hard and time consuming process compared with the forward converter. The fundamental RNS concepts such as 1)RNS definition with properties and their applications,2)consideration of modulo set selection,3)design of forward converter,4)modulo arithmetic units,4)design of reverse converter are discussed[2].

The voltage over scaling(VOS) technique is applied to the residue number system to achieve high energy efficiency. The VOS technique introduces soft errors which degrades the performance of the system. To overcome these soft errors a new technique is implemented called joint RNS-RPR(JRR) which is the combination of RNS and the reduced precision redundancy. This method provides the advantage of satisfying

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the basic properties of RNS includes shorter critical path, reduced complexity and low power[3].New architectures are presented for the moduli sets(2n- 1,2n,2n+1) for the conversion from the residue to the binary equivalents[4].Here the speed and the cost are major concern. Distributed arithmetic principles are used to perform the inner product computation in[5].The input data which are in the residue domain which are encoded using the Thermometer code format and the ouputs are encoded using the One hot code format. Compared to the conventional method which used Binary code format, the proposed system which achieves higher operating speed. The residue number system which provides carry free addition and fully arithmetic operation[6],for several applications such as digital signal processing and cryptography[7]-[11]. In this brief, we present a comprehensive method which uses the parallel prefix adder in selected position, thereby using the shift operation on one bit left to design a multiplier on the same design module to achieve a fast reverse converter design.

The usage on parallel prefix structure in the design leads to higher speed in operation meanwhile it increases the area and power consumption. Inorder to compensate the tradeoff between the speed, area and power consumption, a novel specific hybrid parallel prefix based adder components are used to design the reverse converter. These hybrid design which provides the significant reduction in the power delay product(PDP)metric and leads to considerable improvements in the area time^2 product(AT^2) in comparison with the traditional converters without using parallel prefix adders.

2. Related Work

The Residue number system mainly composed of three main parts such as, forward converter, modulo arithmetic units and reverse converter. On comparing with the other parts the reverse converter design is a complex and no modular structure. So more attention is needed in designing the reverse converter thereby preventing the slow operation and compromises the benefits of the RNS. The parallel prefix structure helps to achieve the faster operation in the reverse converter design but causes increased power consumption. In the existing system the novel specific hybrid parallel prefix adder based components are used to replace the existing components thereby reducing the power consumption and getting faster operation.

A. ParalleL Prefix Block:

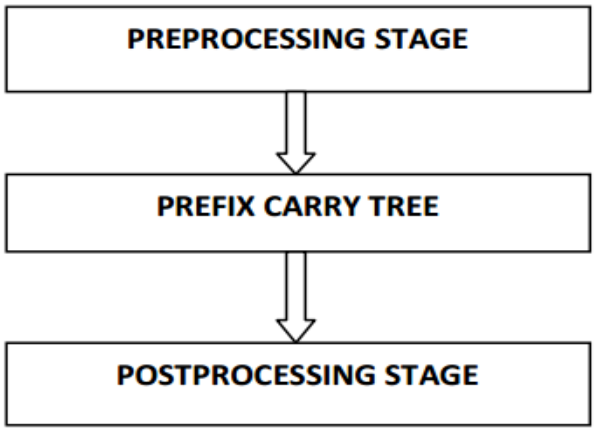

Fig 1(a): Basic Parallel prefix structure.

The Parallel prefix structure consists of three main blocks, they are preprocessing block, prefix carry tree and post processing block. The parallel prefix adder operation begins with preprocessing stage by generating the Generate (Gi) and Propogate (Pi) equation [1] & [3]. The prefix carry tree get proceeded with the previous block signal to yield all carry bit signal and these stage contains three logic complex cells such as Black cell, Gray cell and Buffer cell. Black cell

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compute both the propogate (P(i,j)) and generate (G(i,j)) by using the equation[3] &[4].The Gray cell executes only the generate(G(i,j)).The carry bits generated in the second stage get passed to the post processing block thereby generating the sum using the equation[5].The block diagram is shown in the Fig.1(a).

Gm:n=An AND Bn (1)

G0 =Cin (2)

Pm:n=An XOR Bn (3)

P0 =0 (4)

Gm:n=Gn:k OR Pn:k AND Gk-1:n (5)

Pm:n=Pn:k AND Pk-1:j (6)

Sn =Pn XOR Cin (7)

The Brent Kung adder prefix structure is employed to achieve the higher speed with reduced power consumption. On comparing with the other parallel prefix adder structure the BK adder is chosen mainly for minimum fanout and should be higher speed in operation than others.Fig.1.(b) shows the example BK adder prefix structure which uses the three basic cells in the prefix structure. These structure is elaborated for the proposed design having the modulo addition of (4n+1) for n=5.

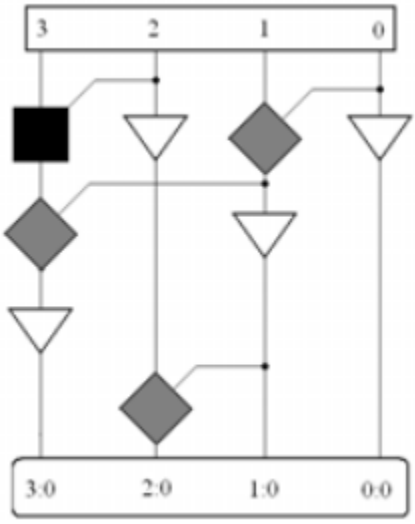

Fig 1(b): 4-bit BK adder prefix structure.

B. HRPX Structure: (Hybrid Regular Parallel prefix XOR/OR adder component)

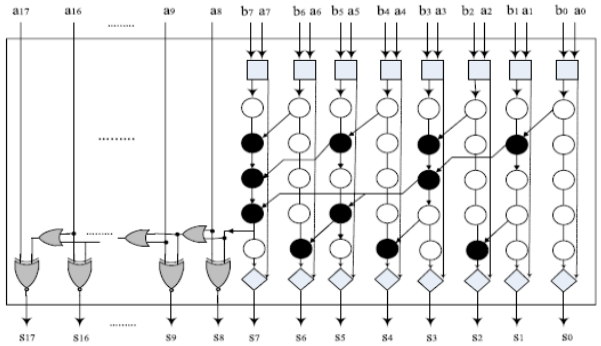

Fig 2: HRPX Structure using BK prefix network.

Fig. 2 shows HRPX Structure. The regular parallel prefix adder is used to do the first part of addition and the simplified RCA logic is used to do the second part where the corresponding bits of the operand are fully variable. Full adder can be designed with XOR/OR gates because of the constant operand. In this reverse converter design the carry chain is not needed and can be ignored. For most modulo sets (2^n-1) addition is a necessary operation. The End around Carry (EAC) for (2^n-1) addition is represented with two zero, but for the reverse converter design one zero representation is required. To correct these zero representation problem, a detector circuit was employed in the design but it incorporates additional delay. So, the Binary to excess one converter (BEC) is used to solve the double zero representation issue.

C. HMPE Structure (Hybrid Modular Parallel prefix Excess one adder component)

The HMPE Structure consists of two parts: Regular prefix adder and the Modified Excess One unit. The first two operands are added using the parallel prefix adder and the result is

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conditionally incremented based on the control signal generated by the prefix structure to assure the single zero representation.

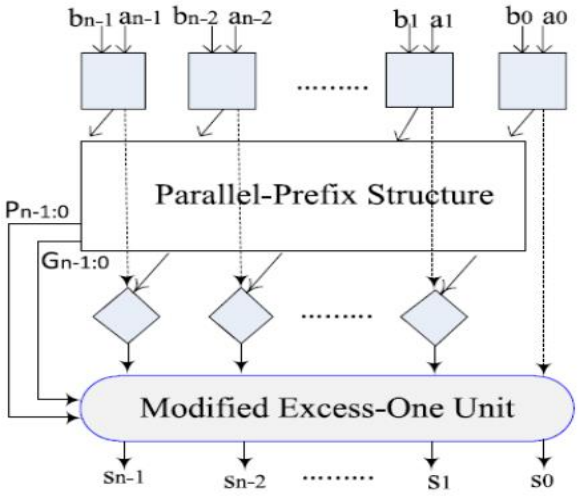

Fig 3: HMPE Structure.

D. Modified Excess One unit Description

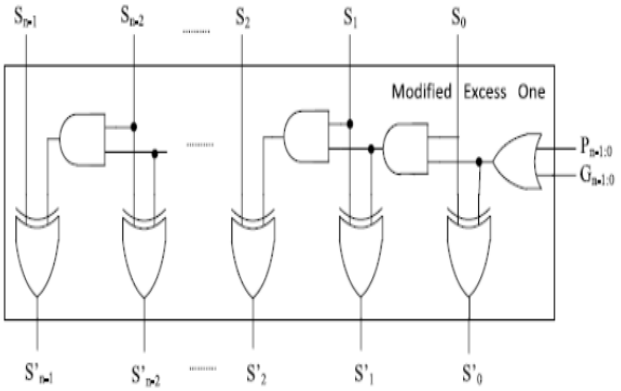

Fig 4: shows the Modified Excess One unit circuit diagram.

The result generated by the prefix structure is conditionally incremented by this unit based on the control signal generated by the parallel prefix adder.

3. Implementation

The proposed design, as shown in Fig.3 .The reverse converter design is implemented for (4n+1)modulo addition(n=5) designing the adder and also the multiplier by using the same adder design without using any parallel prefix multiplier structure for designing multiplier.

In this design, the adder design is implemented by using the BK adder parallel prefix structure. Here the first two operands are added by using the prefix adder preprocessing stage thereby generating the propogate and generate equation. The first stage processed signal get passed to the next stage called the prefix carry tree, this stage again computes the generate and propogate equation by using the previous output and all the logic cells employed in the BK adder network. These processed signals are passed to the post processing block.

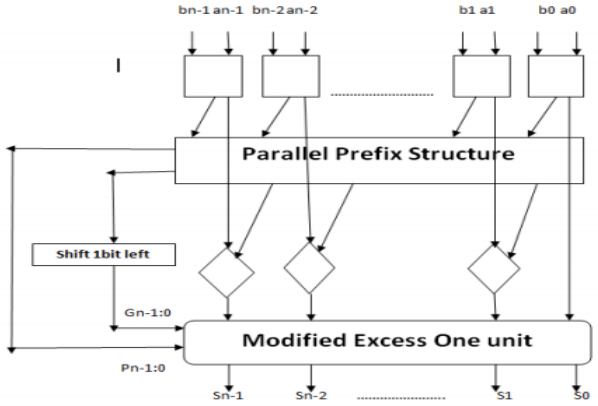

Fig 5: Parallel prefix adder based multiplier design.

The generated carry bits in first two stages of the parallel prefix network get passed to the last stage. Again the generated and propogated signal in the second stage get passed to the last stage called the post processing stage, this stage computes the sum and the carryout signal by using the processed generate and propogate equation to design the adder for (4n+1)modulo addition for n=5.In that design the propogated signal or the generated signal get left shifted to 1-bit position and then the sum get obtained for designing the multiplier.

4. Experimental Results

The circuit can be designed and specified in Verilog. For four different values of n(4,8,12,16)are considered in the base paper whose experimental results are compared with the prosed vale of n=5.When comparing with the fully prefix adders, the area,power,AT^2 AND PDP of the proposed design is significantly improved. The PDP for the proposed converters are worse when compared with the RCA based, but this one get improved for the larger value of n(i.e)for n=16 the HMPE and HRPX better improvement on PDP over RCA based one. The main goal is to provide a better tradeoff between the delay and the power consumption. The delay occurs in the multiplier design is mainly due to shift operation. For instance at n=16,63% of power is saved at the expense of 35% of delay increase and also there is 42% of improvement in the PDP metric when comparing with the fully parallel prefix adder design. The proposed design consumes more power in order to operate in higher speed when compared with the RCA based one.

The comparison Table1.for different n values using HMPE-BK network in described below. These table provides the comparison including the area ,power consumption,AT^2 metric and PDP metrics to analyse the performance of the existing one with the proposed one. The proposed prefix adder based component allows us to achieve the better trade off between the cost and the speed thereby choosing the correct adder structure. The different parallel prefix adder structures are analysed based on the area, power consumption and speed, by using that evaluated value computed in the table [1].

Table 1. Comparison table for different n values using HMPE-BK Adder network

HMPE-BK Prefix network				
n value	AT^2	PDP	Delay	Power consumption
n=4	5610	2.67	0.5	5.916
n=8	11310	5.28	0.27	9.512
n=12	15875	7.57	0.285	11.72
n=16	18960	10.00	0.455	15.17
n=20	21220	12.46	0.51	18.23

5. Conclusion

In this paper, the reverse converter can be implemented by using the BK parallel prefix adder network and the parallel prefix adder components are designed by using novel specific hybrid adder components for faster operation and reduced power consumption. The parallel prefix adder can be implemented upto (4n+1) modulo addition for n=5 in Verilog. The same adder design can be used for designing the multiplier by using the shift operation.

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