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Design of an Energy Efficient, High Speed, Low Power Full Subtract or Using GDI Technique

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Abstract—

This paper proposes the design of an energy efficient, high speed and low power full subtractor using Gate Diffusion Input (GDI) technique. The entire design has been performed in 150nm technology and on comparison with a full subtract or employing the conventional CMOS transistors, transmission gates and Complementary Pass-Transistor Logic (CPL), respectively it has been found that there is a considerable amount of reduction in Average Power consumption (Pavg), delay time as well as Power Delay Product (PDP). Pavg is as low as 13.96nW while the delay time is found to be 18.02pico second thereby giving a PDP as low as 2.51x10-19 Joule for 1 volt power supply. In addition to this there is a significant reduction in transistor count compared to traditional full subtractor employing CMOS transistors, transmission gates and CPL, accordingly implying minimization of area. The simulation of the proposed design has been carried out in Tanner SPICE and the layout has been designed in Microwind.

I. INTRODUCTION

A subtractor is one of the significant building blocks in the construction of a binary divider [1], [2]. In recent times, applications are aimed at battery operated devices so that power dissipation becomes one of the primary design constraints [3]–[10]. In the past processor speed, circuit speed, area, performance, cost and reliability were of prime importance. Power consumption was of secondary concern. However, in recent years power consumption is being given equal importance. The reason for such a hanging trend is attributed probably due to the rapid increase in portable computing devices and wireless communication systems which demand high speed computations and complex functionality with low power consumption. In addition to this high performance processors consume severe power which in turn increases the cost associated with packaging and cooling. Subsequently there is a rise in the power density of VLSI chips thereby disturbing the reliability. It has been found that every 10o rise in operating temperature roughly doubles the failure rate of components made up of Silicon due to several Silicon failure mechanisms such as thermal runaway, junction diffusion, electro migration diffusion, electrical parameter shift, package related failure and Silicon interconnect failure [11]. From the environment point of view, the lesser the power dissipation of electronic components, lesser will be the heat dissipated in rooms which in turn will have a positive impact on the global environment. Also, lesser electricity will be consumed. Therefore, for further optimization of performance of a full subtractor in terms of power consumption, delay time as well as Power Delay Product (PDP), a new low power, high speed energy efficient full

subtractor is being proposed using Gate Diffusion Input (GDI) technique. GDI is a novel modus operandi for low power digital circuits. This procedure allows reduction in power consumption, propagation delay and transistor count of digital circuit. The method can be used to minimize the number of transistors compared to conventional Complementary Pass-transistor Logic (CPL) and Dual Pass transistor Logic (DPL) CMOS design. The proposed subtractor has a transistor count of 14— a reduction of 72.00%, 63.16% and 58.82% compared to a full subtractor composed of CMOS logic, transmission gates and CPL, proposing a reduction in area. In order to establish the technology independence of the design the proposed subtractor has been simulated using 150nm technology. The current paper is systematized as follows: Section II gives a brief account of the Gate Diffusion Input (GDI) technique while ection III shows some of the logic gates that can be generated using GDI procedure along with a pithy analysis. Section IV presents the full subtractor that is intended for proposition while Section V imparts the simulation and performance analysis of the proposed full subtractor. Section VI concludes the paper.

II. GATE DIFFUSION INPUT (GDI)

Gate Diffusion Input (GDI) method is based on the utilization of a simple cell as shown in Fig. 1 which can be used for low power digital circuits [3]. This technique is implemented in twin-well CMOS or Silicon on Insulator (SOI) technologies. In this process, the bulks of both NMOS and PMOS transistors are hardwired to their diffusions to reduce the bulk effect that is dependence of threshold voltage on source-to-bulk voltage [12]. The dependence of transistor threshold voltage on source-to-bulk voltage is as follows:

$$V_{th} = V_{th0} + \gamma\left(\sqrt{|2\phi_F + V_{SB}|} - \sqrt{|2\phi_F|}\right) - \eta V_{DS} \qquad (1)$$

Where VSB is source-body voltage, Vth0 is threshold voltage at VSB=0, γ is linearized body coefficient, ΦF is the Fermi potential and η is Drain Induced Barrier Lowering (DIBL) coefficient. Using this procedure power consumption can be reduced along with delay time thereby delivering a reduced power delay product. Consequently area of the circuit is minimized.

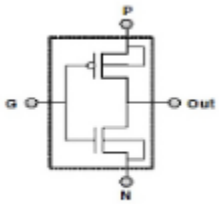

Figure 1: Basic GDI Cell

It should be noted that though the circuit resembles with standard CMOS inverter, there are certain important differences compared to conventional one. The GDIinput to the outer diffusion node of the PMOS transistor is not connected to Vdd while N which is the input to the outer diffusion node of the NMOS transistor is not connected to GND, and G which is the common gate input of both the NMOS and PMOS transistors. The Out node which is the common diffusion of both the transistors may be utilized as input or output port depending on the circuit configuration. The ports P and N delivers 2 extra pins which yield the DI design more compliant than the usual CMOS design [3]. Fig. 2 shows the transient response of a GDI cell which is quite similar to that of a standard CMOS inverter [13], [14]. This analysis is based on the Shockley model in which the drain current ID is represented

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as shown below [3]: cell contains 3 inputs— P which is the

$$I_D = \begin{cases} I_{D0}\left(\frac{W}{L}\right) e^{(qV_{GS}/KT)} \\ \quad (V_{GS} \le V_{TH} : \text{subthreshold region}) \\ K\{(V_{GS} - V_{TH})V_{DS} - 0.5V_{DS}^2\} \\ \quad (V_{DS} < V_{GS} - V_{TH} : \text{linear region}) \\ 0.5K(V_{GS} - V_{TH})^2 \\ \quad (V_{DS} \ge V_{GS} - V_{TH} : \text{saturation region}) \end{cases} \quad (2)$$

Where K denotes device transconductance parameter, VTH denotes threshold voltage, W denotes channel width and L denotes channel length.

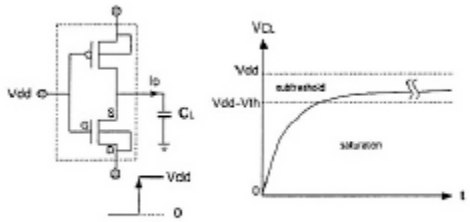

Figure 2: Transient response of a GDI cell [3]

However, it is to be mentioned that in GDI cell Vds has to be considered as a variable of input voltage in Shockley model [3] in contrast with CMOS inverter analysis [15] where Vgs was considered as an input voltage. Table I shows the various operations that can be performed with a basic GDI cell.

TABLE I. DIFFERENT OPERATIONS OF BASIC GDI CELL [3]

N	P	G	Out	Operation
'0'	B	A	AB	F1
B	'1'	A	A+B	F2
'1'	B	A	A+B	OR
B	'0'	A	AB	AND
C	B	A	AB+AC	MUX
'0'	'1'	A	A	NOT

From table I, it can be noticed that using only 2 transistors various functions can be performed. For instance, OR gate can be designed using a single GDI cell whereas in case of designing of an OR gate utilizing transmission gates, it required 6 transistors. Similarly, AND(MUX) can be devised using a single GDI cell. Thus, a simple alteration to the input configuration of the GDI cell would yield myriad variety of Boolean functions. Multiple-input gates can be implemented by combining several GDI cells. The main advantage of GDI cell is that a huge number of functions can be carried out using basic GDI cell. The GDI gates are more compact and flexible compared to static CMOS gates and have very low leakage current. This is due to the unique structure of the GDI cell which purges both the sub-threshold as well as gate leakage current [16].

III. LOGIC GATES BASED ON GDI METHOD

A. XOR gate based on GDI method

Fig. 3 shows the design of a XOR gate based on GDI procedure. It contains two GDI cells in which the first cell acts as a basic inverter while for the second cell 'x' is given as an input to port P of the GDIcell whereas 'y' is given as an input to port G and the output of the first cell is given as an input to port N of the second cell. gate can be designed using only 2 transistors and even a Multiplexer

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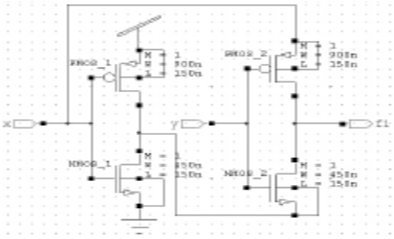

Figure 3: XOR gate using GDI method

Fig. 4 shows the input and output waveforms of a XOR gate designed using GDI technique in 150nm technology.

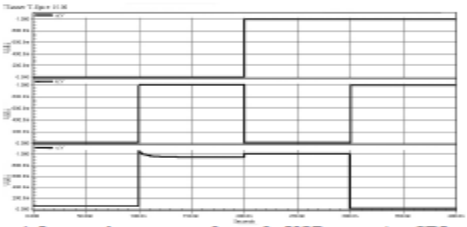

Figure 4: Input and output waveform of a XOR gate using GDI method in 150nm technology

B. AND Gate based on GDI method

Fig. 5 shows the design of an AND gate based on GDI method. It requires a single GDI cell in which the source of the PMOS that is port P is connected to GND and A is given as an input to port G while port N is supplied input B.

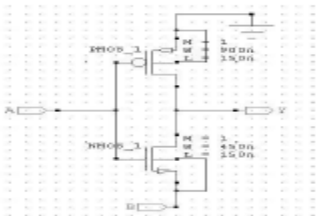

Figure 5: AND gate using GDI method

Fig. 6 shows the input and output waveforms of an AND gate conceived using GDI procedure in 150nm technology.

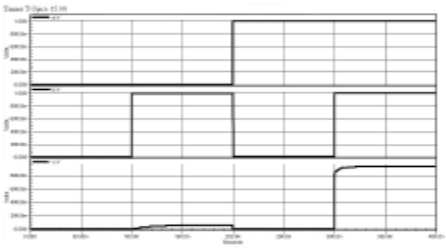

Figure 6: Input and output waveform of an AND gate using GDI method in 150nm technology

C. OR Gate based on GDI method

The OR gate consists of a single GDI cell as shown in Fig.7 where port P is given an input B, port G an input A while port N is supplied with Vdd.

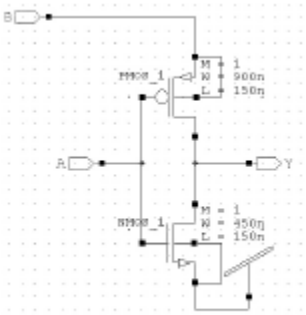

Figure 7: OR gate using GDI method

Fig. 8 shows the input and output waveforms of an OR gate constructed using GDI method in 150nm technology.

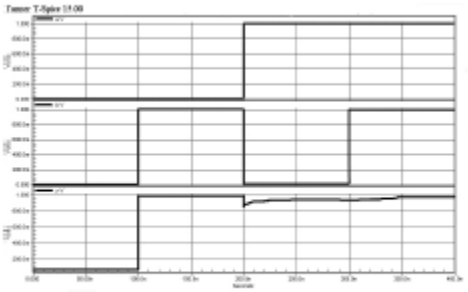

Figure 8: Input and output waveform of an OR gate using GDI method in 150nm technology

D. NOT Gate based on GDI method

The design of the NOT gate based on GDI procedure is similar to that of a standard CMOS inverter which is quite evident from table I. Fig. 9 shows the circuit diagram of a NOT gate derived using GDI technique.

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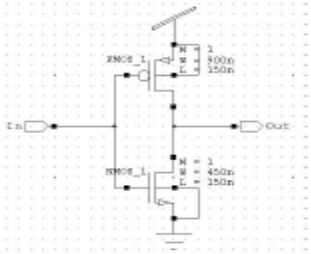

Figure 9: NOT gate using GDI method

Fig. 10 shows the input and output waveforms of the NOT gate via GDI approach in 150nm technology.

Figure 10: Input and output waveform of NOT gate using GDI method in 150nm technology

Fig. 11 displays a graphical comparative study of the average power consumption of the XOR, AND and OR gate based on GDI method with respect to those designed using conventional CMOS logic, transmission gates (TG) and CPL in 150nm technology.

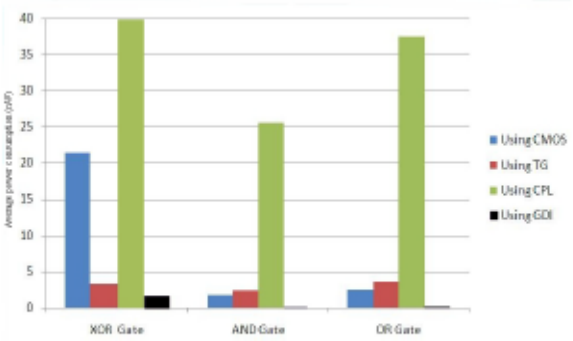

Figure 11: Graphical analysis of the average power consumption (nW) in 150nm technology

Since the design of a NOT gate based on GDI method is equivalent to the conventional CMOS inverter, comparison between them would be insignificant. The average power consumption of the NOT gate by means of GDI process in 150nm technology is 3.01x10-10 watts on application of a power supply voltage (VDD) of 1.0 volt.

IV. DESIGN OF THE PROPOSED FULL SUBTRACTOR

A full subtractor is a combinational circuit which performs subtraction on 3 bits that is minuend bit, subtrahend bit and the orrow bit from the previous stage. Therefore, a subtractor has 3 inputs– X (minuend), Y (subtrahend) and Z (Borrow from previous stage), and 2 outputs– D (difference) and B (Borrow out). The truth table for thefull subtractor is displayed in table II.

TABLE II. TRUTH TABLE OF A FULL SUBTRACTOR

X	Y	Z	D	B
0	0	0	0	0
0	0	1	1	1
0	1	0	1	1
0	1	1	0	1
1	0	0	1	0
1	0	1	0	0
1	1	0	0	0
1	1	1	1	1

The Boolean expressions for the design of the full subtractor are as follows:

$$D = X \oplus Y \oplus Z \quad (3)$$

$$B = Z \cdot (\overline{X \oplus Y}) + \overline{X} \cdot Y \quad (4)$$

Where D denotes difference and B represents the borrow.

In the current paper, we propose the design of the full subtractor using GDI technique which will consume lesser power, exhibit higher speed thereby delivering a better power delay product along with a reduced transistor count. The design of the AND, XOR, OR and NOT gates using GDI procedure has already been discussed in section III. Using these logic gates, we propose a new circuit design of the full subtractor. The logic circuit of the full subtractor is shown in Fig. 12.

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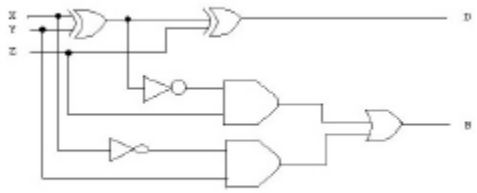

Figure 12: Logic Circuit of full subtractor

The circuit diagram of the proposed full subtractor is shown in Fig. 13 while fig. 14 depicts the corresponding layout design. The W/L ratio of all PMOS transistors is taken to be 6/1 whereas the W/L ratio of all NMOS transistors is taken to be 3/1.

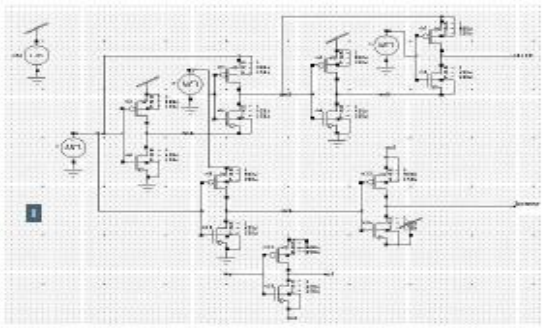

Figure 13: Circuit diagram of the proposed full subtractor

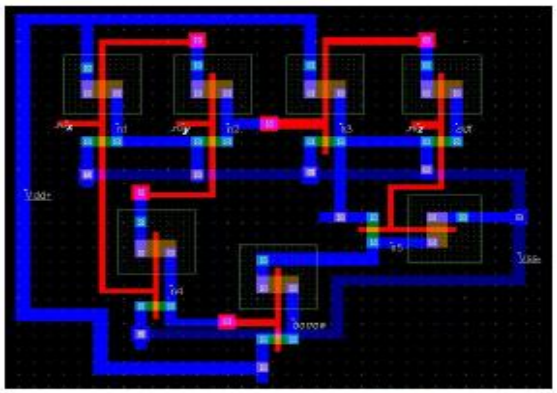

Figure 14: Layout design of the proposed full subtractor

V. SIMULATION AND PERFORMANCE ANALYSIS

The proposed full subtractor has been simulated with all combinations of inputs with rise and fall time of 0.1ns, respectively. The circuit operates satisfactorily at a power supply voltage of 1 volt. The pulse width, low time and high time has been taken to be 100 ns, respectively. Schematic for the proposed circuit have been done using Tanner S-Edit in 150nm technology using BSIM3 Ver.3.3.0. Schematics are used to obtain the netlist of the proposed circuit, and netlist is used for simulation and test. The input and output waveforms for the proposed full subtractor are shown in Fig. 15.

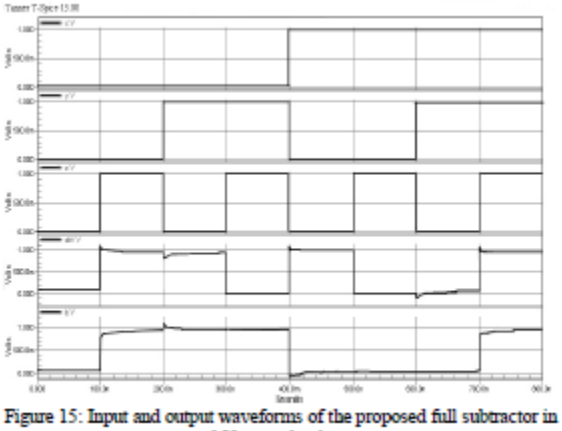

Figure 15: Input and output waveforms of the proposed full subtractor in 150nm technology

Table III shows a comparative study of the performance parameters of the proposed full subtractor employing Gate Diffusion Input (GDI) technique with respect to a full subtractor employing standard CMOS procedure, transmission gates (TG) and Complementary Pass Transistor Logic (CPL).

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TABLE III. COMPARATIVE STUDY OF THE PERFORMANCE PARAMETERS OF FULL SUBTRACTORS

Parameter	Full Subtractor employing standard CMOS Technique	Full Subtractor employing standard Transmission Gates (TG)	Full Subtractor employing Complementary Pass-Transistor Logic (CPL)	Full Subtractor employing Gate Diffusion Input (GDI) Technique
Number of transistors used	50	38	34	14
Average Power Consumed (watts)	4.395×10^{-6}	1.244×10^{-7}	1.006×10^{-4}	1.396×10^{-8}
Delay time (ps)	118.92	115.47	125.82	18.02
Power delay product (J)	5.23×10^{-16}	1.44×10^{-17}	1.26×10^{-14}	2.51×10^{-19}
Surface area (cm^2)	3.24×10^{-5}	1.18×10^{-5}	1.82×10^{-5}	8.92×10^{-7}

Fig. 16 shows a graphical analysis of the performance parameters of the proposed full subtractor (FS_GDI) with respect to full subtractor molded of traditional CMOS (FS_CMOS), transmission gates (FS_TG) as well as Complementary Pass-Transistor Logic (FS_CPL).

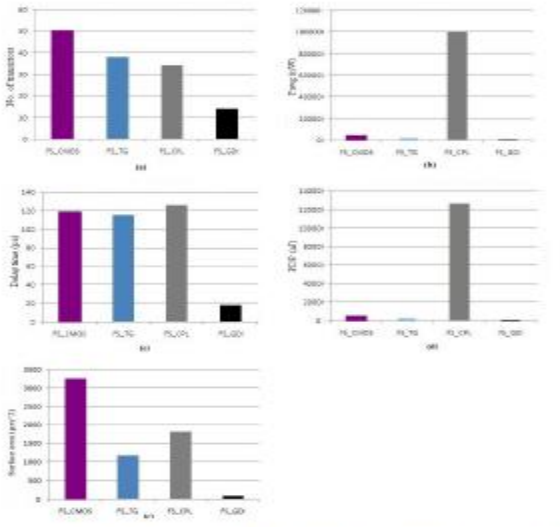

Figure 16: Graphical analysis of proposed full subtractor employing GDI technique w.r.t those employing standard CMOS method, transmission gates and CPL in terms of (a) Number of transistors (b) Average power consumption in nW (c) Delay time in ps (d) Power delay product (PDP) in aJ (e) Surface area in μm^2

From table III as well as from Fig. 16, it can be seen clearly that a reduction of 72.00%, 63.16% and 58.82% in transistor count is obtained while using the GDI method for designing the proposed full subtractor compared to a full subtractor possessing CMOS transistors, transmission gates and CPL, respectively. On the other hand, using GDI technique a reduction of 99.68%, 88.78% and 99.99% in average power consumption is attained compared to a full subtractor made up of CMOS transistors, transmission gates and CPL, correspondingly. A decline of 84.85%, 84.39% with 85.68% in average delay time is gained while a significant deterioration of 99.95%, 98.25% as well as 99.99% in power delay product is achieved using the GDI technique for devising the recommended full subtractor contrasted to a full subtractor containing CMOS transistors, transmission gates and CPL. In addition to this a remarkable descent of 97.24%, 92.42% and 95.10% in surface area is acquired while utilizing the GDI scheme to conceive the proposed full subtractor compared to a full subtractor embracing the regular CMOS transistors, transmission gates and CPL, respectively.

VI. CONCLUSION

The current work proposes the design of a full subtractor using Gate Diffusion Input (GDI) procedure which on simulation has been found to consume low power in conjunction with lesser delay time and fewer transistors while maintaining proper output-voltage swing. In order to establish the technology independence the present work has been performed in 150nm technology using Tanner SPICE and the layout has been concocted in Microwind. Comparisons with standard CMOS, transmission gate and CPL techniques showed a reduction of 72.00%,

63.16% and 58.82% in terms of transistor count, 88.78% and 99.99% in terms of average power consumption, 84.85%, 84.39% and 85.68% in terms of delay time and a significant 99.95%, 98.25 % and 99.99% in terms of power delay product, respectively. Furthermore, a depreciation of 97.24%, 92.42% together with 95.10% in surface area is reaped when judged against a full subtractor composed adopting the popular CMOS approach, transmission gatesand CPL, proportionately. Because of the noteworthy minimization of power delay product, transistor count and surface area the proposed logic can be useful in portable and low power applications

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