International Journal of Research
Available at https://edupediapublications.org/journals
p-ISSN: 2348-6848
e-ISSN: 2348-795X
Volume 03 Issue 10
June 2016

Design and Simulation of PV Based Multi Level Inverter to Reduce Leakage Current FED Induction Motor Drive

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Abstract: The proposed modulation technique attains reduced common mode voltage with simplicity in implementation of the modulation technique. This work presents the comparison of various multicarrier based Pulse Width Modulation (PWM) techniques for the chosen single phase CMLI (Cascaded Multi Level Inverter). Multilevel inverters are a source of high power, often used in industrial applications and can use either sine or modified sine waves. A multilevel inverter uses a series of semiconductor power converters (usually two to three) thus generating higher voltage. Reverse leakage current in a semiconductor device is the current from that semiconductor device when the device is reversing biased. In earlier method transformer is used for generating multilevel output and grid synchronization. Transformer increases the leakage current. Now transformer less method and sine modulation techniques are presented to reduce the leakage current. It has been illustrated that the proposed modulation technique has less leakage current as compared to the two and three-level inverters. The proposed concept can be implemented to PV based MLI to reduced leakage current fed IM drive using MATLAB/SIMULINK software.

***Index Terms*—Cascaded H-bridge multilevel inverter, hybrid multicarrier pulse width modulation (H-MCPWM), leakage current reduction, transformer less photovoltaic (PV) system.**

I. INTRODUCTION

THE total power generation from the photovoltaic (PV) sys-tem is relatively small as compared to other common en-ergy resources due to its high installation cost. Reducing the PV system cost and increasing its efficiency have attained greater research interest. One of the solutions to reduce the cost of the PV power system is to remove transformer required in the output of the PV inverter [1]. Most of the national electricity regulatory authority made it compulsory to use trans-former above certain threshold power in the system because it ensures galvanic isolation. However, the use of transform-less increases weight, size, and cost of the PV system and radices the power conversion efficiency. This has motivated the research community to work in the transformer less PV system. The advancement of power electronics technology has made the use of transformer less PV inverter popular in kilo watt (kW) range by imposing standards such as DIN VDE 0126-1-1 [4]. However removal of the transformer introduces harmful leakage current to flow through the parasitic capacitance which exists between the PV module and the ground. This leakage current may increase the system losses, total harmonic distortion in the grid current, electromagnetic inferences, and safety concerns [6]. The factors used to limit magnitude of the common mode voltage include nature of the output pulse width of the inverter, number of commutation, and grounding of the PV system [10].

The commercial transformer less centralized PV inverter has been successfully connected in roof-top projects with ratings above 10 MW and it is recognized by IEEE 1547 and other standards. This encourages the possibility to use transformer-less inverter topology for high-power applications [13]. Next-generation PV inverter has reached higher power ratings with modularity, and redundant topologies will be adopted in the design for reliability of the inverter. Traditional two- and three-level inverters are unable to provide high efficiency and grid code requirements for higher power and voltage ratings; there-fore, converter topologies for medium-voltage and megawatt-scale PV inverters are moving toward the multilevel structures. Among various multilevel inverters, cascaded H-bridge multi-level inverter has various advantages compared to other topologies [14]. This use of cascaded H-bridge multilevel inverter opens up the option to eliminate the transformer from the PV system. In general, following two well-established modulation techniques are available for the multilevel inverter topologies which provide constant common mode voltage: space vector modulation (SVM) and multicarrier pulse width modulation (MCPWM). The SVM technique is more constructive from the view of switching timings. The switching sequence and modulation can be decided by the users, but it requires regress effort for implementation [15]. In, the author has demonstrated the use of SVM to reduce the leakage current in transformer-less PV inverter topology by placing zero active vectors at appropriate switching instants. However, selection of switching states is not easy for practical implementation. The MCPWM technique eliminates the problem of common mode

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voltage applied in the neutral clamped multilevel inverter, which in-creases the computational burden due to more number of carrier signals In, the authors have reported the effect of common mode voltage using bipolar and unipolar modulation schemes on the neutral point clamped multilevel inverter and cascaded H-bridge multilevel inverter. As the level of cascaded H-bridge multilevel inverter increases, it is expected to get reduction in leakage current, and further studies are required to know the relation

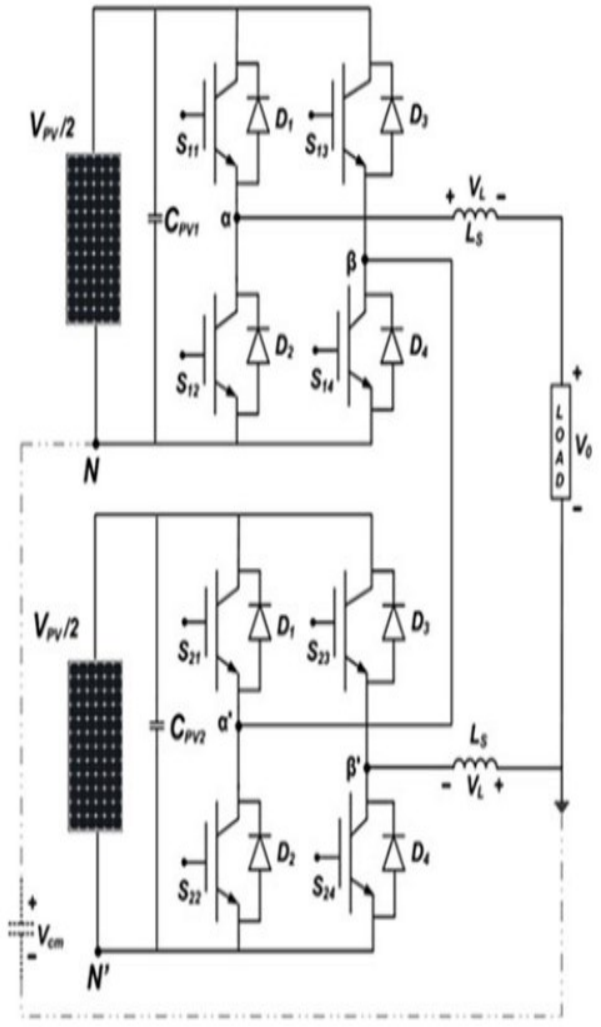

Fig. 1. PV-supported transformer less single-phase five-level cascaded multi-level inverter.

Between the modulation strategy and the leakage current. The cascaded H-bridge multilevel inverter has the advantages of less leakage current as compared to the conventional single H-bridge inverter due to reduced value of dc-link voltage per bridge. The common multicarrier modulation techniques used in the transformer less cascaded H-bridge multilevel PV inverter topologies introduce common mode voltage.

This letter proposes a hybrid multicarrier pulse width modulation (H-MCPWM) technique to reduce leakage current in transformer less cascaded H-bridge multilevel inverter for PV systems. When the common mode voltage changes in a large step value, it induces high leakage current in the PV system through the parasitic capacitance between the PV module and the ground. The reduced voltage transition in the common mode voltage reduces the leakage current. It is easy to implement the proposed modulation technique without much complexity and require half the number of carriers as required in the conventional MCPWM techniques.

II. CASCADED MULTILEVEL INVERTER AND HYBRID MULTICARRIER MODULATION SCHEME FOR CONSTANT COMMON MODE VOLTAGE

Fig. 1 shows the PV-supported single-phase five-level cascaded H-bridge inverter topology, where two H-bridges are connected in cascade and provides a common output. The configuration of two cascaded H-bridges adds the output voltage of the upper and lower bridges to generate five-level stepped output voltage at the ac side, i.e., V_{PV}, $V_{PV}/2$, 0, $-V_{PV}/2$, and $-V_{PV}$. It is assumed that the grid does not contribute common mode voltage in the system [9]. The converter topology and modulation method have significant contribution in leakage current generation. Therefore, the transformer less cascaded multilevel inverter shown in Fig. 1 is connected to a simple resistive load for Evaluation of the proposed modulation technique. The leakage current is generated in the parasitic capacitance formed between the PV module and the ground, where common mode voltage is also induced at the same point as shown in Fig. 1. The common mode voltage of any electrical circuit is the mean value of voltage between the outputs and a common reference point.

The negative terminal of the dc bus, i.e., terminal N is called here as common reference point for upper H-bridge inverter. Similarly, for lower H-bridge inverter, $N-$ is the common reference point. The parasitic capacitance formed for the lower H-bridge and upper H-bridge is assumed to be the same, be-cause both the H-bridges are supplied from the similar rated PV modules [11]. The common mode voltage (CMV) and leakage current in the two H-bridges are also same; hence, the capaci-tive currents flow from point N to ground and $N-$ to ground is considered equal. The common mode voltage V_{cm} for the upper full-bridge (H-bridge) inverter is defined as follows

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[3]:

$$V_{\mathrm{cm}} = \frac{V_{\alpha N} + V_{\beta N}}{2} \quad (1)$$

where $V_{\alpha N}$ and $V_{\beta N}$ are the voltages between the mid-point of the upper H-bridge inverter legs to the negative terminal of the dc link, $V_{\alpha\_\beta\_}$ is the voltage between the mid points of the two legs of the lower H-bridge inverter, and let V_o is the output voltage across the load. The leakage current mainly depends upon the magnitude of the inverter common mode voltage. In order to derive the expression of the common mode voltage in the cascaded multilevel inverter, the following equations can be written from Fig. 1:

$$V_{\mathrm{cm}} + V_{\alpha N} - V_L - V_O = 0 \quad (2)$$

$$V_{\mathrm{cm}} + V_{\beta N} + V_L - V_{\alpha\_\beta\_} = 0. \quad (3)$$

The output voltage V_o has little effect on parasitic capacitance and hence it is neglected. It is assumed that the filter inductance L_s is considered the same in the two H-bridges for simplicity of the analysis and hence the voltage drop V_L due to the inductance L_s in the two H-bridges is also assumed equal [3]. The expression of the common mode voltage can be obtained in (4) by adding (2) and (3) as follows:

$$2V_{\mathrm{cm}} + V_{\beta N} + V_{\alpha N} - V_{\alpha\_\beta\_} = 0. \quad (4)$$

Using (4), the common mode voltage can be expressed as follows:

$$V_{\mathrm{cm}} = \frac{V_{\alpha\_\beta\_} - V_{\alpha N} - V_{\beta N}}{2}. \quad (5)$$

Now considering convention that the leakage current will flow from PV module to ground or vice versa as per the standards IEEE 80 [22], the sign of common mode voltage can be reversed as $V_{\mathrm{cm}'} = -V_{\mathrm{cm}}$ and abbreviated now onward as CMV in this paper. Equation (5) is useful for determining the common mode voltage in various intervals of the reference period.

To minimize the leakage current flow through the parasitic capacitance, the common mode voltage is required to be maintained minimum during the switching instances. The minimum step value of the common mode voltage is defined by $V_{\mathrm{PV}}/(n-1)$ in the MCPWM technique [18]. In phase

TABLE I
SWITCHING INSTANTS OF THE H-MCPWM TECHNIQUE FOR CONSTANT COMMON MODE VOLTAGE

Logic conditions	Switches on upper H-bridge				Switches on lower H-bridge				Common mode voltage
Mode-1: (0 to $T/2$)	S_{11}	S_{14}	S_{13}	S_{12}	S_{21}	S_{24}	S_{23}	S_{22}	V'_{cm}
$V_{c1} > V_{\mathrm{ref}} < V_{c2}$	1	1	0	0	0	0	1	1	$2V_{\mathrm{PV}}/4$
$V_{c1} > V_{\mathrm{ref}} > V_{c2}$	0	1	0	1	0	0	1	1	$V_{\mathrm{PV}}/4$
$V_{c1} < V_{\mathrm{ref}} > V_{c2}$	0	0	1	1	0	0	1	1	$2V_{\mathrm{PV}}/4$
Mode-2: ($T/2$ to T)	S_{11}	S_{14}	S_{13}	S_{12}	S_{21}	S_{24}	S_{23}	S_{22}	–
$V_{c2} > V_{\mathrm{ref}} < V_{c1}$	1	1	0	0	0	0	1	1	$2V_{\mathrm{PV}}/4$
$V_{c2} > V_{\mathrm{ref}} > V_{c1}$	1	1	0	0	1	0	1	0	$V_{\mathrm{PV}}/4$
$V_{c2} < V_{\mathrm{ref}} > V_{c1}$	1	1	0	0	1	1	0	0	0

disposition multicarrier pulse width modulation (PD-MCPWM), the common mode $V_{\mathrm{cm}'}$ varies in the band range of $\pm V_{\mathrm{PV}}/2$. However, in this modulation method, total $(n-1)$ number of carrier signals are used, where n is the inverter level. The proposed H-MCPWM is the modified version of the phase opposite disposition (POD) pulse width modulation technique, where the number of carriers required is half of that required in POD PWM and therefore computational burden is reduced. In this modulation method, the carrier signals used are in-phase with each other. The phase of all the carriers is shifted by 180° after each half-cycle. Table I shows the different switching in-stants and their corresponding magnitude of CMV. It has six switching instants, in which one instant has zero CMV, three in-stants have $2V_{\mathrm{PV}}/4$, and two instants have $V_{\mathrm{PV}}/4$, CMV. There is no voltage transition in zero CMV. The CMV may take the values depending upon the inverter switch states selected since the voltage-source inverter cannot provide pure sinusoidal volt-ages and has discrete output voltage levels synthesized from the output voltage of the PV [10], [23]. The voltage transition depends upon the direction of the current in the inverter; hence, the proposed H-MCPWM modulation technique ensures the re-duced common mode voltage generation in the band limit of maximum $\pm V_{\mathrm{PV}}/4$. The switching pattern of the proposed H-MCPWM technique for five-level cascaded multilevel inverter is illustrated in Fig. 2. The operation of the proposed H-MCPWM is divided into two modes of operation, i.e., mode-1 and mode-2, as explained next

A. Mode-1 (0 to T/2)

In this mode, all the carrier signals are in-phase with each other, the three-level voltages, i.e., 0, $-V_{\mathrm{PV}}/2$, and $-V_{\mathrm{PV}}$, are generated using following switching scheme:

1) When the reference signal V_{ref} is smaller than the

International Journal of Research
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p-ISSN: 2348-6848
e-ISSN: 2348-795X
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carrier signals V_{c1} and V_{c2}, then the switches S_{11}, S_{14}, S_{23}, and S_{22} are turned ON and the complimentary switches, S_{13}, S_{12}, S_{21}, and S_{24}, are turned OFF. In this situation $V_{\alpha N} = V_{PV}/2$, $V_{\beta N} = 0$, and the output voltage is $V_{\alpha\beta} = +V_{PV}/2$.

2) When the reference signal V_{ref} is greater the carrier sig-nal V_{c2}, and lesser than the carrier signal V_{c1}, then the switches S_{14}, S_{12}, S_{23}, and S_{22} are turned ON and the

complimentary switches S_{11}, S_{13}, S_{21}, and S_{24} are turned OFF. In this situation $V_{\alpha N} = 0$, $V_{\beta N} = 0$, and the output voltage is $V_{\alpha\beta} = 0$.

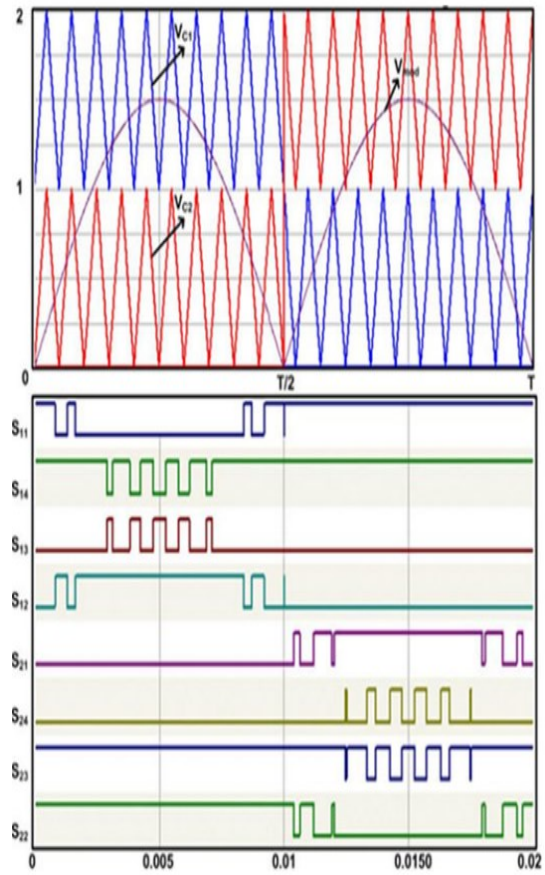

Fig. 2. Switching pattern of the proposed H-MCPWM technique for the fivelevel cascaded multilevel inverter.

3) When both the carrier signals, V_{c1} and V_{c2}, are smaller than the reference signal V_{ref}, then the switches, S_{13}, S_{12}, S_{23}, and S_{22}, are turned ON and the complimentary

switches, S_{11}, S_{14}, S_{21}, and S_{24}, are turned OFF. In this situation $V_{\alpha N} = 0$, $V_{\beta N} = V_{PV}/2$, and the output voltage is $V_{\alpha\beta} = -V_{PV}/2$.

In this mode, all the carrier signals are phase shifted by 180°, the three-level voltages, i.e., 0, $+V_{PV}/2$, and $+V_{PV}$, are generated using following switching scheme.

1) When the reference signal V_{ref} is smaller than the carrier signals V_{c1} and V_{c2}, then the switches, S_{11}, S_{14}, S_{23}, and S_{22}, are turned ON and the complimentary switches,

S_{13}, S_{12}, S_{21}, and S_{24}, are turned OFF. In this situation $V_{\alpha\_N\_} = 0$, $V_{\beta\_N\_} = +V_{PV}/2$, and the output voltage is $V_{\alpha\_\beta\_} = -V_{PV}/2$. When the reference signal V_{ref} is greater the carrier sig-nals V_{c1}, and lesser than the carrier signal V_{c2}, then the switches, S_{11}, S_{14}, S_{21}, and S_{23}, are turned ON and the complimentary switches, S_{13}, S_{12}, S_{22}, and S_{24}, are turned OFF. In this situation $V_{\alpha\_N\_} = +V_{PV}/2$, $V_{\beta\_N\_} = +V_{PV}/2$, and the output voltage is $V_{\alpha\_\beta\_} = 0$.

3) When both the carrier signals, V_{c1} and V_{c2}, are smaller than the reference signal V_{ref}, then the switches, S_{11}, S_{14}, S_{21}, and S_{24}, are turned ON and the complimentary switches, S_{13}, S_{12}, S_{23}, and S_{22}, are turned OFF. In this situation $V_{\alpha\_N\_} = V_{PV}/2$, $V_{\beta\_N\_} = 0$, and the output voltage is $V_{\alpha\_\beta\_} = +V_{PV}/2$.

The summary of the switching instants employed in two modes of operation is presented in Table I. It is clearly visi-ble from the previous discussion that the proposed H-MCPWM technique is able to generate five-level inverter output voltage and attain reduced common mode voltage in the band of maxi-mum $\pm V_{PV}/4$, which is superior to the conventional MCPWM technique.

III. INDUCTION MOTOR

The induction motor speed variation can be easily achieved for a short range by either stator voltage control or rotor resistance control. But both of these schemes result in very low efficiencies at lower speeds. The most efficient scheme for speed control of induction motor is by varying supply frequency. This not only results in scheme with wide speed range but also improves the starting performance. Synchronous speed of Induction Motor is directly proportional to the supply frequency. Hence, by changing the frequency, the synchronous speed and the motor speed can be controlled below and above the normal full load speed. If the machine is operating at

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e-ISSN: 2348-795X
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speed below base speed, then v/f ratio is to be kept constant so that flux remains constant. This retains the torque capability of the machine at the same value. But at lower frequencies, the torque capability decrease and this drop in torque has to be compensated for increasing the applied voltage. Any reduction in the supply frequency without a change in the terminal voltage causes an increase in the air gap flux. Induction motors are designed to operate at the knee point of the magnetization characteristic to make full use of the magnetic material. Therefore the increase in flux will saturate the motor. This will increase the magnetizing current, distort the line current and voltage, increase the core loss and the stator copper loss, and produce a high pitch acoustic noise. While any increase in flux beyond rated value is undesirable from the consideration of saturation effects, a decrease in flux is also avoided to retain the torque capability of the motor. Therefore, the variable frequency control below the rated frequency is generally carried out by reducing the machine phase voltage, V, along with the frequency in such a manner that the flux is maintained constant. Above the rated frequency, the motor is operated at a constant voltage because of the limitation imposed by stator insulation or by supply voltage limitations.

IV MATLAB/SIMULATION RESULTS

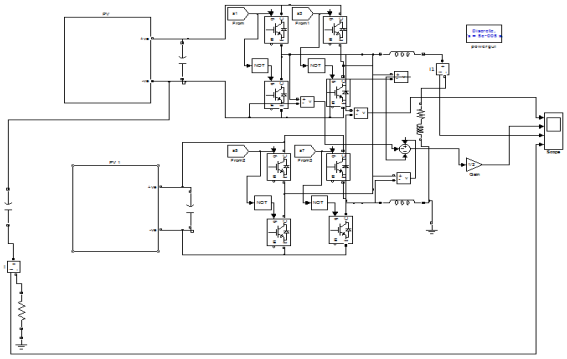

Fig 3 Matlab/simulation model of proposed converter with multi carrier modulation

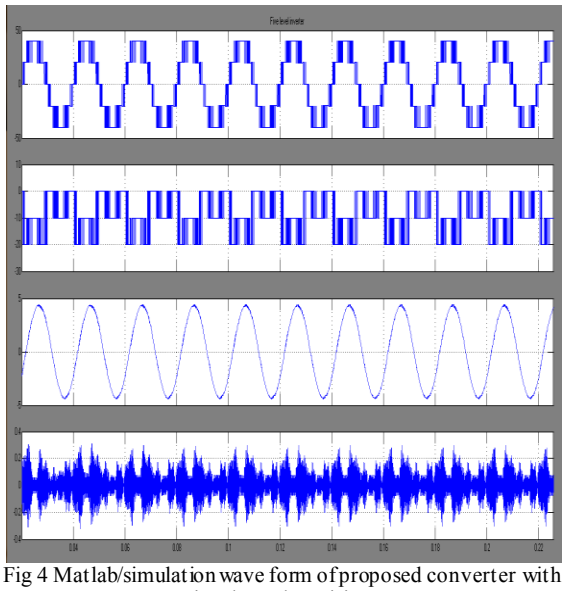

Fig 4 Matlab/simulation wave form of proposed converter with in-phase deposition

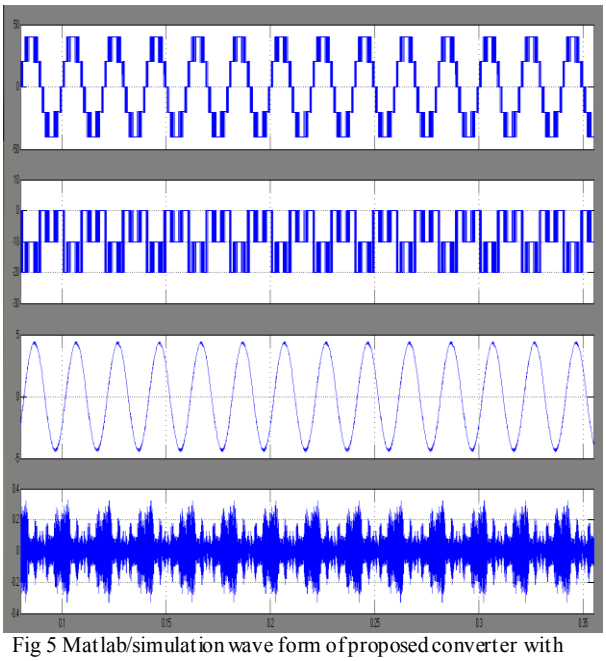

Fig 5 Matlab/simulation wave form of proposed converter with out -phase deposition

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Volume 03 Issue 10
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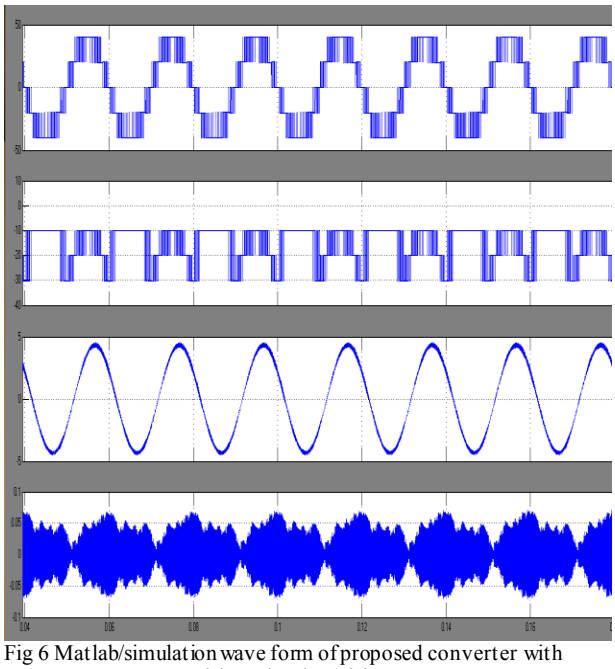

Fig 6 Matlab/simulation wave form of proposed converter with multi carrier deposition

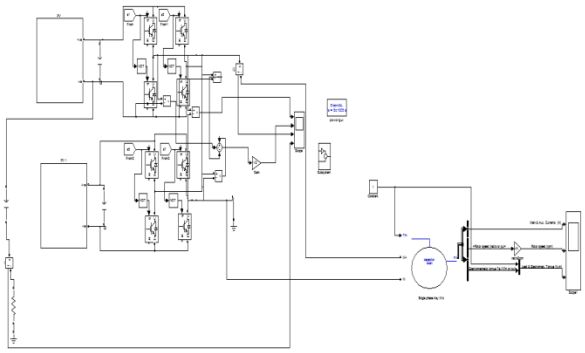

Fig 7 Matlab/simulation model of proposed converter with multi carrier modulation with Induction Motor drive

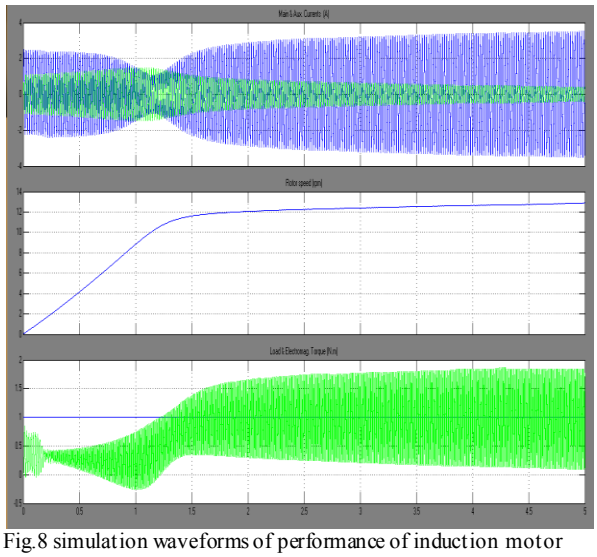

Fig.8 simulation waveforms of performance of induction motor

V CONCLUSION

In this project proposes H-MCPWM technique employed in transformer less cascaded multilevel inverter for the PV systems. The proposed modulation technique attains reduced common mode voltage with simplicity in implementation of the modulation technique. It has been illustrated that the proposed modulation technique has less leakage current as compared to the two-and three-level inverters. It is also observed that the proposed H-MCPWM offers less total harmonic distortion as compared to the conventional modulation methods. It uses only two carrier signals to generate the five-level inverter output which otherwise is four in other multicarrier modulation techniques, and to reduced ripple carrier current and also to study the Induction motor characteristics.

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