

A Novel Multifunctional Distributed Compensation Scheme for Stiff Source connected Induction motors

Singireddi.Umamaheswara Rao

M-tech Student Scholar

Department of Electrical & Electronics Engineering,
Sri Venkateswara College of Engg & Tech,
Etcherla; Srikakulam (Dt); A.P, India.

Abstract-This paper presents a control scheme for Static Compensators applied in distribution systems (DSTATCOM), that are used for regulation of voltage magnitude at point of common coupling (PCC) and it also has the function of eliminating harmonics of voltage through PCC-voltage-detection method. Voltage-magnitude regulation is accomplished through quadrature-current injection at PCC and harmonic mitigation is released reading the voltage at PCC and producing harmonic currents capable of voltage-distortion compensation at PCC. Using this method there is not necessity of source or load current measurement. The voltage regulator was implemented using a four-wire three-phase shunt-connected VSI. If it operates in a voltage control mode, it can make the voltage of the bus to which it is connected a balanced sinusoid, irrespective of the unbalance and distortion in voltage in the supply side or line current. Similarly when operated in a current control mode, it can force the source side currents to become balanced sinusoids. Loads connected to a stiff source cannot be protected from voltage disturbances using a distribution static compensator (DSTATCOM). In this paper, a new control algorithm based multifunctional DSTATCOM is proposed to operate in voltage control mode under stiff source. This scheme provides fast voltage regulation at the load terminal during voltage disturbances and protects induction machine drive system. The simulation results are obtained using MATLAB/SIMULINK software.

Index Terms—DSTATCOM, multifunctional, stiff source, power factor, voltage regulation, induction machine drive system.

I. INTRODUCTION

The rapidly developing power electronic technology provides an opportunity for developing new power equipment for improving the performance of the power system. Flexible AC Transmission System technology (FACTS) uses the latest power electronic devices and methods to control electronically the high-voltage side of the network [1]. FACTS devices can be used for power flow control, voltage regulation, transient stability improvement, and damping of power oscillations. FACTS devices can be of shunt series or combination of shunt and series types [2]. The shunt devices can be used for voltage regulations, while series devices can be used for regulation of line impedance and series-parallel combination can be used

Jallu Hareesh Kumar

Assistant Professor

Department of Electrical & Electronics Engineering,
Sri Venkateswara College of Engg & Tech
Etcherla; Srikakulam (Dt); A.P, India.

for real and reactive power compensation in addition to regulation of voltage and regulation of line impedance [3]. The load compensation using state feedback control of DSTATCOM with shunt filter capacitor gives better results [4]. The switching frequency components in the terminal voltages and source currents are eliminated by using state feedback control of shunt filter capacitor. In this situation, DSTATCOM should operate in CCM [5]. However, due to grid faults, source voltage (stiff or non-stiff) can change at any time and then VCM operation is required. DSTATCOM regulates the load voltage by indirectly regulating the voltage across the feeder impedance. When a load is connected to nearly a stiff source, feeder impedance will be negligible [6]–[8]. Under these circumstances, DSTATCOM cannot provide sufficient voltage regulation at the load terminal [9].

This paper proposes a new control algorithm based DSTATCOM topology for voltage regulation even under stiff source. It is achieved by connecting a suitable external inductor in series between the load and the source point. Point of common coupling (PCC) will be the point where external inductor and source are connected. DSTATCOM, connected at the load terminal, provides voltage regulation by indirectly regulating the voltage across the external inductor [10]. Proposed control algorithm to obtain variable reference load voltage is formulated as a function of the desired source current [11]. This voltage indirectly controls the current drawn from the source for a permissible range of source voltage. Therefore, the control algorithm makes source currents balanced, sinusoidal, and in phase with respective source voltages during normal operation. During voltage disturbances, a constant voltage is maintained at the load terminal. Hence, proposed topology and control algorithm make compensator multifunctional so that it provides fast voltage regulation at load terminal and additionally provides advantages of CCM while operating in VCM [12].

II. BASIC MODEL OF D-STATCOM

The D-STATCOM system comprises of a VSC, a set of coupling reactors (leakage reactance of the transformer) and a controller. The DSTATCOM generates a controllable ac voltage from the Voltage Source Inverter (VSI) connected to a dc capacitor (energy storage device).

The ac voltage appears behind the transformer leakage reactance. The active and reactive power transfer between the power system and the DSTATCOM is caused by the voltage difference across this reactance. The D-STATCOM is connected to the power network at the Point of Common Coupling (PCC), where the voltage-quality problem is a concern. All required voltages and currents are measured and are fed into the controller to be compared with the reference. The controller then performs feedback control and outputs a set of switching signals to drive the main semiconductor switches (IGBTs) of the power converter accordingly (Introducing Custom Power, 1995). The basic diagram of the D-STATCOM is illustrated in Figure 1.

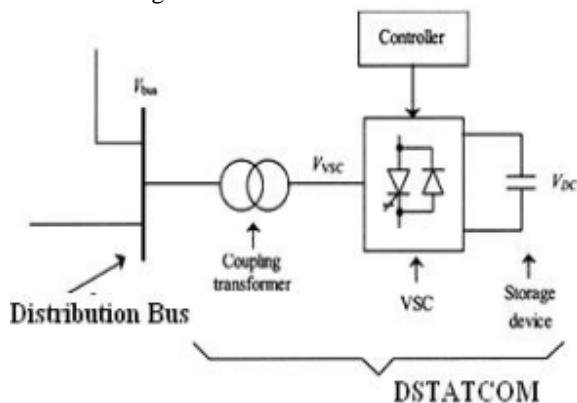


Figure.1. Basic Block Diagram of D-STATCOM.

III. DSTATCOM CONFIGURATION

A neutral point clamped voltage source inverter (VSI) topology is chosen as it provides independent control of each leg of the VSI [7]. A single phase equivalent circuit of DSTATCOM in distribution network is shown in Fig. 2. VSI represented by u V dc is connected to load terminal through an LC filter ($L_f - C_{fc}$).

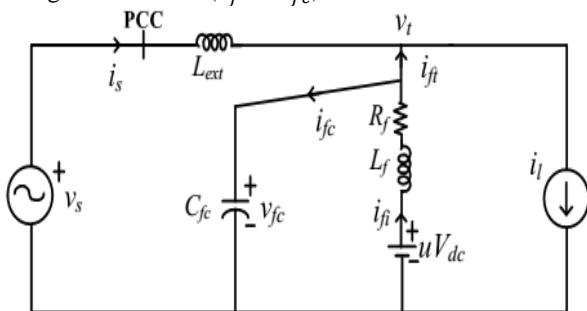


Fig.2.Single phase equivalent circuit of DSTATCOM in distribution network.

The load terminal is connected to the PCC through an external series inductance L_{ext} . V_{dc} is the voltage maintained across the each dc capacitor and 'u' is a control variable which can be +1 or -1 depending upon switching state. If i , i_t , and i_c are currents through VSI,

DSTATCOM and C_{fc} respectively. V_s and V_t are source and load voltages respectively. Loads have both linear and nonlinear elements with balanced or unbalanced features. Load and source currents are represented by I_l and i_s respectively.

IV. SELECTION OF EXTERNAL INDUCTOR

Under normal operation, external impedance (Z_{ext}) does not have much importance, whereas it plays a critical role during voltage disturbances. The value of external impedance is decided by the rating of the DSTATCOM and amount of sag to be mitigated. At any time, the source current in any phase by assuming balanced source voltage is given as

$$\bar{I}_s = \frac{V_s \angle 0 - V_t \angle -\delta}{R_{ext} + jX_{ext}} \quad (1)$$

Where, V_s , V_t , R_{ext} , X_{ext} , and δ are rms source voltage, rms load voltage, external resistance, external reactance, and load angle respectively. For most practical case $X_{ext} \gg R_{ext}$. As a worst case design the reactive source current ($I_m [I_s]$) which is supplied by the compensator, will be maximum when δ is minimum. For this, source current will supply only losses in the VSI. Therefore, it will be very small. Hence, $I_m [I_s]$ is given as

$$I_m [I_s] = \frac{V_t - V_s}{X_{ext}} \quad (2)$$

During voltage disturbances, the aim is to protect the sensitive loads with focus is on to improve the DSTATCOM capability to mitigate deep sag. Therefore, keeping it into account, the load voltage during voltage sag is taken as 0.9 p.u (per unit) which is sufficient to protect the load. Assuming that the reactive current that a compensator can inject is 20 A and load needs to be protected from sag of 40%, then the value of external reactance is found to be

$$X_{ext} = \frac{0.9 - 0.6}{20} \times 230 = 3.45 \Omega \quad (3)$$

External reactance of 3.45 that corresponds to an inductance of 11 mH for a 50 Hz supply is used.

V. PROPOSED CONTROL ALGORITHM

Proposed control algorithm aims to provide fast voltage regulation at the load terminal during voltage disturbances while retaining the advantages of CCM during normal operation. Firstly, currents that must be drawn from the source together with advantages of CCM are computed. Using these currents, magnitude of voltages that need to be maintained at load terminal is computed. If this voltage magnitude lies within a permissible range then same voltage is used as reference voltage to provide advantages of CCM. If voltage lies outside the permissible range, it is a sign of voltage disturbance and a fixed voltage magnitude is selected as reference voltage. A two loop controller, whose output is load angle, is used

to extract load power and VSI losses from the source. Finally, a discrete model is derived to obtain switching pulses. All these steps are presented in detail in this section.

A. Computation of Reference Voltage Magnitude (V_t^*)

During normal operation, load voltage must be regulated in such a way that following advantages provided by CCM operation are achieved:

1. Source currents are balanced and sinusoidal.
2. Unity power factor (UPF) at PCC.
3. Source supply load average power and VSI losses.

To achieve all aforementioned objectives, instantaneous symmetrical component theory [15] is used to get reference source currents. DSTATCOM makes the load voltages balanced and sinusoidal, but still may contain some switching harmonics which will give unacceptable reference source currents when directly used. Therefore, positive sequence component of load voltages (v_{ta}^+ , v_{tb}^+ , and v_{tc}^+) are extracted and used to compute reference source currents (i_{sa}^* , i_{sb}^* , and i_{sc}^*) as follows:

$$\begin{aligned} i_{sa}^* &= \frac{v_{ta}^+}{\Delta_1^+} (P_{lavg} + P_{loss}) \\ i_{sb}^* &= \frac{v_{tb}^+}{\Delta_1^+} (P_{lavg} + P_{loss}) \\ i_{sc}^* &= \frac{v_{tc}^+}{\Delta_1^+} (P_{lavg} + P_{loss}) \end{aligned} \quad (4)$$

Where, $\Delta_1^+ = \sum_{j=a,b,c} (v_{tj1}^+)^2$, P_{lavg} is average load power and is calculated using a moving average filter (MAF). Total losses in the inverter, P_{loss} , computed using a PI controller, helps in maintaining averaged dc link voltage ($V_{dc1} + V_{dc2}$) at a predefined reference value ($2V_{dcref}$) by drawing a set of balanced currents from the source and is given as follows:

$$P_{loss} = K_{pdc} e + K_{idc} \int e dt \quad (5)$$

Where, K_{pdc} , K_{idc} , and $e = 2V_{dcref} - (V_{dc1} + V_{dc2})$ are proportional gain, integral gain, and voltage error of the PI controller respectively. The reference currents to be drawn from the source are computed using (4), reference voltages at the load terminal can be derived. Applying KVL in the circuit shown in Fig.3.

$$\vec{V} = \vec{I}_s Z_{ext} + \vec{V}_t \quad (6)$$

Source voltage and source current will be in phase for the UPF operation. Also, source voltage is taken as reference. Therefore

$$V_s = I_s (R_{ext} + j X_{ext}) + V_t \angle -\delta$$

From the above equation, the load voltage can be computed as follows:

$$V_t = \sqrt{(V_s - I_s R_{ext})^2 + (I_s X_{ext})^2} \quad (7)$$

Based on standards, load voltage has a permissible range of variations between 0.9 to 1.1 p.u. Therefore, as long as V_t , obtained using (7) lies between 0.9 to 1.1 p.u, is

used as reference load voltage (V_t^*) and the advantages of CCM operation are achieved. Here, V_t is indirectly controlled by the desired source current. During sag and swell, the load voltage magnitude will be between 0.9 to 1.1 p.u and 1.1 to 1.8 p.u respectively for half cycle to 1 minute [16]. Therefore, reference load voltage magnitudes are set to 0.9 p.u and 1.1 p.u during sag and swell respectively. The reason to keep load voltages at these values is to maximize the DSTATCOM disturbance withstanding ability while keeping load voltage at the safe limits for satisfactory operation. Therefore, following conclusions can be drawn:

$$\begin{aligned} \text{If } 0.9 \text{ pu} \leq V_t \leq 1.1 \text{ pu} &\text{ then } V_t^* = V_t \\ \text{Else If } V_t > 1.10 \text{ pu} &\text{ then } V_t^* = 1.1 \text{ pu} \\ \text{else if } V_t < 0.9 \text{ pu} &\text{ then } V_t^* = 0.9 \text{ pu} \end{aligned} \quad (8)$$

B. Computation of Load Angle (δ)

The block diagram of controller to compute load angle is shown in Fig.3. It ensures that the load average power and losses in the VSI are supplied by the source [7]. Alternately, P_{loss} responsible for maintaining dc link voltage must be equal to shunt link power P_{sh} . Comparing P_{loss} and P_{sh} , an error is generated which is passed through a PI controller to compute δ as follows:

$$\delta = K_{pa} (P_{loss} - P_{sh}) + K_{ia} \int (P_{loss} - P_{sh}) dt \quad (9)$$

Where, K_{pa} and K_{ia} are proportional and integral gains of the inner PI controller respectively. The value of shunt link power, P_{sh} , is computed using a MAF as follows:

$$P_{sh} = \frac{1}{T} \int_{t_1}^{t_1+T} (V_{ta} i_{fta} + v_{tb} i_{ftb} + v_{tc} i_{ftc}) dt \quad (10)$$

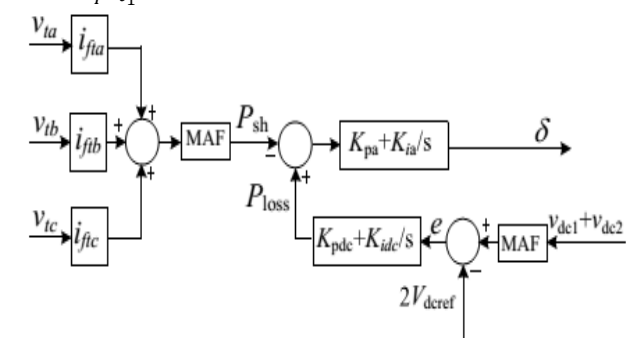


Fig.3: Controller to calculate δ and P_{loss} .

A positive value of P_{sh} means power flow from DSTATCOM to load terminal, whereas negative value of P_{sh} represents power flow from load terminal to DSTATCOM. In steady state, VSI losses are compensated by taking power from the source. Hence, P_{sh} will be negative in steady state. Moreover, capacitor voltage decreases from its reference voltage in steady state. Deviation of capacitor voltage from reference voltage represents losses in the VSI. Hence, P_{loss} will be negative

during steady state. Therefore, at all time, P_{sh} and P_{loss} should be equal. Hence, difference of P_{sh} and P_{loss} should be minimized. Output of inner PI controller, shown in Fig. 3, is delta which ensures that shunt link power P_{sh} drawn from source equals to losses in the capacitor P_{loss} .

C. Generation of Instantaneous Reference Voltage

By knowing the zero crossing of phase-a source voltage, selecting suitable reference load voltage magnitude from (8) and computing load angle from (9) the three phase reference voltages are given as follows:

$$\begin{aligned} v_{trefa} &= \sqrt{2}V_t^* \sin(\omega t - \delta) \\ v_{trefb} &= \sqrt{2}V_t^* \sin(\omega t - \frac{2\pi}{3} - \delta) \\ v_{trefc} &= \sqrt{2}V_t^* \sin(\omega t + \frac{2\pi}{3} - \delta) \end{aligned} \quad (11)$$

Where, ω is the frequency.

D. Generation of Switching Pulses

Each phase of the VSI can be controlled independently and hence, a discrete model of single phase has been derived to generate switching pulses. Dynamics of filter inductor and capacitor can be presented by following equations:

$$\begin{aligned} \frac{dv_{fc}}{dt} &= \frac{1}{c_{fc}} i_{fi} - \frac{1}{c_{fc}} i_{ft} \\ \frac{di_{fi}}{dt} &= -\frac{1}{l_f} v_{fc} - \frac{R_f}{l_{fi}} + \frac{v_{dc}}{l_f} u. \end{aligned} \quad (12)$$

Matrix representation of (12) is given as follows:

$$\dot{x} = Ax + Bz \quad (13)$$

$$A = \begin{bmatrix} 0 & \frac{1}{c_{fc}} \\ -\frac{1}{l_f} & -\frac{R_f}{l_{fi}} \end{bmatrix}, B = \begin{bmatrix} 0 & -\frac{1}{c_{fc}} \\ \frac{v_{dc}}{l_f} & 0 \end{bmatrix}$$

$$x = [v_{fc} \ i_{fi}]^t, \quad z = [u \ i_{ft}]^t.$$

Where, (13), given in continuous form, can be represented in discrete time form as follows:

$$x(k+1) = Gx(k) + Hz(k) \quad (14)$$

Where, matrix G and H are given as

$$G = \begin{bmatrix} G_{11} & G_{12} \\ G_{21} & G_{22} \end{bmatrix}, \quad H = \begin{bmatrix} H_{11} & H_{12} \\ H_{21} & H_{22} \end{bmatrix}$$

From (14) capacitor voltage will be

$$v_{fc}(k+1) = G_{11}v_{fc}(k) + G_{12}i_{fi}(k) + H_{11}u_k + H_{12}i_{ft}(k). \quad (15)$$

The reference voltage, V_{tref} , is maintained at the load terminal. A cost function, J, is chosen as

$$J = [v_{tref}(k+1) - v_{fc}(k+1)]^2 \quad (16)$$

Cost function is

$$v_{fc}(k+1) = v_{tref}(k+1) \quad (17)$$

Finally, reference discrete voltage control law from (15) and (17) is given as

$$u^*(k) = \frac{v_{tref}(k+1) - G_{11}v_{fc}(k) - G_{12}i_{fi}(k) - H_{12}i_{ft}(k)}{H_{11}} \quad (18)$$

$U^*(k)$ is regulated around a hysteresis band h to generate switching pulses of VSI using hysteresis control.

VI. INDUCTION MOTOR

An induction motor is an example of asynchronous AC machine, which consists of a stator and a rotor. This motor is widely used because of its strong features and reasonable cost. A sinusoidal voltage is applied to the stator, in the induction motor, which results in an induced electromagnetic field. A current in the rotor is induced due to this field, which creates another field that tries to align with the stator field, causing the rotor to spin. A slip is created between these fields, when a load is applied to the motor. Compared to the synchronous speed, the rotor speed decreases, at higher slip values. The frequency of the stator voltage controls the synchronous speed. The frequency of the voltage is applied to the stator through power electronic devices, which allows the control of the speed of the motor. The research is using techniques, which implement a constant voltage to frequency ratio. Finally, the torque begins to fall when the motor reaches the synchronous speed. Thus, induction motor synchronous speed is defined by following equation,

$$n_s = \frac{120f}{p} \quad (19)$$

Where f is the frequency of AC supply, n , is the speed of rotor; p is the number of poles per phase of the motor. By varying the frequency of control circuit through AC supply, the rotor speed will change.

A. Control Strategy of Induction Motor

Power electronics interface such as three-phase SPWM inverter using constant closed loop Volts/Hz control scheme is used to control the motor. According to the desired output speed, the amplitude and frequency of the reference (sinusoidal) signals will change. In order to maintain constant magnetic flux in the motor, the ratio of the voltage amplitude to voltage frequency will be kept constant. Hence a closed loop Proportional Integral (PI) controller is implemented to regulate the motor speed to the desired set point. The closed loop speed control is characterized by the measurement of the actual motor speed, which is compared to the reference speed while the error signal is generated. The magnitude and polarity of the error signal correspond to the difference between the actual and required speed. The PI controller generates the

corrected motor stator frequency to compensate for the error, based on the speed error.

VII.MATLAB/SIMULINK RESULTS

Here simulation is carried out in several cases, in that 1) Proposed DSTATCOM Topology for PQ Improvement Features. 2) Proposed DSTATCOM Topology Applied to Induction Machine Drive.

Case 1: Proposed DSTATCOM Topology for PQ Improvement Features

Proposed Novel Multifunctional Distributed Compensation Scheme can mitigate several power quality (PQ) problems. In current control mode (CCM), it injects harmonic and reactive components of load currents to make source currents balanced, sinusoidal, and in phase with load voltages. In voltage control mode (VCM), it regulates load voltage at a constant value to protect sensitive loads from voltage disturbances such as sags, swells, transients, and/or fluctuations. However, the objectives of these two modes are different and it can be Achieved by proposed DSTATCOM.

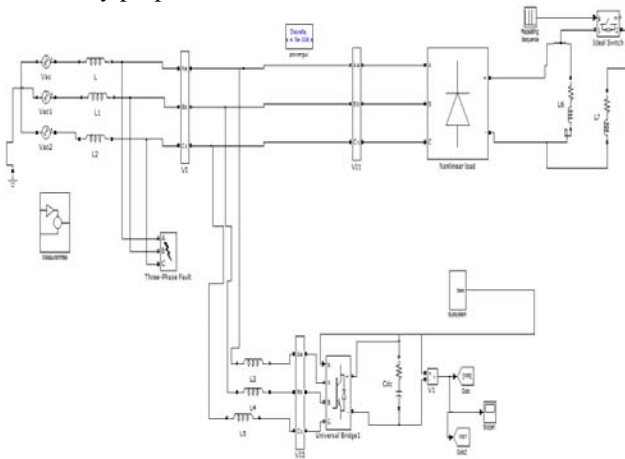


Fig.4 Mat lab/Simulink Model of Proposed DSTATCOM Topology for PQ Improvement Features.

Figure.4. gives the Simulation model of system with M-DSTATCOM. In a distribution system with a non-linear load connected to the system will generates harmonics. A nonlinear load in a power system is characterized by the introduction of a switching action and consequently current interruptions. This behavior provides current with different components that are multiples of the fundamental frequency of the system. These components are called harmonics. The amplitude and phase angle of a harmonic is dependent on the circuit and on the load it drives.

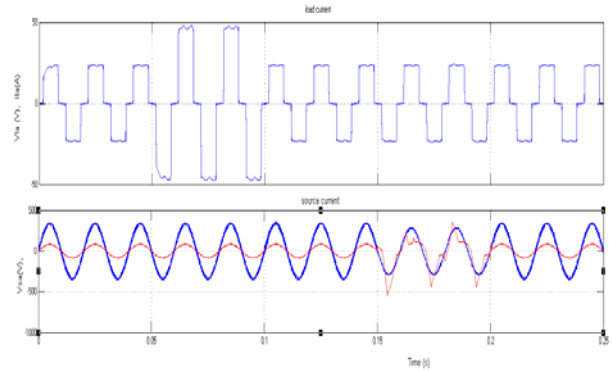


Fig.5. Phase-a waveforms before, during, and after load change. (a) Load current. (b) Source voltage and source current of Proposed DSTATCOM Topology with stiff source.

Initially, a three phase and non-linear load is connected. For achieved multifunctional DSTATCOM operation there phase fault is connected at source side. And at load side an ideal switch breaker is connected. Which is closed at $t = 0.05$ s. Then load is increased but source currents are balanced and sinusoidal and CCM mode is achieved. It can be seen that both voltage and currents are in phase with each other, maintain unity power factor. Increased load current will not effect on source performance and vice versa. It showed in phase-a, is shown in fig.5 (a).

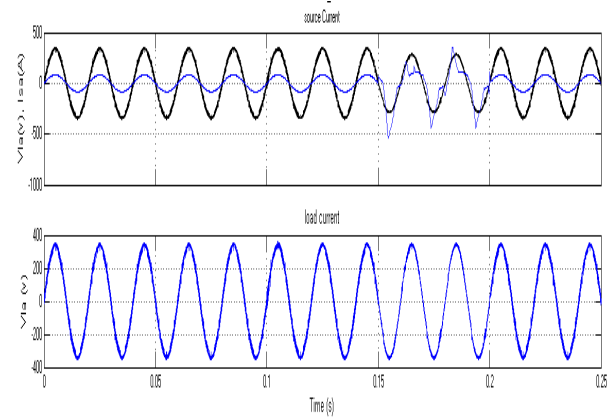


Fig.6.Phase-a: waveforms before, during, and after sag. (a) Source voltage and source current. (b) Load voltage of Proposed DSTATCOM Topology with stiff source.

At $t = 0.15$ s, fault is created by three phase fault at source side. But a fast voltage regulation is provided at load side. It can be seen in fig.6, here voltage control mode is performed.

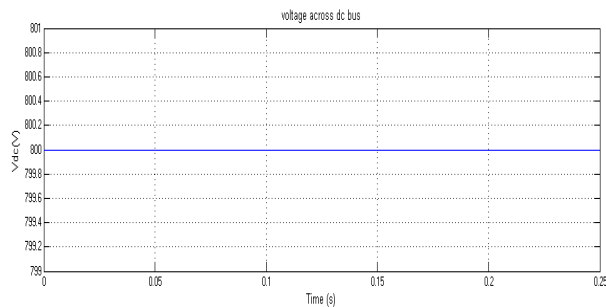


Fig.7 voltage across dc bus

Fig.7: shows the load angle shows the voltage at dc bus which is regulated around 800 V during entire operation.

Case 2: Proposed DSTATCOM Topology Applied to Induction Machine Drive

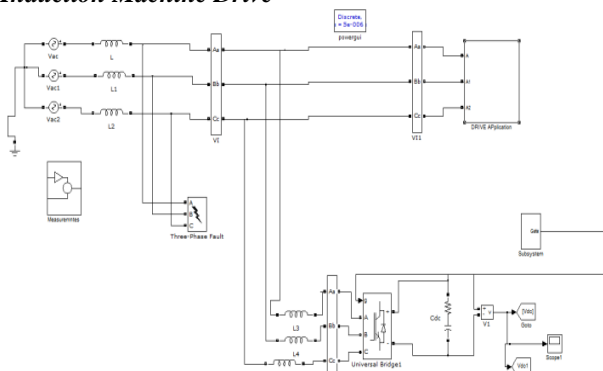


Fig.8. Matlab/Simulink Model of Proposed DSTATCOM Topology for PQ Improvement Features with Induction Machine Drive Application. Recently, developments in power electronics and semiconductor technology have lead improvements in power electronic systems. Pulse Width Modulation variable speed drives are increasingly applied in many new industrial applications that require superior performance for controlling the power flow for this industrial application requires Facts device, which is operated under distribution system is nothing but distributed compensation scheme.

A DSTATCOM is capable of compensating either bus voltage or line current. If it operates in a voltage control mode, it can make the voltage of the bus to which it is connected a balanced sinusoid, irrespective of the unbalance and distortion in voltage in the supply side or line current. Similarly when operated in a current control mode, it can force the source side currents to become balanced sinusoids.

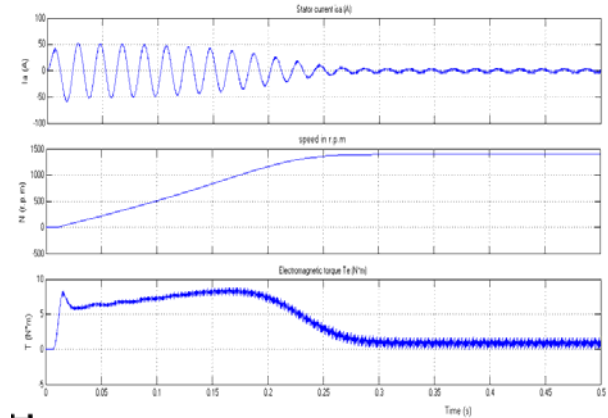


Fig.9. Armature Current, Speed, Electromagnetic Torque.

Fig.9.shows the Armature Current, Speed, and Electromagnetic Torque of Proposed DSTATCOM Topology for PQ Improvement Features with Induction Machine Drive Application.

VIII.CONCLUSIONS

In this paper we presented a control scheme for DSTATCOM current controlled that was used for voltage magnituderegulation at point of common coupling (PCC) through reactiveinjection, also it mitigates voltage harmonics throughPCC voltage detection. The proposed which has superior features over conventional topologies in terms of the required power switches and isolated dc supplies, control requirements, cost, and reliability with a new control algorithm based multifunctional DSTATCOM is proposed to protect the load from voltage disturbances under stiff source. It has been achieved by placing an external series inductance of suitable value between the source and the load. Moreover protects the Induction machine drive through DSTATCOM under power quality concerns with near to optimal features with efficient operation.

REFERENCES

- [1] Chandan Kumar and Mahesh K. Mishra, "A Multifunctional DSTATCOM Operating Under Stiff Source," IEEE Transactions on Industrial Electronics, vol.61, no.7, pp.3131-3136, July 2014".
- [2] A. Bhattacharya and C. Chakraborty, "A shunt active power filter with enhanced performance using ANN-based predictive and adaptive controllers," IEEE Trans., Ind. Electron., vol. 58, no. 2, pp. 421-428, Feb. 2011.
- [3] S. Rahmani, A. Hamadi, and K. Al-Haddad, "A Lyapunov-function based control for a three phase shunt hybrid active filter," IEEE Trans. Ind. Electron., vol. 59, no. 3, pp. 1418-1429, Mar. 2012.
- [4] Mahesh K. Mishra and K. Karthikeyan, "An investigation on design and switching dynamics of a voltage source inverter to compensate unbalanced and nonlinear loads," IEEE Trans. Ind. Electron., vol. 56, no. 8, pp. 2802-2810, Aug. 2009.
- [5] J. Liu, P. Zanchetta, M. Degano, and E. Lavopa, "Control design and implementation for high performance shunt active filters in aircraft power grids," IEEE Trans. Ind. Electron., vol. 59, no. 9, pp. 3604-3613, Sep. 2012.

- [6] A. Bhattacharya, C. Chakraborty, and S. Bhattacharya, "Parallel connected shunt hybrid active power filters operating at different switching frequencies for improved performance," *IEEE Trans. Ind. Electron.*, vol. 59, no. 11, pp. 4007–4019, Nov. 2012.
- [7] Q.-N. Trinh and H.-H. Lee, "An advanced current control strategy for three-phase shunt active power filters," *IEEE Trans. Ind. Electron.*, vol. 60, no. 12, pp. 5400–5410, Dec. 2013.
- [8] Mahesh K. Mishra, A. Ghosh, and A. Joshi, "Operation of a DSTATCOM in voltage control mode," *IEEE Trans. Power Del.*, vol. 18, no. 1, pp. 258–264, Jan. 2003.
- [9] H. Fujita and H. Akagi, "Voltage-regulation performance of a shunt active filter intended for installation on a power distribution system," *IEEE Trans. Power Electron.*, vol. 22, no. 3, pp. 1046–1053, May 2007.
- [10] R. Gupta, A. Ghosh, and A. Joshi, "Performance comparison of VSC based shunt and series compensators used for load voltage control in distribution systems," *IEEE Trans. Power Del.*, vol. 26, no. 1, pp. 268–278, Jan. 2011.
- [11] F. Gao and M. Iravani, "A control strategy for a distributed generation unit in grid-connected and autonomous modes of operation," *IEEE Trans., Power Del.*, vol. 23, no. 2, pp. 850–859, Apr. 2008.
- [12] Y.-R. Mohamed, "Mitigation of dynamic, unbalanced, and harmonic voltage disturbances using grid-connected inverters with LCL filter," *IEEE Trans. Ind. Electron.*, vol. 58, no. 9, pp. 3914–3924, Sep. 2011.



SINGIREDDI

UMAMHESWARARAO was born in 1991 month of July 10th. He received his B.Tech degree in Electrical and electronics Engineering from AkulaGopayya College of engineering & Technology in 2012. At present pursuing M.Tech specialization in Power electronics in Sri Venkateswara college of Engineering, Etcherla, Srikakulam district, Andhra Pradesh, India.



JALLU HAREESH KUMAR

Completed his graduation in Electrical and Electronics Engineering from Sarada Institute of Science, technology & Management. in the Year 2012 and received his M.Tech from Vignan's Institute of information & technology in 2015. He is presently working as Assistant Professor in Department of Electrical & Electronics Engineering in Sri Venkateswara College Of Engineering Etcherla, Srikakulam district, Andhra Pradesh, India. His areas of Interest are Power Electronics & Industrial Drives.