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Review of Adiabatic Logic Techniques

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ABSTRACT:

Now a day's every application need usage of portable devices such as mobiles, laptops etc., all these portable devices made up of electronic components such as resisters, capacitors, transistors. Portable device functionality depends on life time of the battery. Best solution of running portable devices for long time is 1) improve the capacity of the battery 2) Reduce the power consumption of the devices i.e: designing of the circuit by using low power consumption techniques. Here we deal with second issue, which is reduction of power consumption of the circuit being used. This can be achieved by the usage of adiabatic logic circuits. Most of the circuits are designed using CMOS logic which consumes less power, instead of that a new technology called adiabatic logic is used to get ultra low power consumption. This paper deals with all adiabatic logic techniques, power consumption of each technique is analyzed including CERL,PFAL,TSAL,SCRL,2PASCAL etc.,

I.INTRODUCTION:

In the recent day's use of portable devices becoming more and more proportionately increasing the demand for efficient utilization of battery power, as per the demand of transistors as the number of transistors increase in power consumption of electronic components has become very important in the design of IC's.

The main objective of this paper is to reduce the power consumption of electronic devices, there are several techniques used to reduce the power consumption, adiabatic technique is one of best technique among that, several researchers had tested power consumption using different types of adiabatic techniques which showed good results compared with conventional CMOS structure. In the conventional CMOS design output capacitor charging and switching of the circuits with rail-to-rail output voltage swing causes an energy transfer from supply to output node and output to ground which causes most of the power dissipation. To decrease the power dissipation the lost energy must be recycled to power supply. The technique which uses this property is called adiabatic technique.

Conventional switching

In conventional CMOS switching logic which uses the constant voltage source Vdd, the

switching event of circuits with rail-to-rail output voltage swing causes an energy transfer from the power supply to the output node or from the output node to the ground. During a 0-to-VDD transition of the output, the total output charge Q= *CL VDD* is drawn from the power supply at a Constant voltage. Thus, energy *E = CL VDD2* is drawn from the power supply during this transition. Charging the output node capacitance to the voltage level VDD means that at the end of the transition, the amount of stored energy in the output node is ***E = ½ CL VDD2.***Thus, half of the injected energy from the power supply is dissipated in the PMOS network while only one half is delivered to the output node. During a subsequent VDD-to-0 transition of the output node, no charge is drawn from the power supply and the energy stored in the load capacitance is dissipated in the NMOS network. To reduce the dissipation, the circuit designer can minimize the switching events, decrease the node capacitance, reduce the voltage swing, or apply a combination of these methods.

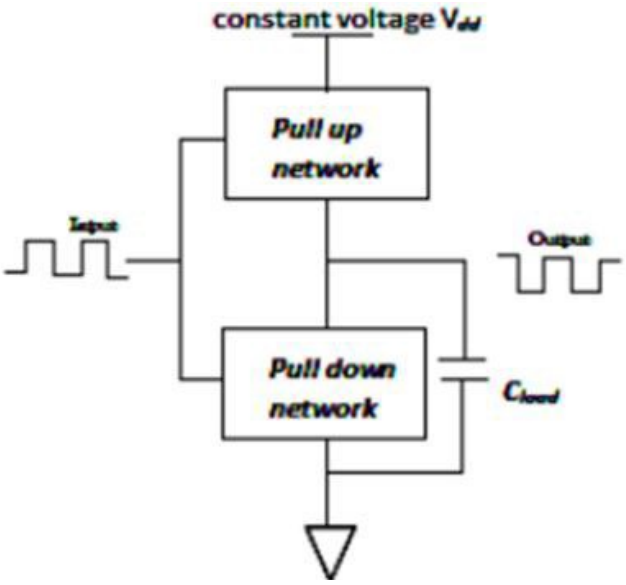

Fig1. Conventional CMOS charging and Discharging

Figure 1 shows the model of an adiabatic logic showing an ideal switch in series with resistance and two complementary voltage supply clocks. Constant voltage source is used in conventional CMOS logic to charge the load capacitance but in case of adiabatic logic switching circuits we use constant current source instead of constant voltage source. Figure3. Depicts clearly how this can be achieved with subsequent explanation. Constant current source is used,

i(t)=c dV/dt =c Vdd/T ------(1)

Energy during charging

E=(I2*R)*Tramp-------- (2)

The voltage across the switch = I*R

Q=CL*Vdd ,

I = (CL *Vdd)/Tramp

Eadiabatic=(I2*R)*Tramp--------- (3)

Therefore Eadiabatic=***R* C2 * Vdd2/Tramp*** ---------- (4)

Where,

E - Energy dissipated during charging time

Q - Charge transferred to the load

CL - the value of the load capacitance

R - on resistance of the PMOS switch

Vdd - the final value of the voltage at the load

Tramp - is the charging time

As explained above, the adiabatic switching power dissipation is asymptotically proportional to inverse of the charging time therefore, one can achieve very low energy dissipation [4] by slowing down the speed of operation and also the charge stored in the load capacitors can be recycled by using AC type power supply rather than DC.

The energy dissipated for adiabatic circuits is smaller if the charging time T is larger than 2RCL. Since, the dissipated energy is proportional to R thus reducing the on-resistance of the PMOS reduces the energy dissipation.

II.Adiabatic techniques:

Over the years various types of adiabatic logic techniques are proposed, complexity of the circuits also changes accordingly for the design by number of operation clock, single dual rail style, charging and discharging path etc. There are two types of adiabatic logic techniques one is partially adiabatic another one is fully adiabatic

A. Partially adiabatic logic:

It has simple architecture and power clock system, the adiabatic loss occurs when current flows through non-ideal switch, which is proportional to the frequency of the power clock. Popular partially adiabatic families include the following.

1. Efficient charge recovery logic (ECRL)
2. Positive feedback adiabatic logic (PFAL)
3. Clocked Adiabatic Logic (CAL)
4. NMOS energy recovery logic (NERL)
5. True single phase adiabatic logic (TSAL)
6. Source-coupled adiabatic logic (SCAL)
7. 2N- 2N2P adiabatic logic.

i)Efficient Charge Recovery Logic (ECRL):

Efficient Charge – Recovery Logic (ECRL) proposed by Moon and Jeong, shown in Figure 4.1, uses cross-coupled PMOS transistors. It has the structure similar to Cascode Voltage Switch Logic (CVSL) with differential signaling. It consists of two cross-coupled transistors *M1* and *M2* and two NMOS transistors in the An AC power supply *pwr* is used for ECRL gates, so as to recover and reuse the supplied energy. Both *out* and */out* are generated so that the power clock generator can always drive a constant load capacitance independent of the input signal. A more detailed description of ECRL can be found in. Full output swing is

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obtained because of the cross-coupled PMOS transistors in both precharge and recover phases. But due to the threshold voltage of the PMOS transistors, the circuits suffer from the non-adiabatic loss both in the precharge and recover phases. That is, to say, ECRL always pumps charge on the output with a full swing. However, as the voltage on the supply clock approaches to V_{dd} .So the recovery path to the supply clock to the supply clock is disconnected, thus, resulting in incomplete recovery. *Vtp* is the threshold voltage of PMOS transistor. The amount of loss is given as

$$\backslash EECRL = C|Vtp|2 / 2$$

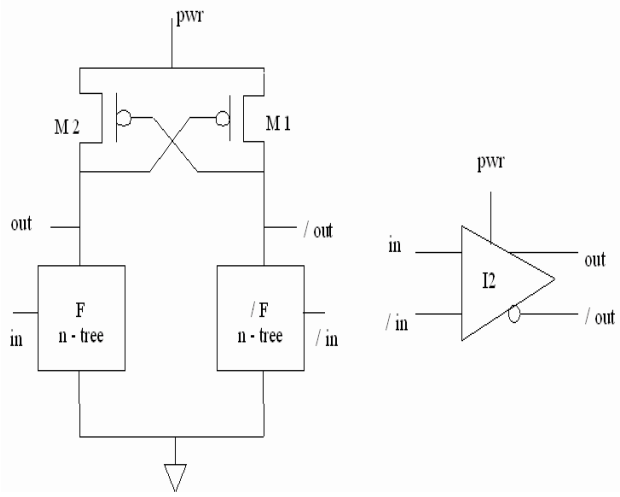

Figure2: The Basic Structure of the Adiabatic ECRL Logic.

ii) Positive Feedback Adiabatic Logic

The partial energy recovery circuit structure named Positive Feedback Adiabatic Logic (PFAL) has been used, since it shows the lowest energy consumption if compared to other similar families, and a good robustness against technological parameter variations. It is a dual-rail circuit with partial energy recovery. The general schematic of the PFAL gate is shown in Figure 4.3. The core of all the PFAL gates is an adiabatic amplifier, a latch made by the two PMOS *M1-M2* and two NMOS *M3-M4*, that avoids a logic level degradation on the output nodes *out* and */out*. The two n-trees realize the logic functions. This logic family also generates both positive and negative outputs. The functional blocks are in parallel with the PMOSFETs of the adiabatic amplifier and form a transmission gate. The two n-trees realize the logic functions. This logic family also generates both positive and negative outputs.

The latch in PFAL is made by two PMOSFET and two NMOSFET rather than by only two PMOSFETS as in ECRL logic and that the functional blocks are in parallel with the transmission PMOSFETs, this produces smaller equivalent resistance when capacitance need to be charged.

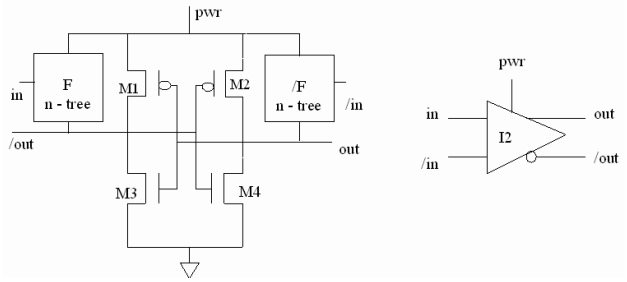

Figure3: The Basic Structure of PFA Logic.

i) iii) NMOS Energy Recovery Logic (NERL)

NMOS energy recovery logic (NERL) is one of

the quasi adiabatic logic technique, which uses NMOS transistors only and a simpler 6-phase clocked power. Its area overhead and energy consumption are smaller, compared with the other fully adiabatic logics. We employed bootstrapped NMOS switches to simplify the NERL circuits. With the simulation results for a full adder, we confirmed that the NERL circuit consumed substantially less energy than the other adiabatic logic circuits at low-speed operation. NERL is more suitable than the other adiabatic logic circuits for the applications that do not require high performance but low energy consumption. Thus technique specifically used for applications where low power consumption is high priority compared to performance.

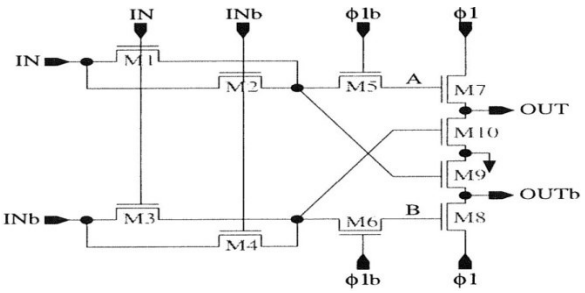

Fig4: NMOS energy recovery logic gate

ii)

iv)Clocked Adiabatic Logic (CAL):

This logic is little bit different compared to other adiabatic logic technique, CAL is a dual-rail logic that operates from a single-phase AC power-clock supply . In the adiabatic mode, low voltage d.c power supply is used, which is used to generate the power-clock supply waveform using an on-chip switching transistor and a small external inductor between the chip and a low-voltage dc supply. The basic CAL gate, the inverter, is shown in Figure5 Cross-coupled CMOS inverters, transistors M1 to M4, provide memory function. In order to realize an adiabatic inverter and other logic functions with a single power clock, an auxiliary timing control clock signal CX has been introduced, as shown in Figure 5. This signal controls the transistors that are in series with the logic trees represented by the functional blocks F and /F. The CX-enabled devices allow operation with a single power clock pwr.

Figure5 : The basic CAL gate- the inverter

v)True Single-Phase Adiabatic Logic (TSEL)

True single phase adiabatic logic is a partially adiabatic circuit family related to 2N2P, 2N- 2N2P, and CAL. Power is supplied to TSEL gates by a single phase sinusoidal power-clock. Cascades are composed of alternating PMOS and NMOS gates. In TSEL two dc reference volatages are used, here Two DC reference voltages ensure high-speed and high-efficiency operation. They also enable the cascading of TSEL gates in an NP-domino

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style. In comparison with corresponding adders in Alternative logic styles and minimum possible supply voltages, it is more energy efficient across a broad range of operating frequencies.Specifically for clock frequencies ranging from 10MHz To 200MHz. TSEL is the first energy-recovering logic family that operates with a single-phase sinusoidal clocking scheme. Both TSEL and SCAL gates are dual-rail and always present a balanced load to the clock generator, regardless of the particular data computed. Moreover, they are both functionally complete.

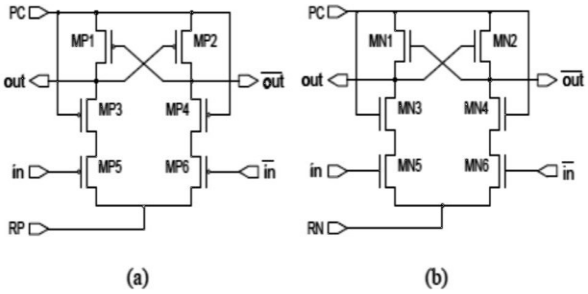

Figure6 : (a) TSEL gates using PMOS (b)TSEL gates using NMOS

vi)Source-Coupled Adiabatic Logic (SCAL)

Source coupled adiabatic logic(CAL) is a quasi adiabatic, dynamic logic family. SCAL retains all of TSEL's positive features, including single-phase power-clock operation. Moreover, it achieves energy efficient operation across a broad range of operating frequencies by using an individually tunable current source at each gate. SCAL achieves increased energy efficiency by using a tunable current source to control the rate of charge flow into or out of each gate. Our adiabatic circuitry avoids a number of problems associated with multiple power-clock schemes, including increased energy dissipation, layout complexity in clock distribution, clock skew, and multiple power-clock generators.

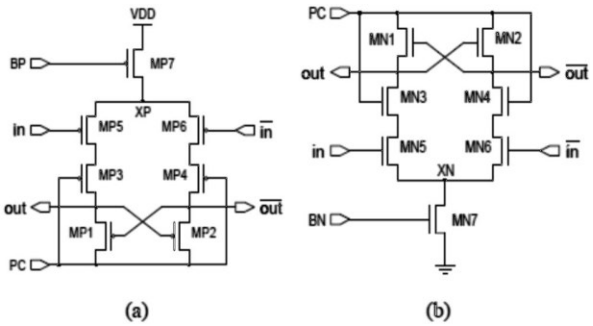

Figure 7: (a) Source-Coupled Adiabatic Logic using PMOS (b) Source-Coupled Adiabatic Logic using NMOS

vii) 2N-2N2P Adiabatic Logic

It is one of the partially adiabatic logic family,its main functionality is to reduce coupling effect,The 2N-2N2P logic family was derived from 2N-2P in order to reduce the coupling effect. The major difference with respect to 2N-2P is that the latch is made by two pMOSFETs and two nMOSFETs, rather than by only two pMOSFETs as in 2N-2P. The additional cross-coupled nMOSFET switches lead to non-floating outputs for a large part of the recovery phase.

B. FULLY ADIABATIC LOGIC

These types of adiabatic logic circuits have non-adiabatic loss but they are much more complex than previous adiabatic logic circuits. All the charge which is stored in capacitor is fully recovered by the power supply. Power clock synchronization and operating speed is the major problem in fully adiabatic logic circuits

Some of the fully adiabatic logic families include:

1. Pass transistor adiabatic logic(PAL)
2. Phase adiabatic Static CMOS logic (2PASCL)
3. Split rail charge recovery logic (SCRL)

i) **i) Pass Transistor Adiabatic Logic (PAL):**

PAL is a dual-rail adiabatic logic with a relatively low gate complexity that operates with a two-phase power clock. A PAL gate consists of true and complementary pass transistor NMOS functional blocks (f, /f), and a cross coupled PMOS latch (M p l, Mp2), as illustrated by the example of Figure 12, which shows the implementation of an AND-OR gate: Q = A.B + C. The power is supplied through a sinusoidal power-clock (PC). When PC starts rising from low, input states make a conduction path from the power clock (PC) through one of the functional blocks to the corresponding output node and allow it to follow the power clock. The other node will be tri-state and kept close to OV by its load capacitance. This in turn causes one of the PMOS transistors to conduct and charge the node that should go to one state, up to the peak of PC. The output state is valid at around the top of the power clock.

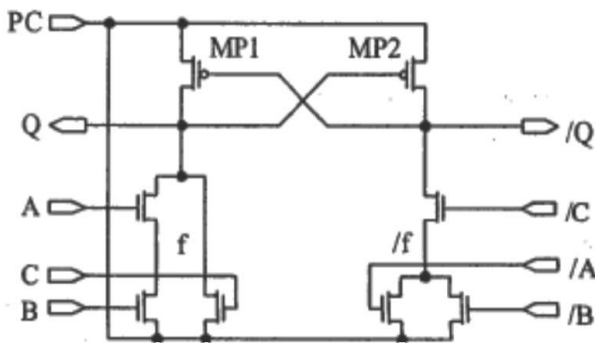

Figure8 : A PAL gate consists of true and complementary pass transistor, NMOS functional blocks and a cross coupled PMOS latch

The power clock will then ramp down toward zero, recovering the energy stored on the output node capacitance. Pass Transistor adiabatic logic (PAL) family exhibits considerable improvements in terms of energy savings and switching noise characteristics, it has the disadvantages of higher supply voltage and lower speed of operation

ii) **Split Charge Recovery Logic (SCRL)**

Split-Level Charge Recovery Logic (SCRL), within which the transfer of charge between the nodes occurs quasi statically. Operating quasi statically, these logic families have an energy dissipation that drops linearly with operating frequency, i.e., their power consumption drops quadratic ally with operating frequency as opposed to the linear drop of conventional

CMOS. The circuit techniques in these new families rely on constructing an explicitly reversible pipelined logic gate, where the information necessary to recover the energy used to compute a value is provided by computing its logical inverse. Information necessary to uncompute the inverse is available from the subsequent inverse logic stage. We demonstrate the low energy operation of SCRL by presenting the results from the testing of the first fully quasi static 8 × 8 multiplier chip (SCRL-1) employing SCRL circuit techniques.

III. CONCLUSION

Our study showed that adiabatic logic circuits provide a method of decreasing the energy dissipation when compared with conventional logic switching under certain circumstances. With adiabatic circuits all input signals must undergo a controlled transition in the form of a ramp, unlike the conventional logic switching where only the input signals which have different final logic state change. To reduce energy dissipation, logic switching cannot be instantaneous but must be gradual instead. With the circuits examined in this paper, there is a lower limit to the energy dissipation beyond which no significant improvements can be achieved for increasing rise/fall times.

This limitation is mainly due to the finite threshold voltage of the MOS transistors and possibly to a lesser extent, the non linear characteristics of the MOS channel resistance.

It was also observed that the fully adiabatic circuits reduce the power consumption significantly but they are very complex to design and although the partially adiabatic circuits are not as efficient as fully adiabatic circuits in terms of power consumption but they reduce the circuit complexity and conserve the power. So we can say that partially adiabatic circuits are fair compromise between the power consumption and complexity trade off.

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