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Ultra Low-Power Scheming of an Efficient Shift Register by Means of Pulsed Latch

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ABSTRACT:

Shift registers are usually used in lots of applications, such as digital filters and communication receivers. In the recent times, as size of image data maintain to increase because of high demand in support of high quality image data, word length of shift register increases for processing huge image data within image processing Integrated circuits. As the recent trends mandate low power design automation on particularly vast scale for matching the trends of power consumption of the present days as well as future integrated chips. We introduce a low-power as well as area-efficient shift register by means of pulsed latches which is an important solution intended for small area as well as low power consumption. Area as well as power consumption are reduced in the proposed system by replacing flip-flops by means of pulsed latches. The proposed system saves area and power when compared to traditional shift register with flip-flops. The shift registers lessen number of delayed pulsed clock signals significantly, though it increases number of latches because of additional temporary storage latches.

Keywords: Shift registers, Integrated circuits, Pulsed latches, Power consumption, Flip-flops, Pulsed clock signals, Image data.

1. INTRODUCTION:

Flip flops are basic elements of storage that are used widely in all types of digital designs. The performance of flip-flop is an important aspect to control the efficiency of complete synchronous circuit. The speed of flip-flop is less significant than area as well as power consumption since there is no circuit among flip-flips within the shift register. A shift register is the

fundamental building block within a VLSI circuit. They are group of flip-flops that are linked in a chain so that output from one flip-flop becomes input of subsequent flip-flop [1]. The present trends will eventually mandate low power design automation on extremely huge scale for matching the trends of power consumption of the present days as well as future integrated chips. While many contributions were made in the direction of art of single edge triggered flip-flops, a requirement clearly occurs for design that further progress performance of single edge triggered flipflops. Our work put forward a low-power as well as area-efficient shift register by means of pulsed latches. The shift register solves the problem of timing among pulsed latches by means of using several non-overlap delayed pulsed clock signals in place of traditional single pulsed clock signal. The shift register makes use of a little number of pulsed clock signals by means of combining latches to numerous sub shifter registers and by means of extra temporary storage latches. In the proposed system, area as well as power consumption are reduced by means of replacing flip-flops by means of pulsed latches. The proposed shift register will save area and power when compared to traditional shift register with flip-flops.

2. METHODOLOGY:

Shift registers are kind of sequential logic circuit, mostly used for storing of digital data. Shift registers are group of flip-flops that are associated in a chain and in this arrangement output from one flip-flop acts as the input of subsequent flip-flop. Flip-flops are perilous timing elements within digital circuits which contains a high impact on the speed of circuit as well as power consumption. For the most part of the registers hold no distinguishing internal sequence of states. All flip-flops are driven by means of a common clock, and all are set at the same time. The performance of flip-flop is significant to control efficiency of complete synchronous circuit. While the word length of shifter registers increase, area as well as power consumption of shift register turn into essential design considerations. The structural design of a shift register is relatively simple where an N-bit shift register includes series of connected N data flip-flops. The speed of flip-flop is

less significant than area as well as power consumption since there is no circuit among flip-flips within the shift register. The smallest flip-flop is appropriate for shift register to decrease area as well as power consumption [2][3]. In the recent times, pulsed latches have replaced flip-flops in lots of applications, since a pulsed latch is much small when compared to a flip-flop. However pulsed latch cannot be utilized within a shift register because of the timing problem among pulsed latches. In our work we introduce the low-power and area-efficient shift register which solves the problem of timing among pulsed latches by using numerous non-overlaps delayed pulsed clock signals rather than traditional single pulsed clock signal. The proposed shift register utilizes small number of pulsed clock signals by grouping latches to several sub shifter registers and by additional latches of temporary storage. A master-slave flip-flop by means of two latches within Master-slave flip-flop is replaced by means of a pulsed latch that consists of a latch as well as pulsed clock signal within pulsed latch. All pulsed latches will share pulse generation circuit in support of pulsed clock signal thus, area as well as power utilization of pulsed latch turn into almost half of the master-slave flip-flop.

3. AN OVERVIEW OF PROPOSED SHIFT REGISTER:

The pulsed latch is an important attractive solution intended for small area as well as low power consumption. The pulsed latch cannot be utilized within shift registers because of timing problem. The shift register includes numerous latches as well as a pulsed clock signal. The operation waveforms within Shift register with latches and a pulsed clock signal waveforms show timing difficulty within the shifter register. The output signal of first latch change accurately since input signal of first latch is stable throughout clock pulse width. But second latch contain an uncertain output signal as its input signal alters throughout the clock pulse width. One solution meant for timing difficulty is to insert delay circuits among latches. The output signal of latch is postponed and achieves the next latch subsequent to clock pulse. In the shift register with latches, delay circuits, and a pulsed clock signal waveforms, output

signals of first as well as second latches alter at some stage in clock pulse width, but input signals of second as well as third latches turn into the same as output signals of first as well as second latches following clock pulse. As a result, all latches have constant input signals during the clock pulse and no timing problem occurs between latches. On the other hand, delay circuits will make huge area as well as power overheads. A different solution is to make use of numerous non-overlaps delayed pulsed clock signals which are produced when pulsed clock signal goes all the way through delay circuits. Each latch makes use of a pulsed clock signal which is postponed from pulsed clock signal used within its subsequent latch [4]. Hence each of the latch updates data subsequent to its next latch updates data. Thus, each latch contains a stable input throughout its clock pulse and no timing difficulty take place between latches. The proposed shift register is separated into sub shifter registers to decrease number of delayed pulsed clock signals and it solves the problem of timing among pulsed latches by means of using several non-overlap delayed pulsed clock signals in place of traditional single pulsed clock signal. A 4-bitsub shifter register includes five latches and it carry out shift operations by means of five non-overlap pulsed clock signal that are delayed. The proposed system makes use of a little number of pulsed clock signals by means of combining latches to numerous sub shifter registers and by means of extra temporary storage latches [5]. Small number of pulsed clock signals is used by grouping of latches to several sub shifter registers and make use of added temporary storage latches. The proposed shift register reduce number of delayed pulsed clock signals considerably, although it increase number of latches due to the added temporary storage latches. The proposed shift register make use of latches rather than flip flops to decrease area as well as power consumption. In chip implementation, static differential sense amp shared pulse latch is selected which is the smallest latch. The proposed shift register attains a small area as well as low power consumption when compared to traditional shift register [6].

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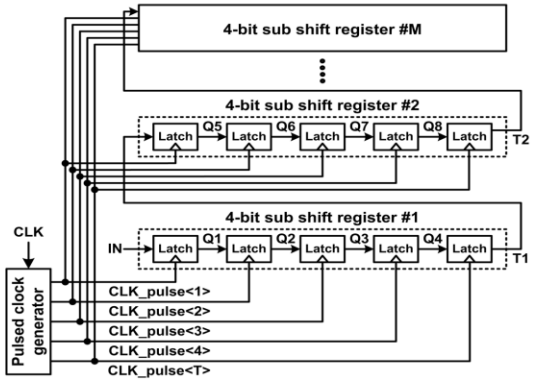

Fig1: An overview of proposed system

4. CONCLUSION:

Recently, pulsed latches have replaced flip-flops in several applications, as a pulsed latch is greatly small when compared to a flip-flop. Pulsed latch cannot be utilized within a shift register due to timing problem among pulsed latches. Here we introduce low-power as well as area-efficient shift register by means of pulsed latches and in this system area as well as power consumption are reduced by means of replacing flip-flops by means of pulsed latches. The proposed system will save area and power when compared to traditional shift register with flip-flops. The shift register decreases number of delayed pulsed clock signals considerably, although it increase number of latches due to the added temporary storage latches. It reduces area as well as power consumption by means of replacing flip-flops by pulsed latches and save area and power when compared to traditional shift register with flip-flops. The timing difficulty among pulsed latches is solved by means of numerous non-overlap delayed pulsed clock signals in place of a particular pulsed clock signal. A minute number of pulsed clock signals are used by grouping of latches to numerous sub shifter registers and make use of added temporary storage latches.

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