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Analysis of Positive Current Conveyor

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Abstract*— *In this paper we have analysis of positive current conveyor using 0.12 µm using CMOS technique. The complete implementation and verification is done on the Tanner tool, Schematic of the positive current conveyor is designed on the S-Edit and net list simulation done by using T-spice and waveforms are analysed through the W-edit. The circuit is characterized by using the 0.12µm technology which is having supply voltage 0f 1.2volt.

***Keywords*—** CMOS SRAM, NLPP, PLNP, PMOSFET, NMOSFET, TANNER TOOL S-edit, L-edit, W-edit

Introduction

At the time of the introduction of the current conveyor (1968) it was not clear what advantages the current conveyor offered over the conventional op-amp. Moreover, the electronics industry was just beginning to focus its efforts on the creation and application of the first generation of monolithic op-amps. Without clearly stated advantages, the electronics industry lacked the motivation to develop a monolithic current-conveyor realization. After all, the op-amp concept was entrenched in the minds of many analog circuit designers since the late 1940's and as far as IC manufacturers were concerned an op-amp market was already there to be tapped and expanded.

It is only now that analog designers are discovering that the current conveyor offers several advantages over the conventional op-amp, specifically a current conveyor circuit can provide a higher voltage gain over a larger signal bandwidth under small or large signal conditions than a corresponding op-amp circuit in effect a higher gain – bandwidth-product.

In addition, current conveyors have been extremely successful in the development of an instrumentation amplifier which does not depends critically on the matching of external components, instead depends only on the absolute value of a single component.

Applications of current conveyor:

The current conveyor is help full in realization of controlled sources, resistivity converters, resistivity inverters, gyrators, and numerous analog computation components as shown within the below table. The differential distinction current conveyor is help ful in applications like analog signal process, Automatic management and instrumentation system. The varied analog circuits like filters, generator and CMOS primarily based multiplier; divider may be forced with the assistance of current conveyors.

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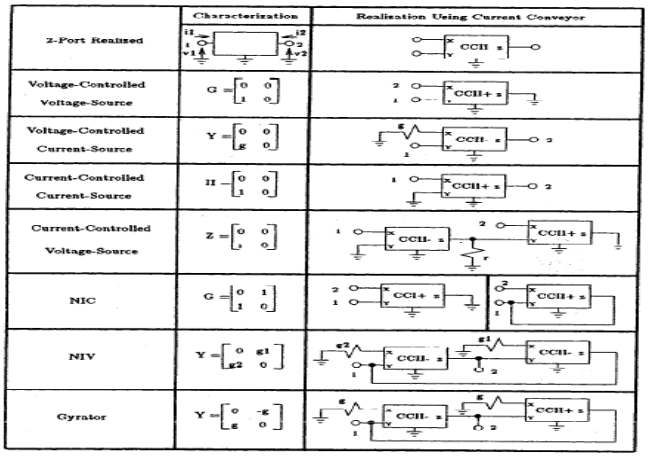

Table: 1 Applications to current conveyor to active network synthesis

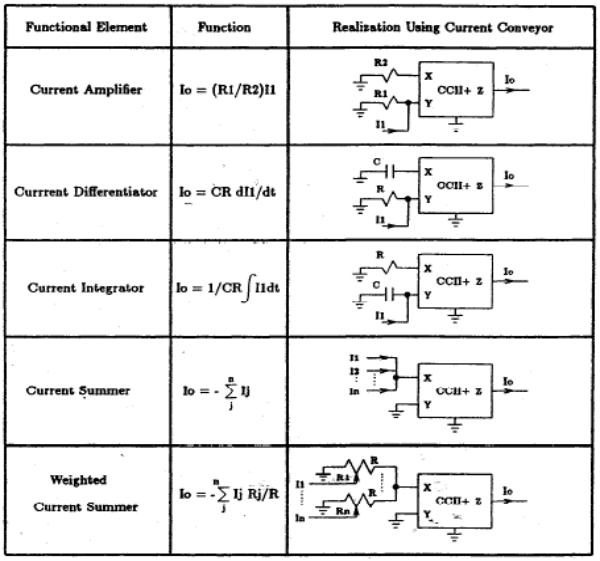

Table 2.Application of current conveyor to analog computation

The First Current Conveyor (CCI)

The current conveyor (CCI), as a introduced, could be a three-port device whose black–box illustration may be seen in figure the operation of this device is specified if a voltage is applied to input terminal Y, associate equal potential can follow the input terminal X. in a very similar fashion, associate input current I being forced into terminal X can end in associate equal quantity of current flowing into terminal Y. As well, the presented will be able to be sent to output terminal Z specified terminal Z has the characteristics of a current supply, of value I, with high output electrical phenomenon. As may be seen, the potential of X, being set by that of Y, is free lance of the present being forced into port X. Similarly, the present through input Y, being fastened by that

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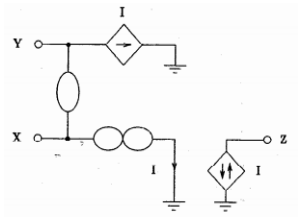
of X, is free lance of the voltage applied at Y. Therefore the device exhibits a virtual short–circuit input characteristic at port X and at win virtual open-circuit input characteristic at port Y.

$$\begin{bmatrix} i_Y \\ v_X \\ i_Z \end{bmatrix} = \begin{bmatrix} 0 & 1 & 0 \\ 1 & 0 & 0 \\ 0 & \pm 1 & 0 \end{bmatrix} \begin{bmatrix} v_Y \\ i_X \\ v_Z \end{bmatrix}$$



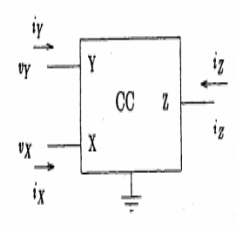


Fig.1 proposed positive current conveyor

Fig.2 proposed positive current conveyor

The Second generation current conveyor (CCII)

To increase the flexibility of the present conveyor, a second version within which no current flows in terminal, Y was introduced. This building block has since proved to be a lot of help full than CCI. Utilizing an equivalent diagram drawn of figure three, CCII is represented by

$$\begin{bmatrix} i_Y \\ v_X \\ i_Z \end{bmatrix} = \begin{bmatrix} 0 & 0 & 0 \\ 1 & 0 & 0 \\ 0 & \pm 1 & 0 \end{bmatrix} \begin{bmatrix} v_Y \\ i_X \\ v_Z \end{bmatrix}$$

Thus terminal Y exhibits a infinite input electrical phenomenon. The voltage at X follows that applied to Y; therefore X exhibits zero input electrical phenomenons. The present sent to the high-impedance output terminal Z where verit'sfurnished witheither positive polarity (CCII+) or negative polarity (CCII-).

Positive current conveyor

The primary circuit enforced is that the positive current conveyor since negative current conveyor is thought-about associate extension of the positive current conveyor. Within the implementation, straightforward current mirror were used despite their low output resistance and poor current gain. The explanation behind this alternative follows from the allowable signal swing at the X terminal. (Refer to work 1.6 (a)) is set by the state of semiconductor unit M1 whereas the negative signal swing is set by money supply.

As long as each transistor stay saturated, the output stage of the op-amp can perform needless to say. so the negative signal swing is restricted to Vds sat2 higher than the negative input bias voltage of the n-channel current mirror whereas the positive signal swing is restricted to Vds sat1 below the positive input bias voltage of the p-channel current conveyor. The circuit implementation of the positive current conveyor is shown in fig.

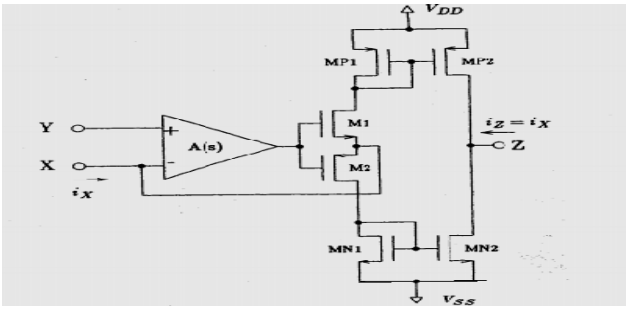


Fig:3 Positive current conveyor

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Design of CMOS based Positive current conveyor.

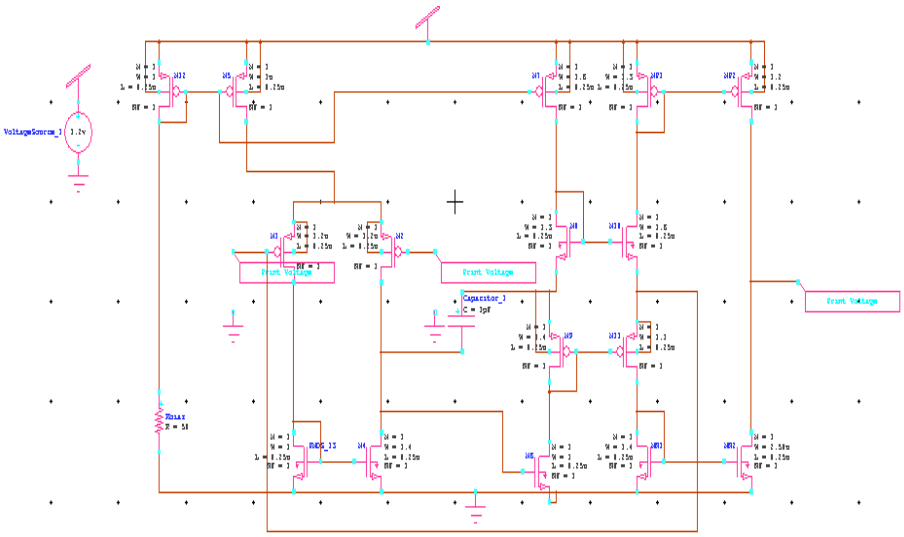

Fig.4 proposed positive current conveyor

In positive current conveyor style the planning the look} of op-amp is equally as shown on top of and also the design of two current mirror units is given below. In current conveyor the present mirror is made by junction transistor MN1, MN2 and MP1, MP2. The current flow through MP1 corresponding VGSP1. Since VGSP1=VGSP2, Ideally an equivalent current or a multiple of the present in MP1 flow through MP2 If the MOSFET are an equivalent size an equivalent drain current flow in every . MOSFET provided MP2 keep within the saturation region. The present IMP is given by

$$I_{MP1} = \beta_1/2*(V_{GS1} - V_{thp})\,2 \qquad 1$$

$$I_{MP2} = \beta_2/2*(V_{GS2} - V_{thp})\,2 \qquad 2$$

$$I_{MP1}/\ I_{MP2} = (W/L)_2/(W/L)_1 = \beta_2/\beta_1 \qquad 3$$

The equation show how to adjust the W/L ratio of the two devices to achieve the desired output current I_{MP2}.The design of second current mirror is similarly as explained.

S.No.	Transistor	W/L
1.	M1,M2	25.7/0.6
2.	M3,M4	7.5/1.5
3.	M5,M7,M12	22.5/1.5
4.	M6	14.25/1.5
5.	M8,M10	40/0.755
6.	M9	86.25/0.75
7.	M11	120.75/.75
8.	MP1,MP2	54.75/1.5
9.	MN1,MN2	30/1.5

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Simulation Results of Second generation CMOS based Positive current conveyor

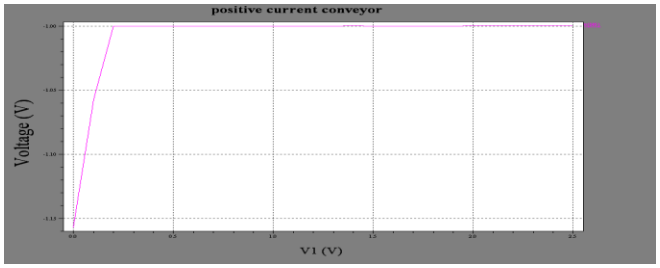

Fig: 5 Voltage at current in-put terminal when -1V is applied at Y terminal

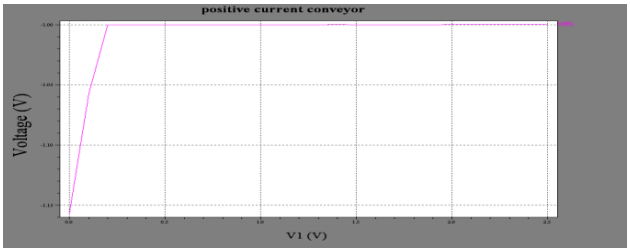

Fig: 6 Current at out-put terminal Z+ when 50 µA is applied at X terminal.

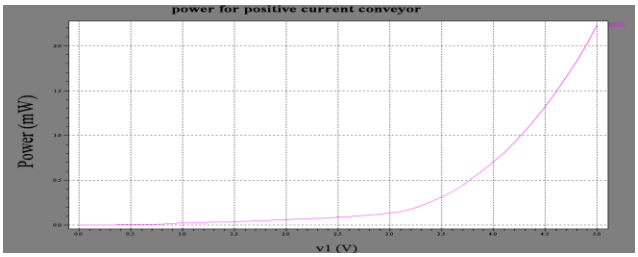

Fig: 7 the leakage power consumed by positive current conveyor.

S.No.	Current at Input Terminal (µA)	Current at Output Terminal (µA)
1	10	10.63
2	50	50.00
3	100	99.73
4	150	149.94
5	200	200
6	300	297.4
7	350	345.67

The above table shown the relationship at current input terminal (X) and current out -put terminal (Z+). When an input current I being forced into terminal X will result in an equal amount of current flowing into terminal Z+ with same polarity up to current range o to 300 µA.

CONCLUSION

The design and implementation of the positive current conveyor is shown in this paper using cmos technology. The voltage applied at Y terminal it will convey to X terminal and independence the value of current applied at X terminal up to voltage range 1.35 to -1.35. The leakage power consumed by CMOS based positive current conveyor is 2.24mW.

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