Modeling and Design of Series Voltage Compensator for Reduction of DC-Link Capacitance fed Industrial Drive Applications

Pappula Sampath Kumar
Research Scholar
EEE Department,
JNTUK , Kakinada;
A.P, India.
pappulasampathkumar@gmail.com

Jesta Poorna Chandra Rao
PG Scholar
EEE Department,
BEC, Bapatla;
A.P, India
purna.jesta@gmail.com

Dr. M. Sushama
Professor
EEE Department
JNTUH, Hyderabad;
TG, India
m73sushama@yahoo.com

Abstract-In this paper Design of Series Voltage Compensator for Reduction of DC-Link Capacitance in Grid-Tie Solar Inverter is proposed. A grid-tie solar inverter with a series voltage compensator for reducing the high-voltage dc-link capacitance is presented. The compensator obtains energy from the dc link to sustain the voltage on its dc side and generates an ac voltage to counteract the voltage ripple on the dc link. As the compensator processes small ripple voltage on the dc link and reactive power, it can be implemented with low-voltage devices, and thus, its volt amp rating is small. As the required energy storage of the dc link, formed by a reduced value of the dc-link capacitor and the compensator, is reduced, the architecture allows replacing popularly used electrolytic capacitors with alternatives of longer lifetime, such as power film capacitors, or extending the system lifetime even if there is a significant reduction in the capacitance of electrolytic capacitors due to aging. Detailed mathematical analysis on the static and dynamic behaviors of the overall system, and the control method will be presented. The simulation results are presented by using Matlab/Simulink system.

Index Terms—Capacitors, capacitor-supported systems, dc–ac power conversion, grid-tie solar inverters, photovoltaic systems, reliability.

I. INTRODUCTION

A capacitor-supported system consists of multiple power converters interconnected by a dc link. The dc-link voltage is maintained by a capacitor bank that absorbs instantaneous power difference between the input source and output load, minimizing voltage variation on the dc link, and providing sufficient energy during the hold-up time of the system. Among different types of capacitor, aluminum electrolytic capacitors (E-Caps) are the most popular choice because of their high volumetric efficiency and low cost. However, they suffer from the drawbacks of high equivalent series resistance (ESR); low ripple current capability; bottleneck of the voltage rating; relatively

short lifetime compared to other components; and considerable maintenance work. Advances in power film capacitor technology are emerging for dc-link filtering [1], [2]. Power film capacitors outperform aluminum E-Caps in terms of ESR, self-healing capability, life expectancy, environmental performance, dc-blocking capability, ripple current capability, and reliability. Although low-voltage and high-value film capacitors are available, the capacitance of the high-voltage film capacitors still cannot compete with E-Caps, due to their relatively low volumetric efficiency and high cost. To lessen the dependency of the dc-link capacitance, there are many prior-art methods, based on the following approaches:

1) Performance trade-off:- This method allows a larger voltage ripple across the dc link with a smaller capacitance. However, it is practically less impressive as the system performance will be degraded. It is more suitable for certain applications, like the ones in [3]–[5]. A set of design procedure is given in [6] for the optimization of capacitor bank.

2) Reduction of the dc-link capacitor current with sophisticated control: The concept is based on reducing the ripple current flowing through the dc-link capacitor [7]. The front-stage converter is an active rectifier, and a step-up dc–dc converter in [8], while the output is an inverter. Their key advantage is that no additional circuit is needed. However, those control methods cannot be applied to systems with front-end diode-bridge rectifier. Apart from requiring a sophisticated controller, some of them also rely on specific relationship in the operating frequency between the converters connected [9].

The method given is limited to three-phase systems. The controller described is based on assuming an ideal energy

conversion. Thus, the actual input current would be distorted unless multiple cell load inverters are used. The performance of those controllers is greatly dependent on the accuracy of the computations [10] and affected by the overall time delays of the control loops.

3) Increase in the frequency of the dc-link voltage ripple: A double frequency front-end converter with multiphase switching is proposed in [11] to reduce the ripple voltage. However, the approach cannot reduce the dc-link capacitance significantly.

4) Ripple cancellation circuit with a coupled element: In [12], a coupled inductor is applied to cancel the voltage ripple of the dc input, dc output, or dc link of a power converter. The concept is based on assuming that the capacitor used in the storage tank is infinite. But in reality, the capacitance has a finite value, and the coupled inductor filter and the capacitor form a low-pass filter. To avoid large-sized coupled windings, the technique is more suitable for filtering high-frequency ripples or noise, such as switching ripple, EMI filtering. Moreover, the dynamic response of the capacitor may be degraded due to the series-connected coupled winding. Large electric drives will require advanced power electronic inverters to meet the high power demands (>1 MW) required of them. One inverter type which is uniquely suited for this application is the multilevel inverter [13]. Two different multilevel converter topologies are ideal for use as large electric drives. The cascaded inverter with separate dc sources closely fits the needs of all-electric vehicles because it can use the onboard batteries or fuel cells to synthesize a sinusoidal voltage waveform to drive the main vehicle traction motor. Where generated ac voltage is available, a back-to-back diode clamped converter can be used to output variable frequency ac voltage for the driven motor [14].

II. OPERATION OF THE SERIES VOLTAGE COMPENSATOR

Fig. 1 shows the architecture of the grid-tie solar inverter system with a series voltage compensator connected to the dc link. The system consists of two power conversion stages. The front stage is a dc–dc boost converter. It is connected between a string of solar panels and the dc link. The output stage is a grid-tie dc–ac converter, which is connected between the dc link and the power grid. The compensator, which is a capacitor supported full-bridge dc–ac converter without an external dc source, is connected between the two converters. The voltage compensator generates an ac voltage that counteracts the ripple voltage on the output of the boost converter. Thus,

the input of the grid-tie inverter is a dc voltage equal to the average value of the voltage Vdc across the dc-link capacitor Cdc .The dc-link voltage Vdc and the input voltage of the voltage compensator Va are sensed. The scaling factor α is the ratio between Vtric and Va,ref , where Vtric is the amplitude of the triangular carrier signal Vtric in the PWM controller and Va,ref is the voltage reference for the input voltage of the voltage compensator. The difference between Va,ref and va is processed by a PI controller G(s) to give an offset voltage vos. The control signal vcon is obtained by combining α vdc with vos. The dc component of α vdc is ideally cancelled in vcon by vos as Vos =−αVdc, where Vos and Vdc are the dc component of vos and vdc, respectively. With such arrangement, it is unnecessary to use a high-pass filter to extract the ac component of vdc. At the same time, the stable dc level of Va can be obtained by
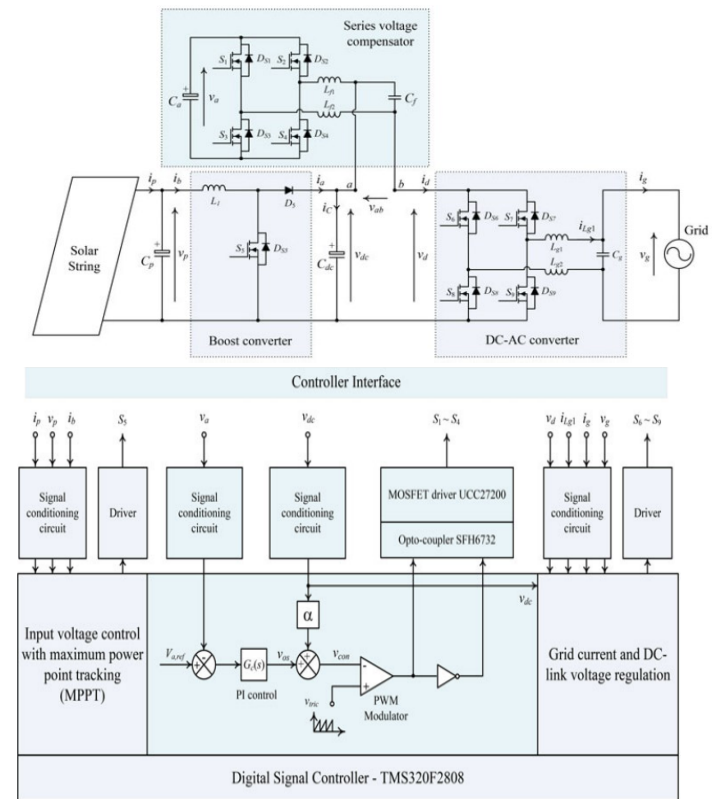

Fig. 1. Architecture of the grid-tie solar inverter with a series voltage compensator.

Voltage control, which ensures the compensator only handles the reactive power in the steady state. During the steady-state operation, Vcon equals the conditioned ac component of αVdc. It is then used to compare with the

triangular carrier waveform in the pulse width modulation modulator to generate the voltage Vab having the same phase and amplitude with ΔVdc. Without any external power supply, the power dissipation of the voltage compensator is obtained from the dc link. Practically speaking ,instead of a pure ac voltage, both Vab and Vcon consists of not only ac component, but also small amount of the dc component .Since the input current of the grid-tie inverter consists of the dc component, some power will be absorbed by the compensator if Vab consists of the dc component. Derivations of the parameters in the control.

III. SYSTEM CHARACTERISTICS

The grid voltage vg and the output grid current ig can be expressed as

$$v_g(t) = V_g \sin \omega t \tag{1}$$

$$i_g(t) = I_g \sin(\omega t + \phi) \tag{2}$$

Where Vg and Ig are the amplitude of vg and ig , respectively, $\omega = 2\pi f$ is the angular line frequency, f is the line frequency, and φ is the phase difference between vg and ig .Based on (1) and (2), the instantaneous output power pg is

$$p_g(t) = v_g(t)i_g(t)$$
$$= \frac{2P_g}{\cos \phi} \sin \omega t \sin(\omega t + \phi) \tag{3}$$

Where Pg =VgIg/2 cos φ is the average output power. By applying the Kirchhoff's current law at the node of the Dc-link capacitor Cdc, the relationship among the output current i_a of the boost converter, the dc-link capacitor current ic, and input current id of the inverter can be expressed as

$$i_C(t) = i_a(t) - i_d(t) \tag{4}$$

The dominant component of ΔVdc is the double of the line frequency harmonics. For the sake of simplicity in the analysis ,ΔVdc is expressed as

$$\Delta v_{dc}(t) = |\Delta V_{dc}| \sin(2\omega t + \theta) \tag{5}$$

Where |ΔVdc| is the magnitude of ΔVdc and θ is the phase angle of ΔVdc.

A. Steady-State Characteristics of the Voltage Compensator

Since the voltage compensator counteracts the ripple voltage on the dc-link capacitor only, the input voltage of the grid-tie dc–ac converter, Vd, is equal to Vdc. By using

(3), the input current of the dc–ac converter, id, can be expressed as

$$i_d(t) = \frac{p_g(t)}{V_{dc}}$$
$$= \frac{P_g}{V_{dc} \cos \phi} [\cos \phi - \cos(2\omega t + \phi)] \tag{6}$$

By substituting (5) and (6) into (4),

$$\gamma \cos(2\omega t + \theta - \delta) = \frac{P_g}{\lambda V_{dc} \cos \phi} \cos(2\omega t + \phi) \tag{7}$$

Where

$$\gamma = \sqrt{\left(\frac{P_g}{V_{dc}}\right)^2 + (2\omega C_{dc} V_{dc})^2}, \delta = \tan^{-1}\left(\frac{P_g}{2\omega C_{dc} V_{dc}^2}\right)$$

and λ = |ΔVd c | /Vd c is the ripple factor.

Detailed proof of (7) is given in the Appendix. By equating the magnitude and phase angle of the LHS and RHS of (7), the following equations can be concluded

$$|\Delta V_{dc}| = \frac{P_g}{\gamma \cos \phi}$$

$$\theta = \phi + \delta. \tag{8}$$

By substituting (8) into (5), the ripple voltage on the dc-link capacitor is

$$\Delta v_{dc}(t) = \frac{P_g}{\gamma \cos \phi} \sin(2\omega t + \phi + \delta)$$
$$= \lambda V_{dc} \sin(2\omega t + \phi + \delta). \tag{9}$$

According to (9), the relationship among the dc-link capacitance Cdc, output phase angle φ, and the ripple factor λ is

$$C_{dc} = \frac{S_g}{2\omega V_{dc}^2} \sqrt{\frac{1}{\lambda^2} - \cos^2 \phi} \tag{10}$$

Where Sg is the apparent power of the solar inverter. Detailed proof of (10) is given in the Appendix.

Thus, for a given apparent power Sg , the required value of Cdc will increase as the power factor cos φ decreases. Thus, one of the design constraints is based on considering the minimum power factor. For example, as stated in the statutory requirement VDE-AR-N 4105, the minimum power factor is 0.9.As the compensator handles ripple voltage only (i.e., Vab =ΔVdc), the ratio between the apparent power handled by the compensator, Sab, and the apparent power of the whole system is

$$\frac{S_{ab}}{S_g} = \frac{v_{ab,\mathrm{rms}}\, i_{d,\mathrm{rms}}}{v_{d,\mathrm{rms}}\, i_{d,\mathrm{rms}}} = \frac{|\Delta V_{\mathrm{dc}}|}{\sqrt{2}\,V_{\mathrm{dc}}} \qquad (11)$$

where $V_{ab,\mathrm{rms}}$ and $v_{d,\mathrm{rms}}$ are the rms values of vab and V_d ,respectively, and $i_{d,\mathrm{rms}}$ is the rms value of the input current of the dc–ac converter. Thus, as ΔVdc Vdc, the power rating of the compensator is much smaller than that of the whole system. The voltage across the capacitor Ca, Va, is regulated at Va,ref by using the control mechanism depicted in Fig. 1. IfVa<Va,ref ,energy will be absorbed from the dc link, and vice versa. When Va=Va,ref , the voltage compensator will ideally absorb zero power. Based on (6) and (9), the average power absorbed by the voltage compensator Pab is

$$P_{ab} = \frac{1}{T} \int_0^T v_{ab}(t)\, i_d(t)\, dt$$

$$= -\frac{P_g^2 \sin\delta}{2\gamma V_{\mathrm{dc}} \cos^2\phi} \qquad (12)$$

Where the period $T = \pi/\omega$.

Thus, based on (12), if the compensator only generates the ripple voltage on the dc-link capacitor, it will generate active power. In order to maintain the power balance for stabilizing va at Va,ref , a small voltage offset at vab, Vab, appears

$$V_{ab} = \frac{-P_{ab}}{I_d}$$

$$= \frac{P_g \sin\delta}{2\gamma \cos^2\phi} \qquad (13)$$

The relationship between Vab and Va can be expressed as

$$v_{ab}(t) = \frac{v_{\mathrm{con}}(t)}{V_{\mathrm{tric}}} v_a(t)$$

$$= \frac{\alpha v_{\mathrm{dc}}(t) + v_{\mathrm{os}}(t)}{V_{\mathrm{tric}}} v_a(t)$$

$$= \frac{\alpha P_g}{\gamma V_{\mathrm{tric}} \cos\phi} \sin(2\omega t + \phi + \delta) v_a(t)$$

$$+ \frac{\alpha V_{\mathrm{dc}} + v_{\mathrm{os}}(t)}{V_{\mathrm{tric}}} v_a(t). \qquad (14)$$

The first term αPg sin(2ωt+φ+δ)γVtric cos φ va(t) represents the ripple voltage compensation on the dc-link capacitor. The second term αVdc +vo s (t)Vtric Va(t) represents the dc component, related to the power balance

described in (13). Thus, asymmetrical PWM switching occurs .Fig. 2(a) and (b) present the operating modes of the compensator using a full bridge. When S2 and S3 are on, the capacitor Ca is charged by the load current id. Conversely, when S1 andS4 are on, the capacitor Ca is discharged by id. Fig. 2(c) shows the waveforms of the dc-link capacitor voltage Vdc, modulating signal Vm , triangular carrier signal Vtric, and the voltage across Ca, Va .The dc component on Vab is very small. It is observed to be 2.1 V, about 0.5% of the average dc-link voltage of400 V in the 2-kW inverter system, which will be described. Thus, such dc component is neglected in the following discussion.
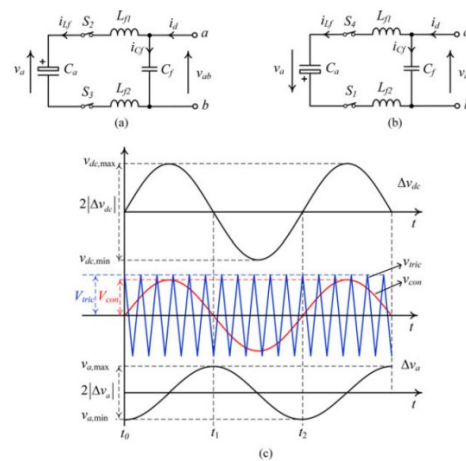

Fig. 2. Ripple voltage on the input capacitor Ca in the compensator. (a) Operation when S2 and S3 are on. (b) Operation when S1 and S4 are on. (c) SPWM and the ripple voltage generated across Ca .

During the time interval between the time instants t0 and t1 in Fig. 2(c), Ca is charged by the load current. By using (6) and (9)

$$v_a(t)$$

$$= v_{a,\min} + \frac{1}{C_a} \int_{t_0}^{t_1} [i_d(t) - i_{Cf}(t)] \frac{v_{\mathrm{con}}(t)}{V_{\mathrm{tric}}} dt$$

$$= v_{a,\min}$$

$$+ \frac{1}{C_a} \int_{t_0}^{t_1} \left\{ \frac{P_g}{V_{\mathrm{dc}} \cos\phi} [\cos\phi - \cos(2\omega t + \phi)] - i_{Cf}(t) \right\}$$

$$\times \frac{\alpha P_g}{\gamma V_{\mathrm{tric}} \cos\phi} \sin(2\omega t + \phi + \delta)\, dt \qquad (15)$$

Where Va ,min is the minimum voltage of Va.

From t0 to t1, the net charge on the output filter capacitor Cf is zero. Only the double frequency component of the voltage on Ca is considered. Based on (15), the peak-peak voltage on Ca,2|ΔVa|, is

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$$2\,|\Delta V_a| = \frac{\alpha P_g^2}{\gamma \omega C_a V_{dc} V_{tric} \cos\phi} \tag{16}$$

Thus, the voltage on Ca is

$$v_a(t) = V_a - \frac{\alpha P_g^2}{2\gamma \omega C_a V_{dc} V_{tric} \cos\phi}\cos(2\omega t + \phi + \delta) \tag{17}$$

Hence, the ripple voltage on the input of the voltage compensator is dependent on the values of Ca and Cdc. The guidelines for designing their values will be discussed later. Finally, based on (9), the voltage across Cdc, Vdc, and the current through Cdc, i_C , are

$$v_{dc}(t) = V_{dc} + \frac{P_g}{\gamma \cos\phi}\sin(2\omega t + \phi + \delta) \tag{18}$$

$$\begin{aligned} i_C(t) &= C_{dc}\frac{dv_{dc}(t)}{dt} \\ &= \frac{2\omega C_{dc} P_g}{\gamma \cos\phi}\cos(2\omega t + \phi + \delta) \end{aligned} \tag{19}$$

The maximum voltage across Cdc, Vdcmax, and the rms current through Cdc, ic,rms, are

$$V_{dc,max} = V_{dc} + \frac{P_g}{\gamma \cos\phi} \tag{20}$$

$$I_{C,rms} = \frac{\sqrt{2}\omega C_{dc} P_g}{\gamma \cos\phi} \tag{21}$$

B. Steady-State Characteristics of the Boost Converter

The voltage conversion ratio gb(t) of the front-stage boost converter is

$$\begin{aligned} g_b(t) &= \frac{v_{dc}(t)}{v_p(t)} \\ &= \frac{V_{dc} + \Delta v_{dc}(t)}{v_p(t)} \end{aligned} \tag{22}$$

Where $V_p(t)$ is the input voltage of boost converter.
Under the steady-state operation, V_p should be relatively constant in order to ensure that the solar string is controlled to operate at a stable operating point (normally at the maximum power point). Thus, based on (22), the duty cycle db(t) of the main switch S5 in the boost converter is

$$d_b(t) = 1 - \frac{V_p}{V_{dc}\,[1 + \lambda \sin(2\omega t + \phi + \delta)]} \tag{23}$$

Where Vp is the amplitude of Vp. Hence, the average duty cycle of S5, Db, is

$$D_b = 1 - \frac{V_p}{V_{dc}} \tag{24}$$

By substituting (24) into (23)

$$d_b(t) = 1 - (1 - D_b)\frac{V_{dc}}{v_{dc}(t)} \tag{25}$$

Based on (22), the minimum conversion ratio of the boost converter, gbmin, is unity. Thus

$$g_{b,min} = \frac{V_{dc}(1 - \lambda_{max})}{V_{p\_max}} = 1 \tag{26}$$

Where V_p max is the maximum input voltage of boost converter or the maximum voltage delivered by the solar string. Thus, based on (26), the maximum value of λ, λ_{max}, is

$$\lambda_{max} = 1 - \frac{V_{p\_max}}{V_{dc}}$$

By substituting (27) into (10), the minimum value of the dc-link capacitance, Cdc min, for a front-end boost converter is

$$C_{dc\_min} = \frac{P_g}{2\omega V_{dc}^2}\sqrt{\frac{1}{\left(1 - \frac{V_{p\_max}}{V_{dc}}\right)^2} - 1} \tag{28}$$

C. Small-Signal Dynamical Modeling

The solar string is modeled by a resistor Req. The boost converter, compensator, and the dc–ac converter are modeled by using the averaged ac modeling technique described. Their small-signal models and control block diagrams are shown in Figs. 3–5 the small-signal model of the whole system in Fig. 1 is shown in Fig. 6. Based on, the small-signal equation for the solar string is

$$\Delta V_p(s) = -R_{eq}\Delta I_p(s) \tag{29}$$

For the boost converter, the small-signal equations are given as follows:

$$\Delta V_p(s) - sL_1\Delta I_p(s) + V_{dc}\Delta D_b(s) - (1 - D_b)\Delta V_{dc}(s) = 0 \tag{30}$$

$$(1 - D_b)\Delta I_p(s) - I_p\Delta D_b(s) - \Delta I_a(s) = 0 \tag{31}$$

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$$\Delta D_b(s) = \frac{1}{V_{\text{trib}}} G_b(s) \Delta V_p(s)$$
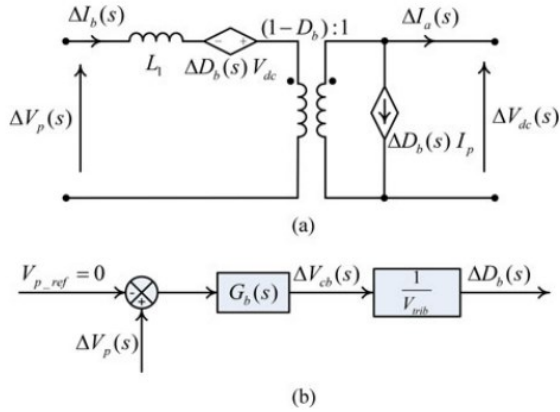
(32)

(a)

(b)

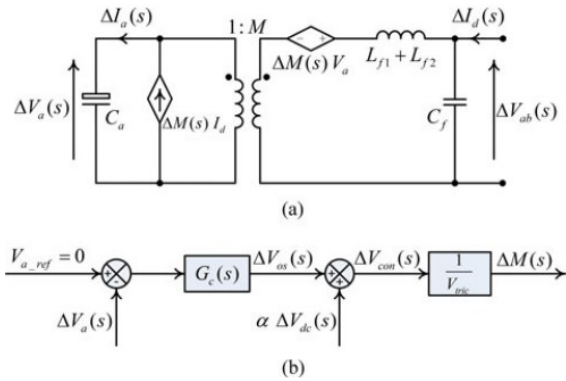Fig. 3. Modeling of the boost converter. (a) Power stage. (b) Control block diagram.

(a)

(b)

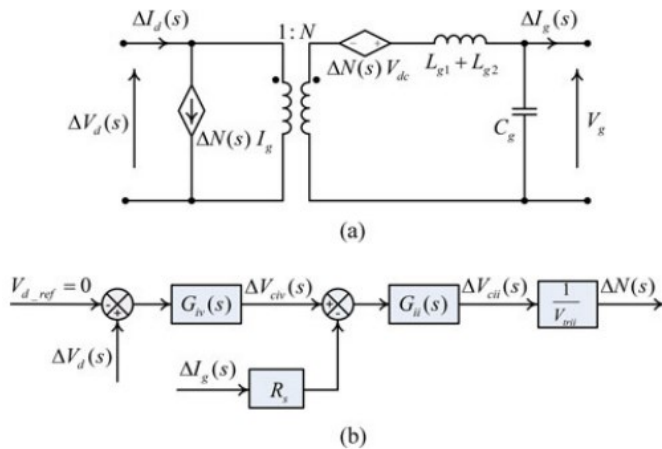Fig. 4 Modeling of the compensator. (a) Power stage. (b) Control block diagram.

(a)

(b)

Fig. 5. Modeling of the dc–ac converter. (a) Power stage. (b) Control block Diagram.

Where $G_b(s)$ is the transfer function of the controller in the boost converter and Vtrib is the amplitude of the carrier of the PWM modulator.

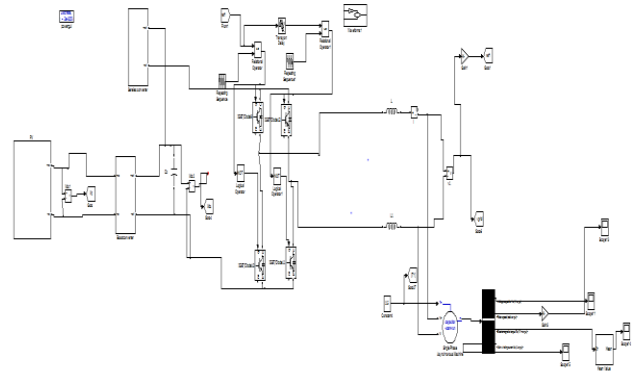## IV.MATLAB/SIMULATION RESULTS

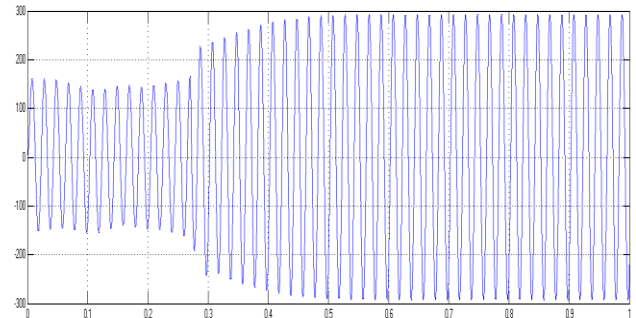Fig. 6. Simulink diagram with svc for induction motor

Fig. 7. Capacitor Voltage Waveform

In fig.7 shows the compensated voltage across the DC-link capacitor connected in system
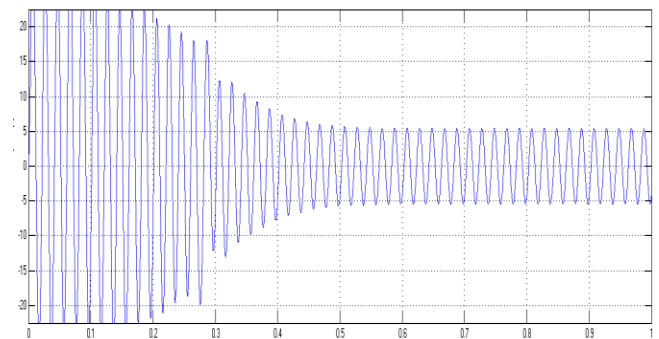

Fig. 8. Current Waveform

In fig.8 shows the main winding current of induction motor run by series connected compensator.
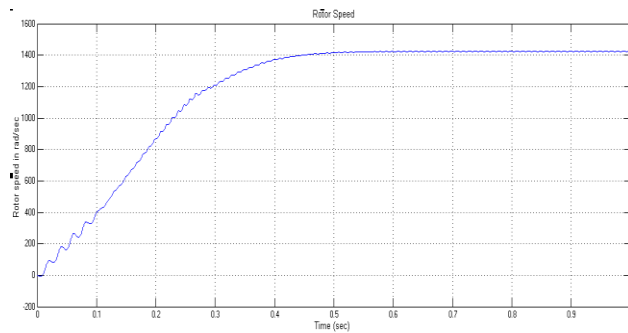

Fig. 9. Rotor Speed Waveform

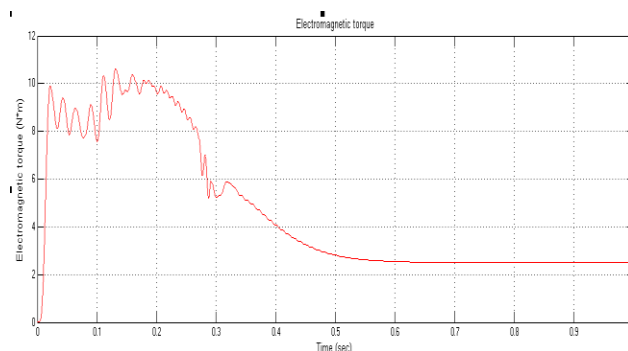Fig.9 shows the variation in rotor speed of induction motor.

Fig. 10. Electromagnetic Torque Waveform

Fig.10 shows the electromagnetic torque of induction motor.

V. CONCLUSION

This paper extends the study of the concept proposed, in which a series voltage compensator is used to reduce the dc-link capacitance. Such concept is applied to a grid-tie solar inverter. The modeling and design of the series voltage compensator has been presented. An active series voltage compensator for reducing the dc-link capacitance in a capacitor-supported power electronic system has been proposed. The implementation requires low-voltage devices only, as the dc-link module only handles ripple voltage in the dc-link and reactive power flow in the dc link. A detailed study on the dc and ac characteristics, stability analysis, and hold-up time performance has been given. The design guidelines for the dc-link module for applications with and without the hold-up time requirement have been described.

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