A Three-Phase Four-Switch PWM Voltage-Source Rectifier usingd-q control fed induction motor drive

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Abstract—Controller design for six-switch pulse width modulated (PWM) voltage source rectifiers (VSRs) is often accomplished in the rotating d-q frame coordinates in order to achievea high-performance control. In contrast, the development of a d-qframe controller for a four-switch PWM VSR is rarely reported inthe literature. In this regard, this paper introduces a control designapproach in rotating d-qframe for the four-switch PWM VSRs. Forthis purpose, a mathematical model of the four-switch PWM VSRin rotating d-q frame is first derived. Its success is relied on performing a so-called "reduced Park Transformation" on switchingfunctions. The derived model shares much structural property withthat of a six-switch VSR. Then, two d-q frame current controllerdesigns, input–output feedback linearization (IOFL) and linearproportional-plus-integral (LPI) control, are performed based onthe derived model as application examples. Their effectiveness isverified via computer simulation and hardware experiment. Responses of an LPI a-b-c frame controller originated from the six switch VSR are also documented for comparative study. Test resultsevidence the superiority of the d-q frame controllers.

Index Terms—Four-switch pulse width-modulated (PWM) voltage source rectifier (VSR), input–output feedback linearization(IOFL), linear proportional-plus-integral (LPI) control, reducedPark Transformation.

I. INTRODUCTION

Due to their low input current distortions, improved power factor, and regulated dc-ink voltage, pulse width modulated (PWM) voltage source rectifiers (VSRs) [1] are favourable substitutes for line-commutated rectifiers in high performance industrial applications. Recent investigations have mainly focused on the development of high-performance VSRs with six power switches (see for examples [1], leading to a high maturity in the development of both circuit topology and control methodology for this type of VSRs. From the aspect of current and dc-bus voltage control, controller design in rotating d-q frame has been popular since in this transformed coordinates the unity-power-factor control objective may be simplified to a set-point reference regulation problem, rather than a sinusoidal tracking problem. As a consequence, various control strategies
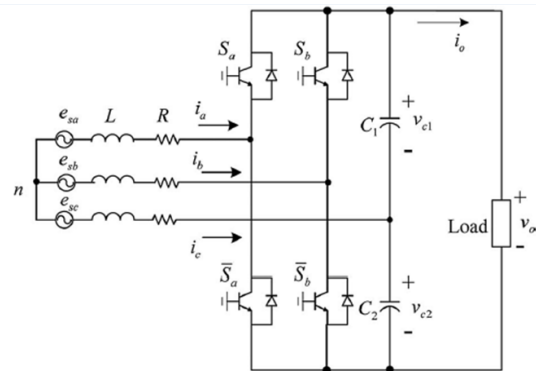

Fig. 1. Power circuit of the three-phase four-switch PWM voltage source rectifier.

to achieve the aforementioned objectives simultaneously under large perturbation in load have been reported [3]. Among these, a simple and effective control technique with the cascaded linear proportional-plus integral (LPI) control loop [3] would provide acceptable performance. As this type of VSR exhibits nonlinearity, nonlinear controller design methodologies, such as variable structure feedback linearization [9], passivity, flatness-based [13], and extended linearization [14], have been applied to achieve a high performance control with a wide operation range. In fact, the success of these control designsdepends mainly on the fidelity of rectifier's mathematical model. Despite the existence of a wealth of control algorithms for six-switch VSRs, the research on developing component minimized VSRs has grown recently, due to economic and reliability reason.

Hence, recent study has been focused on developing high-performance VSRs with less switches and reduced loss. PWM VSRs that can offer the same functionality with only four active switching devices have been considered inAnother research trend has also focused on using the four-switch inverters for motor drives although four-switch PWM VSRs have the feature of structural simplicity and reduced cost, two main shortcomings of this topology merit discussion concerning practical application. First, with the same ac supply, the lower output voltage bound is normally much higher than that of a six-switch PWM VSR; for a four-switch PWM VSR with

100-Vrms ac source supplying line current 7.07 Arms, the output dc voltage may reach as much as 480V. Hence, the high output voltage feature limits its application. Second, as the third phase ac current flows through the split capacitor bank, two output capacitors with large capacities are required to keep the voltage ripples small. However, little research has studied on the modelling and control of the four-switch PWM rectifier. In the work of Sheet al. [15], under the assumption that the VSR operates at steady state, both a-b-c and d-q frame models are derived. A control strategy, called a closed-form controller, to achieve high power factor and near-sinusoidal input current waveforms is reported. As this controller design is based on the steady-state model, transient performance of the current loop is not considered. Kim and Lipo used this type of circuit configuration to form a low cost rectifier/inverter system with only eight switches for ac drives.

In, Chiang devises a linearized dynamical model upon which a hysteresis current control scheme to produce high output voltage is devised. The guidelines to select adequate passive elements such as an inductor and a dc-bus capacitor for a four-switch VSR to operate properly are also documented. Subsequently, an improved version with reduced number of hysteresis comparator is reported in. However, a major drawback of hysteresis current controller is that its switching frequency varies with dc-load current and the power switches are subject to additional stresses. proposes a proportional-plus-integral current controller with compensation for three phase unbalanced supply. By using a mixed p-z approach, mathematical expressions of the system responses is derived and verified experimentally. For a four-switch PWM inverter, efforts have also been made in to reduce the dc-bus voltage ripples with a space vector modulation technique under unbalanced ac power supply. In this paper, a model suitable for

the controller design in d-q synchronous frame for four-switch VSRs is derived. This model is developed based on the state space average model of [15], without any prespecified operating condition. The result relies on utilizing a so-called "reduced Park Transformation" on the switching functions. Except a term describing the voltage difference between the two output capacitor voltages, the derived model resembles that of a six-switch VSR. It is also shown that the modulation policy of the closed form controller developed in [15] corresponds to the steady-state control input of a given operating point. As an illustration of the salient performance of the current control approach in rotating d-q frame, the input–output feedback linearization (IOFL) [10], and LPI [3] controller designs are presented. Then following the usual practice, an outer-loop LPI voltage controller cascaded to the d-axis current loop is adopted to cope with the issue of voltage regulation. The performance of the proposed controller designs is validated through computer simulation and hardware experiment. To give a comparison, simulated and experimental results of an a-b-c frame LPI current controller [3] migrated from six-switch VSR are also provided to show the superiority of the proposed designs in synchronous rotating d-q frame.

II. SYSTEM MODELING IN ROTATING d-q FRAME

A. Coordinate Transformation

The Park Transformation converts the three-phase system from a stationary reference frame into synchronously rotating frame with direct, quadrature, and zero-sequence components. In this coordinates, as the d-axis is aligned with the source supply voltage, the unity-power-factor requirement can be achieved by simply regulating the q-axis source current to zero. Park Transformation has some variants. This paper considers the following transformation matrix

$$T = \frac{2}{3} \begin{bmatrix} \cos(\omega t) & \cos\left(\omega t - \frac{2}{3}\pi\right) & \cos\left(\omega t + \frac{2}{3}\pi\right) \\ \sin(\omega t) & \sin\left(\omega t - \frac{2}{3}\pi\right) & \sin\left(\omega t + \frac{2}{3}\pi\right) \\ 0.5 & 0.5 & 0.5 \end{bmatrix} \quad (1)$$

where ωt is the angle determined by the source supply voltage with angular frequency ω.

For describing the d-q frame model of a four-switch VSR, a coordinate transformation, called reduced Park Transformation, resembling to the upper-left square sub-matrix of T, is adopted as follows:

$$T_u^{-1} = \frac{2}{\sqrt{3}} \begin{bmatrix} \sin\left(\omega t + \frac{1}{3}\pi\right) & -\cos\left(\omega t + \frac{1}{3}\pi\right) \\ \sin(\omega t) & -\cos(\omega t) \end{bmatrix} \quad (2)$$

The reduced Park Transformation (3) converts d- and q-axis dc components into two sinusoidal signals with 60◦ out of phase from each other.

B. Modelling in rotating d-q Frame

The schematic diagram of a three-phase four-switch VSR under consideration is shown in Fig. 1. It is assumed that a resistive load RL is connected to the output terminal. Also, the two series-connected output capacitors are identical (i.e., C1 =C2 = C). As demonstrated in [15], assuming that esa + esb +esc = 0 and ia + ib + ic = 0, the a-b-c frame state equations of the four-switch VSR are represent the switching actions for the four switches. Denoting es = [esa esb esc] T, is = [ia ib ic] T, the a-b-c frame model in vector form can be expressed as (3)

$$p_j = \begin{cases} 1, & S_j \quad \text{closed}, \\ -1, & \overline{S}_j \quad \text{closed}, \end{cases} \quad j = a, b \quad (3)$$

$$e_s = L\frac{di_s}{dt} + Ri_s + v_s \quad (4)$$

where

$$v_s = \frac{1}{6}\left(v_{c1}\Lambda\Gamma_1 + v_{c2}\Lambda\Gamma_2\right)$$

Under a balanced three phase ac supply, neglecting the resistance of the power switches, and performing the Park's Transformation matrix T on the both sides of the state equation (11) leads to

$$\Lambda = \begin{bmatrix} 2 & -1 & -1 \\ -1 & 2 & -1 \\ -1 & -1 & 2 \end{bmatrix}, \quad \Gamma_1 = \begin{bmatrix} p_a \\ p_b \\ -1 \end{bmatrix} \text{ and } \Gamma_2 = \begin{bmatrix} p_a \\ p_b \\ 1 \end{bmatrix},$$

$$T\Lambda = 3 \begin{bmatrix} \cos(\omega t) & \cos\left(\omega t - \frac{2}{3}\pi\right) & \cos\left(\omega t + \frac{2}{3}\pi\right) \\ \sin(\omega t) & \sin\left(\omega t - \frac{2}{3}\pi\right) & \sin\left(\omega t + \frac{2}{3}\pi\right) \\ 0 & 0 & 0 \end{bmatrix} \quad (5)$$

the transformed phase-to-neutral voltages in (4) is now simplified to

$$Tv_s = \frac{T}{6}(v_{c1}\Lambda\Gamma_1 + v_{c2}\Lambda\Gamma_2) = \frac{1}{3}\begin{bmatrix} u_d v_o + v_{cd} \\ u_q v_o + v_{cq} \\ 0 \end{bmatrix} \quad (6)$$

Denote the transformed variables [id iq 0] T= Tis and [Em 0 0] T= Test, withEm being the amplitude of the phase voltage. Substituting (6) into (4), the current dynamics of the four-switch VSR in the rotating d-q frame is obtained as

$$E_m = L\frac{di_d}{dt} + Ri_d + \omega Li_q + \frac{1}{3}v_o u_d + \frac{1}{3}v_{cd} \quad (7)$$

The expressions of the dc-bus voltage dynamics in the rotating d-q frame may be derived as follows. Applying the Park's Transformation to the a-b-c frame state equations.

we have

$$\dot{v}_{c1} = \frac{1}{2C}(\gamma_{11}i_d + \gamma_{12}i_q) - \frac{1}{R_L C}v_{c1} - \frac{1}{R_L C}v_{c2} \quad (8)$$

$$\dot{v}_{c2} = \frac{1}{2C}(\gamma_{21}i_d + \gamma_{22}i_q) - \frac{1}{R_L C}v_{c1} - \frac{1}{R_L C}v_{c2} \quad (9)$$

As the two dc-bus capacitors are identical and vo= vc1 + vc2, the output voltage (8), (9) may be combined to a single one

$$\dot{v}_o = \frac{1}{2C}[(\gamma_{11} + \gamma_{21})i_d + (\gamma_{12} + \gamma_{22})i_q] - \frac{2}{R_L C}v_o. \quad (10)$$

Applying (4) to (9) again, and rearranging (6), the complete d−q frame model of the four-switch VSR is

$$\frac{di_d}{dt} = -\frac{R}{L}i_d - \omega i_q - \frac{1}{3L}v_o u_d - \frac{1}{3L}v_{cd} + \frac{E_m}{L} \quad (11)$$

$$\frac{di_q}{dt} = \omega i_d - \frac{R}{L}i_q - \frac{1}{3L}v_o u_q - \frac{1}{3L}v_{cq} \quad (12)$$

$$\dot{v}_o = \frac{1}{C}(u_d i_d + u_q i_q) - \frac{2}{R_L C}v_o. \quad (13)$$

Remark 1: The d-q frame model derived in [15] assuming that the VSR operates at steady state and vc1 = vc2 = (1/2) vo. It can be checked that in the derivation of the state-space model (11)–(13), no such assumptions are made. Therefore, the derived

state equations provide a mathematical model more suitable for controller design. As compared to the d-q frame model for a six-switch VSR [5], [7], [8], the capacitor voltage difference terms vcd and vcq are unique to the four-switch VSR. Accordingly, when there is no difference between capacitor voltages vc1 and vc2, vcd and vcq vanish, and the d-q frame model (11)–(13), is almost identical to that of a six-switch VSR. As using two identical capacitors in the capacitor bank, it is reasonable to assume that vc1 is equal to vc2 if the imperfection of the capacitors is ignored. Then, a wealth of analytical and control methods for the six-switch VSR may be directly applied to the four-switch VSR.

C. Steady-State Solution

The d-q frame model derived in Section II for four-switch VSRs is a two-input nonlinear system. With a resistive load RL connected at dc output, as dc-bus voltage vo reaches a given desired setting Vo∗with a unity power factor, the steady-state solution may be found as follows.

The switching functions in d-q frame at steady state may be transformed back into a-b-c frame by the inverse reduced Park Transformation (3), i.e.,

$$\begin{bmatrix} \bar{p}_a \\ \bar{p}_b \end{bmatrix} = \frac{2}{\sqrt{3}} \begin{bmatrix} \sin(\omega t + \frac{2}{3}\pi) & -\cos(\omega t + \frac{2}{3}\pi) \\ \sin(\omega t) & -\cos(\omega t) \end{bmatrix} \begin{bmatrix} \bar{u}_d \\ \bar{u}_q \end{bmatrix} \quad (1$$
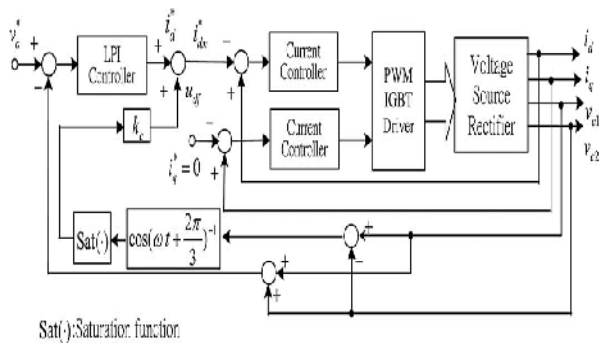

Fig. 2. Block diagram of the overall control system for control in d-q frame.

It can then be checked that the steady-state switching functions are the modulation policies of the closed-fromcontroller proposed in on the other hand, the steady-state d-axis source current may be solved as

$$I_d^* = \frac{1}{2}\left[\frac{E_m}{R} \pm \sqrt{\left(\frac{E_m}{R}\right)^2 - \frac{8(V_o^*)^2}{3R_L R}} \right]. \quad (15)$$

In, it has been shown that the larger solution in

isnot a stable equilibrium point and hence not feasible.

Remark 2: When there is a failure of one bridge arm of a six-switch VSR, a practical application of this topology is to recover the functionality of the six-switch VSR with split dc link capacitors. In this situation, under the condition that the ac supply and dc load remain unchanged, the delivered power of this simplified VSR will increase since the lower output voltage bound of the four-switch VSR is normally much higher than that of a six-switch VSR. Typically, the lower output voltage bound of the four-switch VSR is increased by 173.2%. Thus, the simplified VSR will deliver power triple as much as that of the original six-switch PWM VSR.

III. CURRENT CONTROLLER DESIGNS

The expressions indicate that the dynamics of a four-switch VSR are nonlinear and bear a resemblance to that of a six-switch VSR. In fact, when vc1 = vc2, they are almost identical. Thus, many existing control strategies (for example, see may be adopted to design a controller that could exhibit satisfactory performance. Due to the non minimum phase property, the control of VSRs is usually accomplished in a cascaded structure as shown in Fig. 2. The inner loop performs current control and the outer-loop voltage controller generates a current reference for the inner current loops. To show the effectiveness of the current controller design in d-q frame, this section describes two current controller designs for four-switch VSRs, based on the d-q frame model derived in the previous section.

A. IOFL

The IOFL provides an effective means to transforming the original system into a linear one under which a regular linear controller design can be applied. In [10], the author has given a thorough analysis on the geometric properties of the six-switch VSR and discovered that the so-called voltage control, with output variables chosen to be vo and iq , leads to a non minimum phase system, and thus not feasible. Instead, the feedback linearization is considered for the d- and q-axis current dynamics.

$$\begin{bmatrix} u_d \\ u_q \end{bmatrix} = \begin{bmatrix} -\frac{1}{3L}v_o & 0 \\ 0 & -\frac{1}{3L}v_o \end{bmatrix}^{-1} \left(\begin{bmatrix} \frac{R}{L}i_d + \omega i_q - \frac{E_m}{L} \\ -\omega i_d + \frac{R}{L}i_q \end{bmatrix} + \alpha \right) \quad (16)$$

The d-axis reference i∗d will be supplied by the outer voltage loop as described in the following section, whereas the q-axis reference i∗q allows the adjustment of power factor. Obviously, the control

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inputs render the current loops be exponentially stable error dynamics. With a substitution of the current control laws into, the internal dynamics may be derived. Similar to the case of six-switch VSRs (see Section III-B of [10]), when the current tracking errors εd and εq approach zero, the zero dynamics may be shown to be stable.

2) Analysis of the Capacitor Voltage Difference Dynamics: By following the analysis in, it can be deduced that the voltage imbalance caused by the initial conditions asymptotically approaches zero with a settling time 4C/kc. Since in the steady state, the d-axis current id will eventually converge toi∗dm. Thus, a larger value of kc will lead to a faster settling time at the price of inducing a larger vibration in d-axis current. **Remark 3**: The compensating term udf in has singular points at ωt = 1/6(4 ± 3n) π, which will render the modified d-axis reference i∗dm be extremely large at these points. This undesired situation may be avoided by placing a limit on the value calculated from the inverse of the cosine functioncos (ωt + (2/3π)).

B. Linear PI Control This scheme employs LPI controllers for both the d- andq-axis current loops [3]. The control policy is generating the modulating signal by performing proportional and integral operation on current tracking error. This method is simple and easy to be analogously or digitally implemented. The magnitude of the d-axis current reference i∗d is provided by the outer voltage loop.

The current controllers may be expressed as

$$u_d = k_{pd}(i_d - i_d^*) + k_{id} \int (i_d - i_d^*)dt \qquad (17)$$
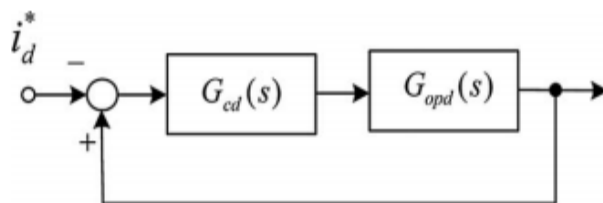

Fig. 3. Block diagram of the closed-loop system for the d-axis current loop with LPI controller.

of the d- and q-axis current loops may be expressed as

$$G_{opj}(s) = \frac{I_j(s)}{U_j(s)} = \frac{-V_o^*/(3L)}{s + (R/L)}, \qquad j = d,q. \quad (18)$$

where Ej(s) represents the Laplace transform of εj (t). With the LPI controller (50), the block diagram of the closed-loop system for the d-axis loop is shown in Fig. 3. The q-axis loop is also with the same control structure and thus omitted here. It can be checked that the resulting closed-loop system is not a standard second-order system. According to] and our simulation study, the presence of the zero at s = −kij/kpj increases the bandwidth of the closed-loop system. In fact, it is discovered that as the location of the zero moves close to the origin, a higher bandwidth is achieved. This can be used as a guideline in choosing the ratio of the controller parameters. Then, the proportional gain is selected so that the open loop has an adequate bandwidth (about one-tenth of the switching frequency for good transient response.

IV. ANALYSIS OF THE EFFECT OF DISTORTED AC SUPPLY ON LINE CURRENTS

The salient performances of the proposed d-q frame current controllers are guaranteed under ideal ac supply. However, in the industrial power distribution system, harmonics distortion in supply voltage is not uncommon. Typically, the fifth- and the seventh-order harmonics are dominant component sin voltage. According to the analysis given in the effect of supply voltage distortion on line currents is analysed as follows.
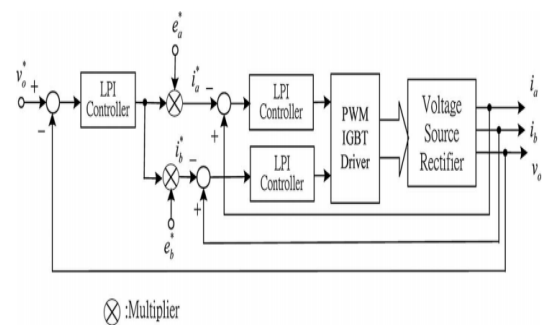

Fig. 4. Block diagram of the cascaded control system for control in an a-b-c frame.

V. INDUCTION MOTOR

The induction motor speed variation can be easily achieved for a short range by either stator voltage control or rotor resistance control. But both of these schemes result in very low efficiencies at lower speeds. The most efficient scheme for speed control of induction motor is by varying supply frequency. This not only results in scheme with

wide speed range but also improves the starting performance. Synchronous speed of Induction Motor is directly proportional to the supply frequency. Hence, by changing the frequency, the synchronous speed and the motor speed can be controlled below and above the normal full load speed. If the machine is operating at speed below base speed, then v/f ratio is to be kept constant so that flux remains constant. This retains the torque capability of the machine at the same value. But at lower frequencies, the torque capability decrease and this drop in torque has to be compensated for increasing the applied voltage. Any reduction in the supply frequency without a change in the terminal voltage causes an increase in the air gap flux. Induction motors are designed to operate at the knee point of the magnetization characteristic to make full use of the magnetic material. Therefore the increase in flux will saturate the motor. This will increase the magnetizing current, distort the line current and voltage, increase the core loss and the stator copper loss, and produce a high pitch acoustic noise. While any increase in flux beyond rated value is undesirable from the consideration of saturation effects, a decrease in flux is also avoided to retain the torque capability of the motor. Therefore, the variable frequency control below the rated frequency is generally carried out

By reducing the machine phase voltage, V, along with the frequency in such a manner that the flux is maintained constant. Above the rated frequency, the motor is operated at a constant voltage because of the limitation imposed by stator insulation or by supply voltage limitations.

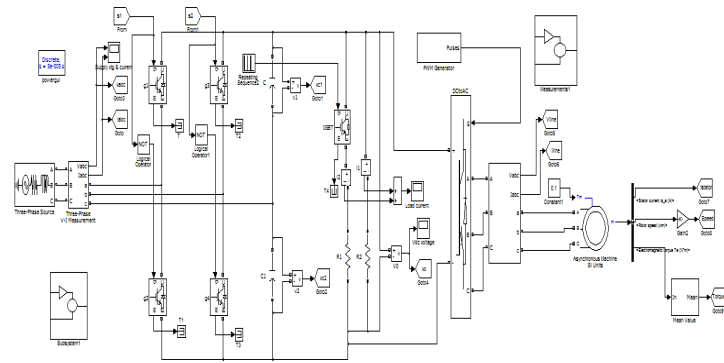## VI .MATLAB/SIMULINK RESULTS

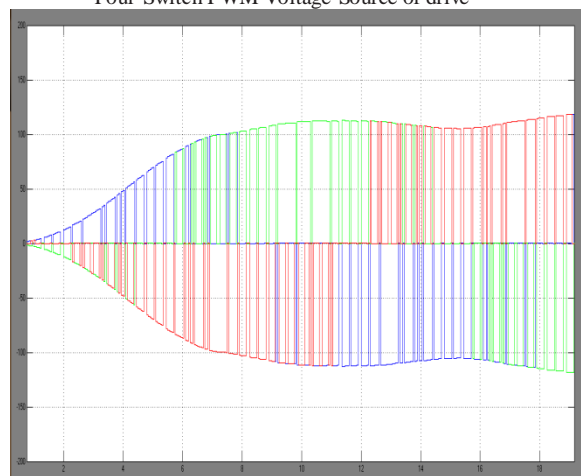Fig.5. Mat lab/Simulink modelling of proposed Three-Phase Four-Switch PWM Voltage-Source of drive
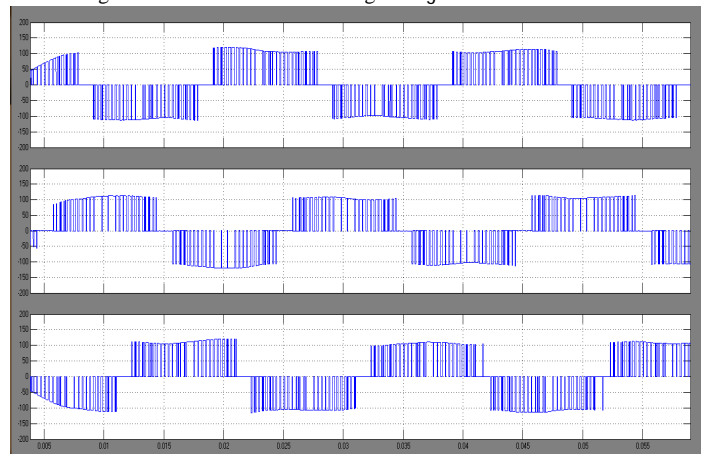

Fig .6 Matlab/Simulink Modelling Voltage line

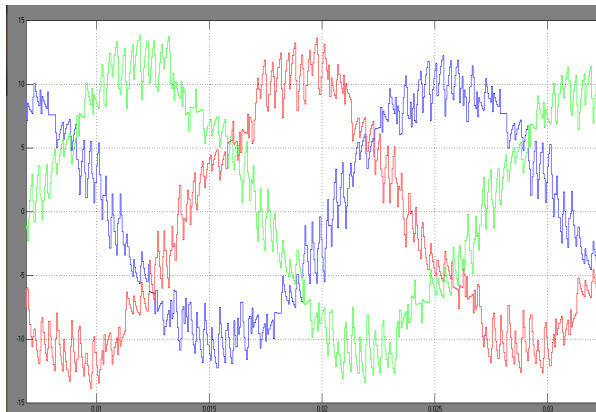

Fig .7 Matlab/Simulink Modelling lineVoltage in extension
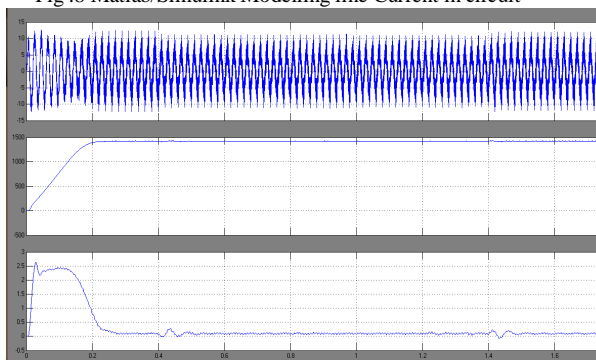
Fig .8 Matlab/Simulink Modelling line Current in circuit

Fig .9 Matlab/Simulink Modelling of Speed, torque and current for IM drive

VII. CONCLUSION

Controller designs in rotating d-q frame have been popular for six-switch VSRs in recent decades. For four-switch VSRs, this approach has not been received much attention, partly because it lacks of a precise model in the rotating d-q frame coordinates. By using a reduced Park Transformation on switching functions, this paper has derived a d-q frame model for a four-switch VSR, which bears a strong resemblance to that of a six-switch VSR. Thus, many existing control strategies for six-switch VSRs are readily applicable to four-switch VSRs. As a demonstration,the IOFL and LPI-DQ current controllers are designed to provide unity-power-factor operation, and verified through computer simulation and hardware experiment. Responses of a classical LPI-SF current controller in a b-c frame are also included as a comparison. The simulation and experimental results are in close agreement. The advantage of control in d-q frame is clearly demonstrated from the measured data. The LPI-SF current controller yields unbalanced line currents, larger dc-bus voltage ripples, and a nonzero phase tracking error. The LPI-DQ current controller delivers nearly sinusoidal and balanced line currents, and small dc-

bus voltage ripple, yet coupling between d- and q-axis current dynamics exists. Induction Motor drive is application and study characteristics of IM drive of speed, torque and current wave forms.

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