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Modular Multilevel DC/DC Converters with Phase-Shift Control Scheme for HVDC based system with Closed loop Control

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Abstract-In this paper, by investigating the topology derivation principle of the phase-shift-controlled three-level dc/dc converters, the modular multilevel dc/dc converters, by integrating the full-bridge converters and three-level flying capacitor circuit, are pro-posed for the high step-down and high power dc-based systems. The high switch voltage stress in the primary side is effectively reduced by the full-bridge modules in series. Therefore, the low-voltage-rated power devices can be employed to obtain the benefits of low conduction losses. More importantly, the voltage auto balance ability among the cascaded modules is achieved by the inherent flying capacitor, which removes the additional possible active components or control loops. In addition, zero-voltage-switching performance for all the active switches can be provided due to the phase-shift control scheme, which can reduce the switching losses. The circuit operation and converter performance are analyzed in detail. Finally, the performance of the presented converter is verified by the simulation and experimental results from a 2-kW prototype. The proposed concept is implemented with closed loop control to attain desired voltage using MATLAB/SIMULINK software.

Index Terms—Input voltage auto balance, modular multilevel dc/dc converter, phase-shift control scheme, zero-voltage switching (ZVS).

I. INTRODUCTION

In recent years a dc to dc converter with high performance is needed for HVDC(High Voltage Direct Current) based systems such as fuel cell power systems and distributed power systems[1-2].Conventional dc to dc converter is not suitable for such applications due to lack of commercial high voltage high performance power MOSFETS. For instance a typical railway system is considered. They are provided by DC transmission lines with voltage levels of 600,750,1500 or 3000v.This high voltage is inverted to 440v, and further rectified to 110v dc for batteries. This 110v dc is again stepped down to 72v,48v,36v and 24v for auxiliary equipments. This multiple conversion stages of voltage leads to low conversion efficiency. An attempt has been made to step down voltage at high switching frequency in single step to improve conversion efficiency .Insulated Gate Bipolar Transistors(IGBTs) and metal Oxide Semiconductor FETS(MOSFETS) are dominantly used switches for medium voltage or high voltage applications.If only high input voltage is a factor , IGBTs are preferred as they have high blocking voltage capability but it limits to only low switching frequency which is an obstacle to achieve high power density. MOSFETS are the unique selection for high switching frequency operation. Though 4000v rated mosfets available they have high ON resistance which results in conduction losses. So in order to achieve high performance converter an attempt has been made to derive advanced converter topologies. To reduce voltage stresses on the devices ISOP(Input Series Output Parallel) converters was proposed in [3]. Many converter topologies are discussed in [4-8] to reduce switch voltage stresses. But the conversion efficiency is unfortunately affected because of hard switching operation of above proposed converters. Another converter has been proposed in [9] which uses snubber circuit to achieve ZVS, of course voltage balance is achieved by external closed loop circuits which increases the complexity of circuit.

In this paper, the flying capacitor and full-bridge converters are combined and integrated to derive the advanced modular multilevel dc/dc converters for the high step-down and high power dc-based conversion applications. Due to the charging and discharging balance of the built-in flying capacitor, the input voltage auto balance ability is naturally realized, and overcomes the input voltage imbalance. Furthermore, the phase-shift control strategy can be used to achieve the soft-switching operation and reduce the switching losses. The concept of modular multilevel dc/dc converters may provide a clear picture on high-voltage dc/dc topologies for the dc-based distribution and micro grid systems.

II. DERIVATION LAW OF MODULAR MULTILEVEL CONVERTERS

The derivation process of the proposed modular multilevel dc/dc converters is discussed in this section. It

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is well known that the neutral-point-clamped (NPC) converters and flying capacitor-based converters are the major multilevel topologies for the high-voltage and high-power applications[10]. For the conventional NPC converters with pulse width modulation control, the abnormal operation condition, such as the mismatch in the gate signals, may cause the voltage imbalance of the input capacitors. Therefore, the converter reliability is impacted. Furthermore, the phase-shift control scheme is not suitable for the conventional NPC converters, which leads to large switching losses. Fortunately, by inserting a small flying capacitor parallel connected with the clamping diodes, the input capacitor voltages are automatically shared because the flying capacitor can be directly parallel with the series input capacitors alternatively[11].

More importantly, the phase-shift control strategy can be easily applied to achieve zero-voltage-switching (ZVS) operation without adding any other power components. The phase-shift controlled three-level dc/dc converter is plotted in Fig. 1(c). From another point of view, the phase-shift-controlled TLC can be regarded as the combination and integration of the three-level NPC converter as given in Fig. 1(a) and the three-level flying capacitor-based circuit as shown in Fig. 1(b), where the input capacitors and active power switches are reused and shared to reduce the circuit complexity. As a result, the advantages of the NPC converter and flying capacitor-based circuit are kept whereas their inherent disadvantages are effectively avoided. Many further improvements are made for the combined phase shift-controlled TLC by adding some active or passive components to extend the soft-switching operation range[12-15].

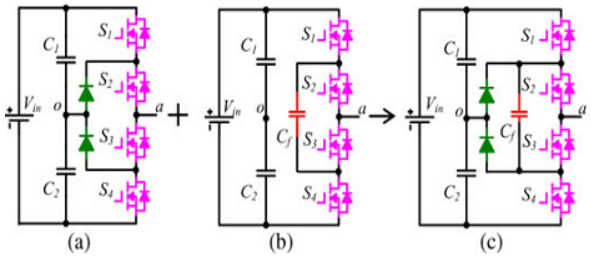

Fig.1. Derivation of novel TLC: (a) NPC TLC, (b) flying capacitor-based TLC, and (c) phase-shift-controlled combined TLC.

Based on the previously summarized combined multilevel derivation principle, it is innovative and attractive to consider the possibility of combination of the other fundamental multilevel topologies. For example, the cascaded full-bridge converter, or the ISOP full-bridge converter, and the three-level flying capacitor-based converter are combined and integrated to derive the advanced modular multilevel dc/dc converters, which is detailed illustrated in Fig. 2. The time sequence of the leading leg in the phase-shift-controlled full-bridge converters is kept constant and only the phase of the lagging leg is shifted to regulate the output voltage. This indicates that the leading legs of the cascaded full-bridge converter can be assembled with the three-level flying capacitor-based converter to achieve the input voltage auto balance. And the lagging legs of the cascaded full bridge converter are still kept unchanged to provide adequate control freedom to achieve fast and accurate output voltage regulation.

Consequently, for the proposed modular multilevel dc/dc converters, the big concern of the input-voltage imbalance existed in the ISOP converters is completely overcome due to the built-in flying capacitor. More importantly, the derived modular multilevel dc/dc concept can be easily put forward to N-stage converters by stacking the full-bridge power modules in series in the primary side to satisfy the growing bus voltage in the dc-based distribution and micro grid systems. In view of the phase-shift-controlled topologies, the aforementioned optimized strategies for the phase-shifted-controlled TLCs can be directly transferred to the derived modular multilevel dc/dc converters to generate a family of high performance topologies for the high-voltage and high-power applications. It can be concluded that this modular multilevel converter concept is one of the general solutions for the high-voltage and high-power dc/dc topology origination.

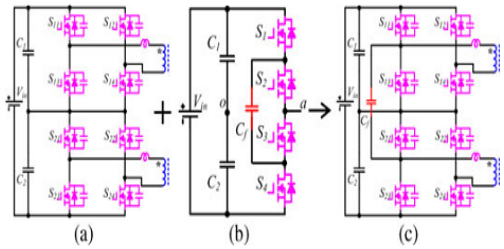

Fig.2. Derivation of the proposed modular multilevel dc/dc converter: (a) cascaded full-bridge converter, (b) flying capacitor-based TLC, and (c) proposed modular multilevel dc/dc topology

III. OPERATION PRINCIPLE AND INPUT VOLTAGE AUTOBALANCE MECHANISM

For the secondary side of the derived modular multilevel dc/dc converters, the current-type full-wave rectifier, full-bridge rectifier, current doubler rectifier, and other advanced current-type rectifiers can be employed. In this section, the widely adopted current-type full-wave

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rectifier is applied as an example to explore the circuit performance of the proposed modular multilevel configuration, which is illustrated in Fig. 3. In the primary side, the capacitors $C_1$and $C_2$are used to split the high input voltage, S_{11}–$S_{14}$are the power switches of the top full-bridge module, S_{21}–S_{24}form the bottom full-bridge module,C_{s11}–$C_{s24}$are the parasitic capacitors of the power switches, and $L_{lk1}$and L_{lk2} are the leakage inductors of the transformers T1andT_2, respectively. In the secondary side, D_{o11}, D_{o12}, L_{f1}, and C_{o1} are for the top full-bridge module and D_{o21}, D_{o22}, L_{f2}, and C_{o2} are for the bottom full-bridge module. i_{p1}, i_{p2}, i_{Do11}, i_{Do12}, i_{Do21}, and $i_{Do22}$are the primary and secondary currents through the windings of the transformers with the defined direction in Fig. 3. And $i_{s1}$and i_{s2} are the filter inductors currents.

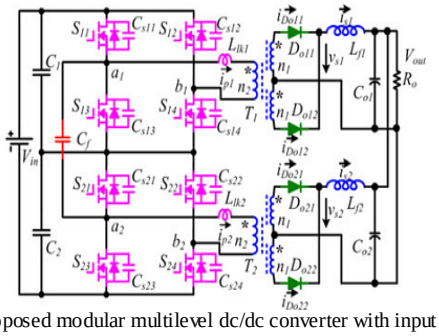

Fig.3. Proposed modular multilevel dc/dc converter with input voltage auto balance ability.

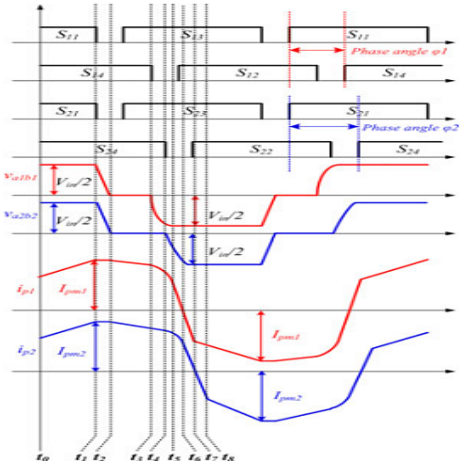

Fig.4. Key waveforms of the proposed converter.

A. Operation Analysis

The phase-shift control scheme is employed in the proposed converter to realize the ZVS performance of all the power switches, where S_{11},S_{13},S_{21}, and S_{23} are the leading-leg switches and S_{12},S_{14},S_{22}, and S_{24} are the lagging-leg switches. The key waveforms of the proposed converter are shown in Fig. 4. For the top full-bridge module,S_{11} andS_{13} act with 0.5 duty cycle complementarily with proper dead time td, so as for the switches S_{12} andS_{14}. The phase-shift angle between the leading and lagging switch pairs is defined as ϕ_1.

The gate signal pattern of the bottom full-bridge module is similar to that of the top full-bridge module with the phase-shift angle ϕ_2. Meanwhile, the leading switches pair S_{11} andS_{13} turns ON and OFF simultaneously with the switch pair S_{21} andS_{23}, while the phase-shift angles ϕ_1 and ϕ_2 are decoupled control freedoms for the output voltage regulation.

The mode 0 <ϕ_1–ϕ_2 <t_d is taken into consideration when analyzing the operation of the converter, and the equivalent operation circuits are depicted in Fig. 5. In order to simplify the analysis, the following assumptions are made: 1) all the power switches and diodes are ideal; 2) the parasitic capacitorsC_{s11}–$C_{s24}$of the switches have the same value as Cs; 3) the voltage ripples on the divided input capacitorsC_1,C_2 and flying capacitors C_f are small due to their large capacitance; 4) the turns ratio of both transformers is N= n_2:n_1; and 5) the input voltage is balanced. There are 15 operation stages in one switching period. Due to the symmetrical circuit structure and operation, only the first eight stages are analyzed as follows.

Stage 1 [t_0,t_1]:Before t_1, the switches S_{11},S_{14},S_{21}, and $S_{24}$are in the turn-on state to deliver the power to the secondary side. The output diodesD_{o11} andD_{o21} are conducted and the output diodesD_{o12} andD_{o22} are reverse biased. The flying capacitor C_f is in parallel with the input divided capacitor C_1 to make V_{Cf} equal toV_{C1}.

$$i_{p1}(t) = i_{p1}(t_o) + \frac{\frac{V_{in}}{2} - NV_{out}}{L_{lk1} + N^2 L_{f1}} (t - t_o) \quad (1)$$

$$i_{p2}(t) = i_{p2}(t_0) + \frac{\frac{V_{in}}{2} - NV_{out}}{L_{lk2} + N^2 L_{f2}} (t - t_o) \quad (2)$$

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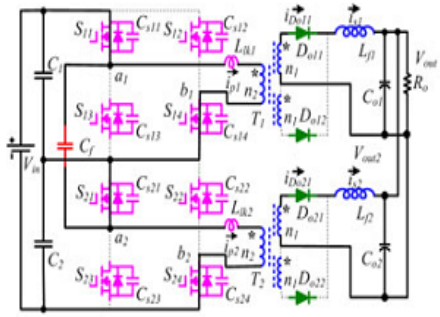
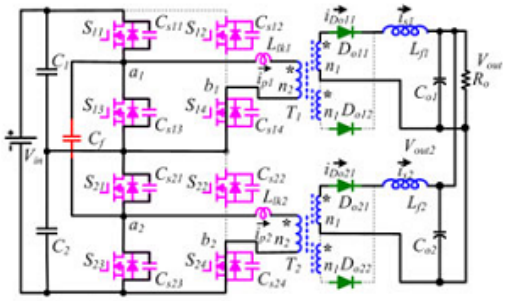


(Stage 1) [t_0-t_1]

Stage 2 [t_1,t_2]:At t_1, the turn-off signals of the switches $S_{11}$and $S_{21}$are given. ZVS turn off for these two switches are achieved due to the capacitors C_{s11} andC_{s21}. C_{s11} andC_{s21} are charged andC_{s13} andC_{s23} are discharged by the primary currents.

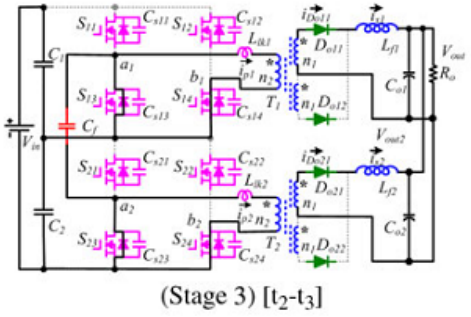


(Stage 2) [t_1-t_2]

Stage 3[t_2,t_3]: At t_2, the voltages of C_{s13} andC_{s23} reach 0 and the body diodes of$S_{13}$and$S_{23}$are conducted, providing the ZVS turn-on condition forS_{13}andS_{23}. The flying capacitor C_f is changed to be in parallel with the input divided capacitor C_2. The primary currents are derived by

$$i_{p1}(t) = \frac{i_{s1}(t)}{N} \quad (3)$$

$$i_{p2}(t) = \frac{i_{s2}(t)}{N} \quad (4)$$

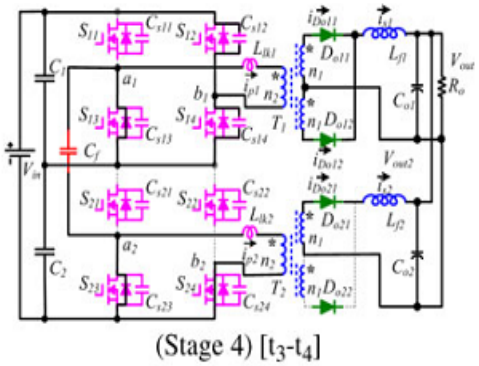


(Stage 3) [t_2-t_3]

Stage4[t_3,t_4]:At t_3,S_{14}turns off with ZVS.$C_{s14}$is charged andC_{s12} is discharged, leading to the forward bias of D_{o12}; hence, the secondary currenti_{s1} circulates freely through both D_{o11}andD_{o12}. $i_{p1}$is regulated by

$$i_{p1}(t) = i_{p1}(t_3)\cos\omega(t - t_3) \quad (5)$$

$$\omega = \frac{1}{\sqrt{2L_{IK2}C_S}} \quad (6)$$



(Stage 4) [t_3-t_4]

Stage 5 [t_4,t_5]:At t_4, the turn-off signal ofS_{24}comes. ZVS turn-off performance is achieved forS_{24}. Similar to the previous time interval, D_{o21} and D_{o22} conduct simultaneously, thus leading to the transformer T_2 short-circuit. i_{p2} is regulated by

$$i_{p2}(t) = i_{p2}(t_4)\cos\omega(t - t_3) \quad (7)$$

$$\omega = \frac{1}{\sqrt{2L_{lk2}C_s}} \quad (8)$$

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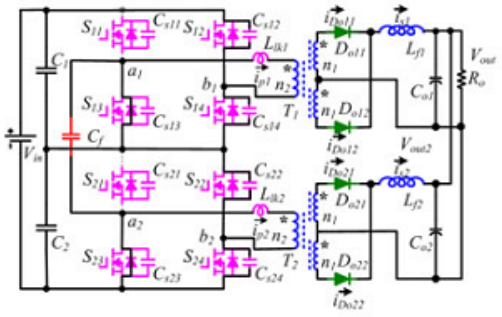
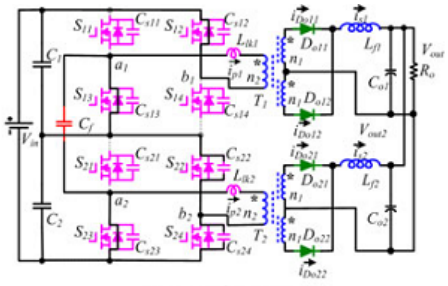


(Stage 5) [t_4-t_5]

Stage 6 [t_5,t_6]: At t_5, C_{s12} is discharged completely and the anti parallel diode of S_{12} conducts, getting ready for the ZVS Turn-on of S_{12}. During this time interval, i_{p1} declines steeply duo to half-input voltage across the leakage inductor L_{lk1}, i_{p1} is given by

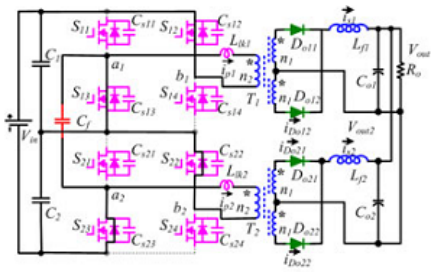
$$i_{p1}(t) = i_{p1}(t_5) - \frac{\frac{V_{in}}{2}}{L_{lk1}}(t - t_5) \qquad (9)$$



(Stage 6) [t_5-t_6]

Stage 7 [t_6,t_7]: At t_6, i_{p1} decreases to 0 and increases reversely with the same slope through S_{12} and S_{13}. C_{s22} is discharged completely and the anti parallel diode of S22 conducts. i_{p2} declines rapidly duo to half-input voltage across the leakage inductor L_{lk2}. i_{p2} is given by

$$i_{p2}(t) = i_{p2}(t_6) - \frac{\frac{V_{in}}{2}}{L_{lk2}}(t - t_6) \qquad (10)$$



(Stage 7) [t_6-t_7]

Stage 8 [t_7,t_8]: At t_7, i_{p2} decreases to 0 and increases reversely through S_{22} and S_{23}. The current through the output diode D_{o11} decreases to 0 and turns off. The output diode D_{o21} turns off after t_8, and then a similar operation works in the rest stages.

B. Input Voltage Auto balance Mechanism

The input voltage imbalance is one of the major drawbacks for most multilevel converters and ISOP converters, which is mainly caused by the asymmetry of the component parameter difference and the mismatch of control signals. It has been carried out that the transformer turns ratio difference (N), leakage inductance distinction (L_{lk}), and phase-shift angle mismatch (ϕ) are the main reasons for the input voltage imbalance in the steady state for the ISOP phase-shift-controlled converters

The input voltage auto balance mechanism of the proposed modular multilevel dc/dc converter is displayed in Fig. 6 and detailed elaborated as follows. According to the steady operation of the proposed converter, for the leading-leg switches, the switches S11 and S21 have the same time sequence and the switches S13 and S23 are operated synchronously. When S_{11} and S_{21} are turned ON, S_{13} and S_{23} are turned OFF accordingly, and the flying capacitor Cf is connected in parallel with the top input capacitor C_1 as plotted in Fig. 5(a). This makes V_{Cf} equal to V_{c1}. In the same way, as given in Fig. 5(b), the flying capacitor C_f is in parallel with the bottom input capacitor C_2, when S_{13} and S_{23} are in turn-on state. This denotes that V_{Cf} and V_{c2} are the same. The connection of Cf with C_1 or C_2 alternates with high switching frequency, which leads to the voltages on both the input capacitors automatically shared and balanced.

It is important to point out that the flying capacitor does not connect with the lagging-leg switches directly. As a result, the operation of C_f hardly affects the states of the lagging-leg switches

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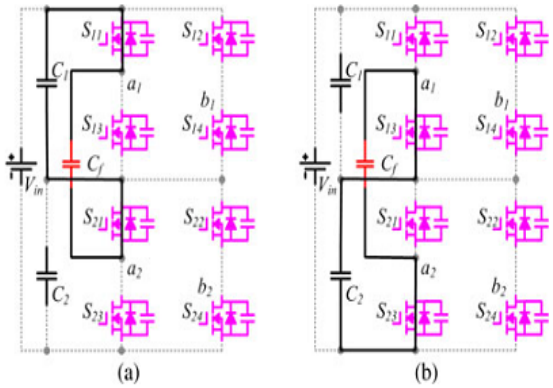

Fig.5. Input voltage auto balance mechanism: (a) C_f in parallel with C_1 and (b) C_f in parallel with C_2

IV. CONVERTER PERFORMANCE ANALYSIS

A. Voltage Stresses of Switches

In the primary side, the voltage stress of the power switches S_{11}–S_{24} is half of the input voltage owing to the series structure and the auto balance mechanism. As a result, the low voltage-rated power devices are available in the high input applications to restrict the conduction losses.

B. ZVS Soft-Switching Condition

1) Leading Legs: ZVS turn-off is achieved for the leading switches due to their intrinsic capacitors. In order to realize ZVS turn-on, enough energy is needed to charge and discharge the intrinsic capacitors. During the dead time interval [t1–t2], S_{11} and S_{21} are turned OFF; C_{s11} and C_{s21} are charged and C_{s13} and C_{s23} are discharged as shown in Fig. 5. According to the Kirchoffs law, the following equations are derived:

$$i_{Cs11} + i_{Cs13} = i_{p1} - i_{Cf} \quad (11)$$

$$i_{Cs21} + i_{Cs23} = i_{p2} + i_{Cf} \quad (12)$$

It is reasonable to assume that i_{p1} and i_{p2} are nearly constant during this period due to the short dead time. When the sum of VC_{s13} and VC_{s21} is not equal to V_{Cf}, C_f may be charged or discharged. The current iCf affects the ZVS performance of the power switches according to (11) and (12): 1) when C_f is discharged, i_{Cf} flows in the positive direction, and ZVS performance of S_{21} and S_{23} is improved but deteriorated for S_{11} and S_{13}; and 2) when C_f is charged, i_{Cf} flows reversely, which improves the ZVS performance of S_{11} and S_{13} but deteriorates that of S_{21} and S_{23}. Fortunately, C_f is much larger than Cs, making i_{Cf} small. Besides, the output filter inductance is reflected to the primary side and is in series with the resonant inductance. The energy of both the filter inductors and the resonant inductors is sufficient to achieve ZVS for the leading switches. The output filter inductance is so large enough that the leading switches can realize ZVS turn-on even at light loads.

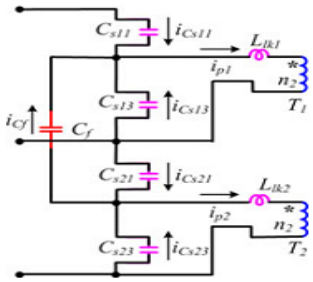

Fig. 6. ZVS equivalent circuit of leading switches during dead time

2) Lagging Legs: Similar with the leading switches, the lagging switches are able to realize ZVS turn-off by utilizing their intrinsic capacitors. However, only the energies of the resonant inductors are employed to achieve ZVS turn-on for the lagging switches

As the resonant inductance is quite smaller than the filter inductance, the achievement of the ZVS turn-on for the lagging switches is more difficult than the leading switches at light loads.

C. Duty Cycle Loss

During interval [t_3–t_7], V_{a1b1} is negative, and ip1 transits from the positive direction to the negative reflected filter inductance current. The secondary diodes D_{o11} and D_{o12} conduct simultaneously, making the secondary rectified voltage become 0. The duty cycle is lost during this time interval, the expression of which is derived by:

$$D_{loss1} = \frac{2(t_7 - t_3)}{T_s} \approx \frac{L_{lk1} I_{o1}}{N V_{in}} \quad (13)$$

For the bottom full-bridge module, the duty cycle loss is similar to the top full-bridge module as given by

$$D_{loss2} = \frac{2(t_8 - t_4)}{T_s} \approx \frac{L_{lk2} I_{o2}}{N V\_in} \quad (14)$$

V. SIMULATION RESULTS

The proposed converter is simulated using Matlab software and the results are presented below:

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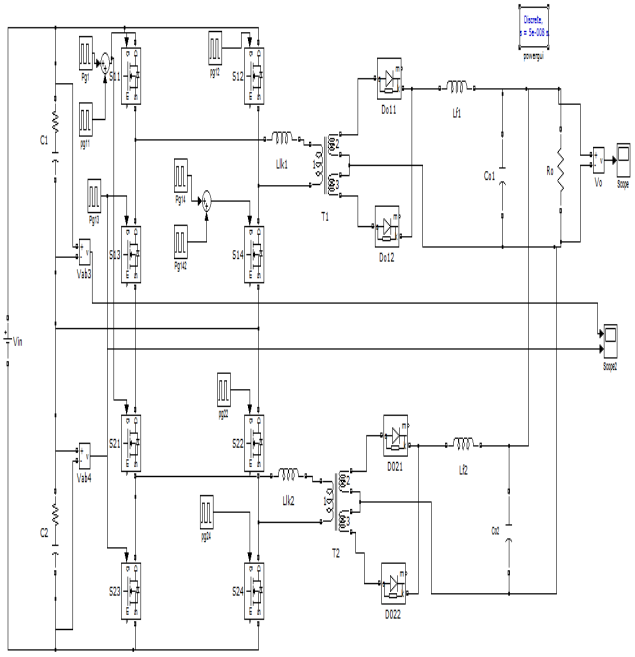

Fig.7. Matlab/Simulink circuit of proposed system without flying capacitor

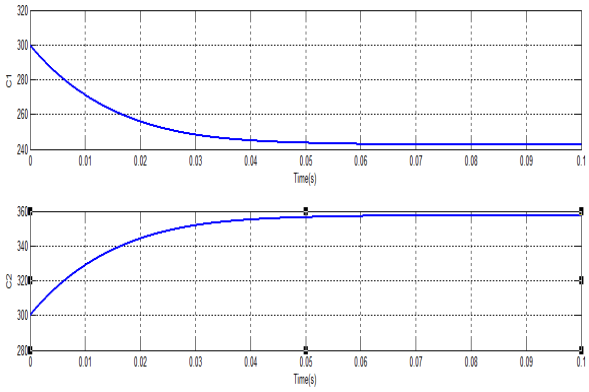

Fig.8.simulation waveform of capacitor voltages without flying capacitor.

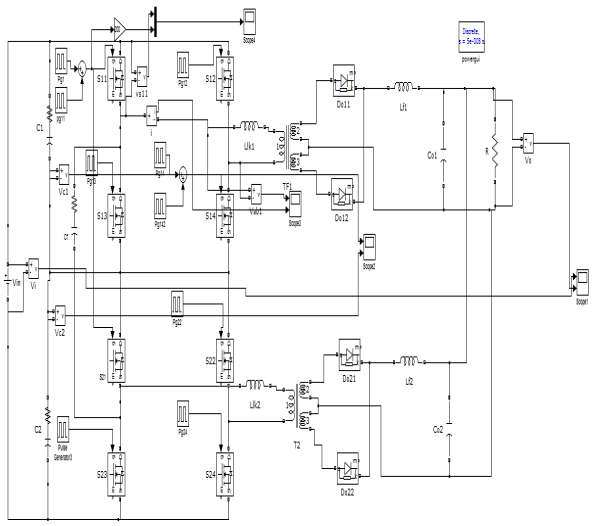

Fig.9.Matlab/Simulink circuit of proposed system with flying capacitor.

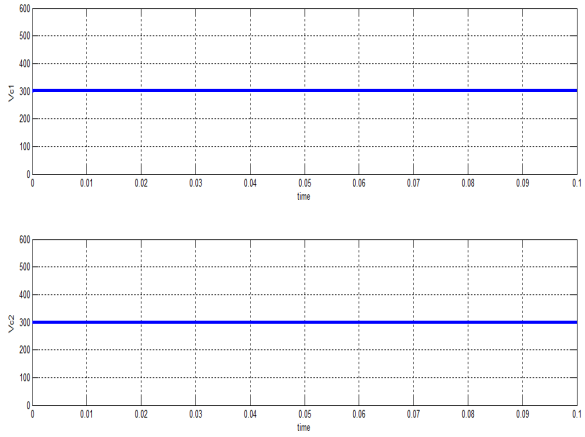

Fig.10. simulation waveform of capacitor voltages with flying capacitor

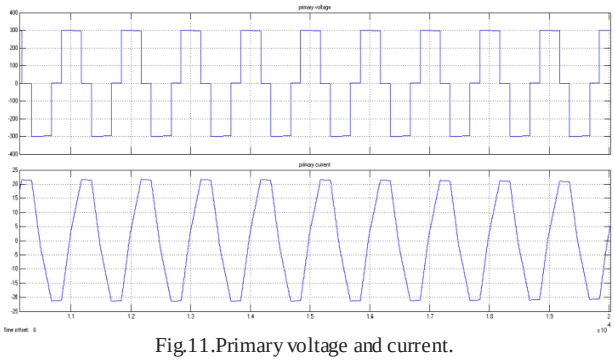

Fig.11.Primary voltage and current.

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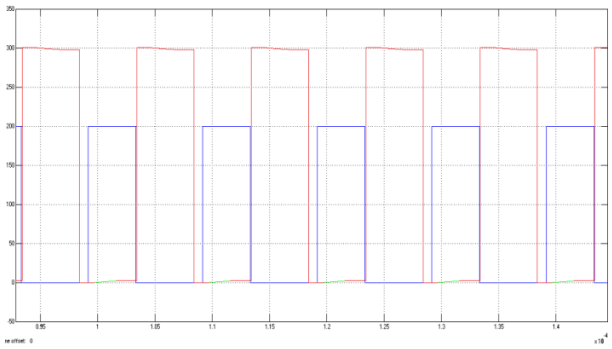


Fig.12. simulation results of ZVS performance of switches.

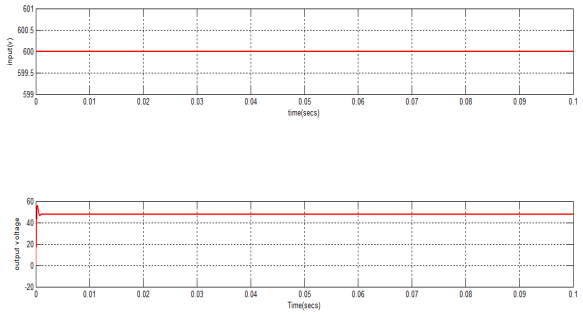


Fig.13.simulation waveform of proposed system input voltage(600v) and output voltage(48v)

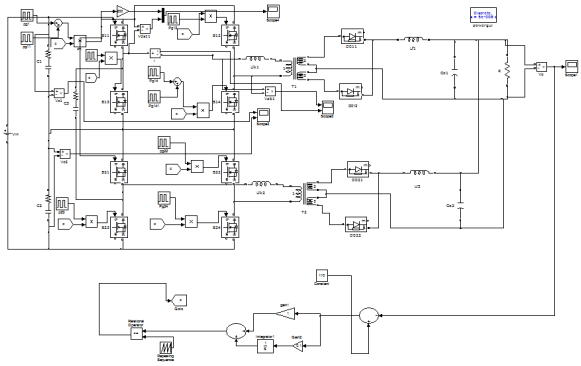
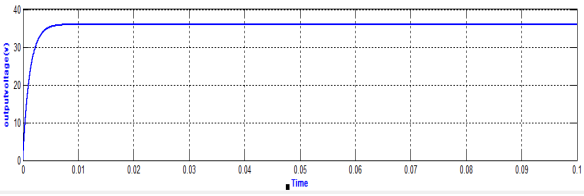


Fig.14.Matlab/Simulink circuit of closed loop system



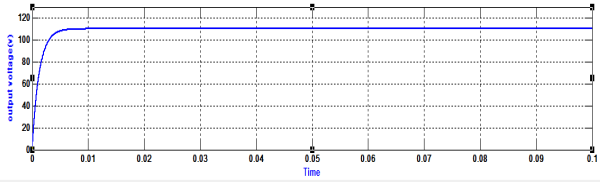


Fig.15. simulation waveforms of closed loop system with desired outputs of 36v and 110v

VI. CONCLUSION

A new converter by integrating full bridge converters and flying capacitor based three level converter is proposed to reduce conduction losses and to attain autobalance of capacitor voltages.ZVS performance of switches is achieved with the help of phase shift control scheme,thereby reduction in switching losses.A closed loop control is implemented to this new converter to achieve desired output voltages for various auxiliary equipments. The modular multilevel dc/dc converter concept can be easily extended to N-stage converter with stacked full-bridge modules to satisfy extremely high-voltage applications with low-voltage-rated power switches.

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