International Journal of Research
Available at https://edupediapublications.org/journals
p-ISSN: 2348-6848
e-ISSN: 2348-795X
Volume 03 Issue 11
July2016

Asymmetrical Multilevel Inverter for Higher Output Voltage Levels

B.SUJATHA
M-tech Student Scholar
Department of Electrical & Electronics Engineering,
Malla reddy Engineering College, (autonomous);
Ranga reddy secunderbad (Dt); Telangana, India.
Email:m.sujatha.mt@gmail.com

CH.NARENDER KUMAR
Associate Professor
Department of Electrical & Electronics Engineering,
Malla reddy Engineering College, (autonomous);
Ranga reddy secunderbad (Dt); Telangana, India.
Email.chnk.eee@gmail.com

Abstract: Now a days the growth of interest in multilevel inverters has been increasing because there are enormous applications of there in FACTS and industrial drives etc., Although there are many topologies of multilevel inverters in literature, popular among them are cascaded H-bridge. In general the control methods of these cascaded inverters are designed an assumption of having all dc source voltages same for all H-bridges. This paper discusses the abilities of cascaded multilevel inverter to produce more output voltage levels with same number of H-bridges, but with different input voltage ratios. The ideal nature of input dc voltage sources is shown as an advantage in this paper. The proposed inverter is then used to feed an induction motor drive and the simulation results are shown.

Keywords: Asymmetrical cascaded multilevel inverter, induction motor, pulse width modulation technique, v/f control method, synchronous speed.

I. INTRODUCTION

An induction motor is a paradigm of asynchronous AC machine, which consists of a stator and a rotor [I]. This motor is extensively used because of its well-built features and sensible cost. Induction motors are used in many industrial applications such as heating, ventilation, air conditioning systems, waste water treatment plants, blowers, fans, textile mills, and in rolling mills, etc. An electromagnetic field is generated when sinusoidal voltage is applied to the stator, in the induction motor. A current in the rotor is induced due to this field, which creates an added field that tries to align with the stator field, causing the rotor to revolve. When a load is applied to the motor a slip is formed between these fields. Compared to the synchronous speed, the rotor speed diminishes, at advanced slip values. The frequency of the stator voltage controls the synchronous speed [2]-[3]. The frequency of the voltage is applied to the stator through power electronic devices, which permits the control of the speed of the motor. Finally, the torque begins to fall when the motor reaches the synchronous speed. Thus, induction motor synchronous speed is defined by following equation,

$$Ns= 120f/p$$

Where f is the frequency of AC supply, n, is the speed of rotor; p is the number of poles per phase of the motor. By altering the frequency of control circuit throughout AC supply, the rotor speed will alter. The induction motor speed variation can be effortlessly achieved for a short variety by either stator voltage control or rotor resistance control. But together of these schemes result in very low efficiencies at lesser speeds. On the whole competent design for speed control of induction motor is by altering supply frequency. This not only results in design with wide speed range but also advances the starting performance. If the machine is functioning at speed under base speed, then v If ratio is to be set aside, so that flux remains stable. This

International Journal of Research
Available at https://edupediapublications.org/journals
p-ISSN: 2348-6848
e-ISSN: 2348-795X
Volume 03 Issue 11
July2016

retains the torque capability of the machine at the same value. But at lesser frequencies, the torque capability reduces and this drop in torque has to be compensated for increasing the applied voltage.

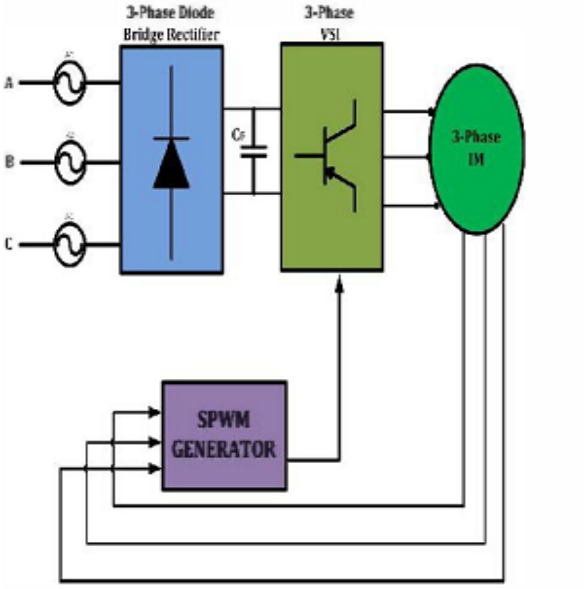


Fig. I. Block Diagram Schematic of Y/f control of YSI fed 3- phase Induction Motor Drive

List of benefits of Vlf Control are as follows:

- It provides good range of speed.
- It provides superior operation and momentary concert.
- It has low starting current requirement.
- It has a wider stable operating region.
- Voltage and frequencies reach rated values at base speed.
- The speeding up can be inhibited by controlling the rate of change of supply frequency.
- It is cheap and easy to implement.

Synchronous speed can be controlled by varying the supply frequency. Voltage induced in the stator is E I oc cD/where cD is the air-gap flux and f is the supply frequency. As we can ignore the stator voltage drop we obtain terminal voltage VI oc cD/. Thus reducing the frequency without varying the supply voltage will direct to a raise in the air-gap flux which is undesirable. Hence whenever frequency is diverse in order to control speed, the terminal voltage is also varied so as to maintain the Vlf ratio stable. Thus by maintaining a steady Vlf ratio, the maximum torque of the motor becomes constant for changing speed. Since voltage and frequency are the significant parameters to be considered for control the speed of induction motor, hence inverters are selected as the front end converters for induction motor, which can controlled together voltage and frequency.

A. Multilevel Inverters: Multilevel inverters have received added awareness for their ability on high-power and medium voltage function and because of former compensation such as high power quality, lower order harmonics, switching losses and improved electromagnetic interference [4], [5]. And also multilevel inverters are promising; they have virtually sinusoidal output-voltage wave forms, Output current with improved harmonic profile, a lesser amount of stressing of electronic components owing to decreased voltages, switching losses that are inferior than those of predictable two-level inverters, a slighter filter size, and worse EMI, all of which make them cheaper, lighter, and more compact. Multilevel inverters make small Common mode voltage; consequently the stress in the bearings of a motor allied to a multilevel motor drive can be condensed. In addition CM voltages can be eliminated by using advanced modulation technique.

Multilevel inverters can draw input current with low distortion. These inverters can operate at equally fundamental frequency and high switching frequency PWM. It should be noted that lower switching frequency means lower switching loss and higher efficiency. These inverters make a stepped voltage waveform by means of a number of dc voltage sources as the input and a suitable arrangement of the power-semiconductor-based devices [6]. Three major structures of the multilevel inverters have been presented: "diode clamped multilevel inverter," "flying capacitor

International Journal of Research
Available at https://edupediapublications.org/journals
p-ISSN: 2348-6848
e-ISSN: 2348-795X
Volume 03 Issue 11
July2016

multilevel inverter," and "cascaded multilevel inverter" [7].

The cascaded multilevel inverter is collected of a number of single-phase H-bridge inverters and is classified into symmetric and asymmetric groups based on the magnitude of dc voltage sources. In the symmetric types, all the dc voltage sources of cascaded H-bridges are having equal magnitudes, whereas in the asymmetric types, the values of the dc voltage sources of all H-bridges are dissimilar. In topical years, a number of topologies with various control techniques have been presented for cascaded multilevel inverters [8]-[9]. In [7] and, diverse symmetric cascaded multilevel inverters have been presented.

The foremost advantage of all these structures is the short variety of dc voltage sources, which is one of the most significant features in determining the cost of the inverter. On the other hand, because some of them utilize an elevated number of bidirectional power switches, a high number of insulated gate bipolar transistors (IGBTs) are necessary, which is the major drawback of these topologies. Consequently, it increases control complexity, circuit size and cost. The major advantage of this asymmetric topology and its algorithms is associated to its ability to create a substantial number of output voltage levels by using a low number of dc voltage sources and power switches but the high diversity in the magnitude of dc voltage sources is their most outstanding disadvantage. Recently, asymmetrical and hybrid multistage topologies are becoming one of the most fascinated research area. In the asymmetrical configurations, the magnitudes of dc voltage supplies are uneven. These topologies diminish the cost and size of the inverter and get better reliability since lesser number of power electronic components capacitors, and dc supplies are used.

The hybrid multistage converters consist of dissimilar multilevel configurations with uneven dc voltage supplies. Bidirectional switches with an suitable control technique can enhance the performance of multilevel inverters in terms of falling the number of semiconductor components, minimizing the withstanding voltage and achieving the required output voltage with higher levels [10]-[11]. The magnitudes of the utilized dc voltage supplies have been selected in a way that brings the elevated number of voltage levels with an effective application of a fundamental frequency staircase modulation technique. For a single-phase seven-level inverter, 12 power electronic switches are required in both the diode-clamped and the flying-capacitor topologies. Asymmetric voltage technology is used in the cascade H-bridge multilevel inverter to allow more levels of output voltage [12], so the cascade H-bridge multilevel inverter is suitable for applications with increased voltage levels. Two H-bridge inverters with a dc bus voltage of multiple relationships can be connected in cascade to produce a single phase seven-level inverter and eight power electronic switches are used. In this paper a new asymmetric Bi-directional converter topology which uses contradictory ratios of dc voltage sources.

II. PROPOSED CONCEPT

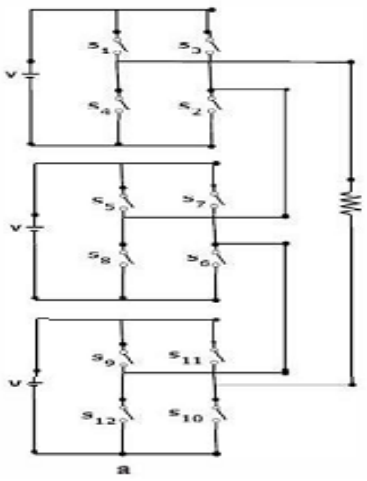
Hybrid Multilevel Inverter was introduced by means of all 3M possible output voltages, where M is the number of modules allied in series. Though this inverter uses extremely different DC voltage sources in the relation of 1:3:9 etc. In distinguish, the DC voltage sources consider in this paper are still exceptionally close to each other, they fluctuate only by ±20 %. The quantity of cells in sequence determines the number of output levels. 3M= 27 switching states SI ,when M= 3 cells. With similar DC voltages, there are numerous switching states that create the same output voltages, resulting in 2.M + 1 = 7 different phase output voltage levels. Uneven DC source voltages direct to an improved number of different output voltage levels. The maximum number of levels is 3M = 27. With the DC source voltages distributed as Viii :Vi12 : Vil3= 1Voc : 3Voc : 9Voc, all the dissimilar output voltage levels are consistently spaced. The aim of such an inverter (Hybrid

International Journal of Research
Available at https://edupediapublications.org/journals
p-ISSN: 2348-6848
e-ISSN: 2348-795X
Volume 03 Issue 11
July2016

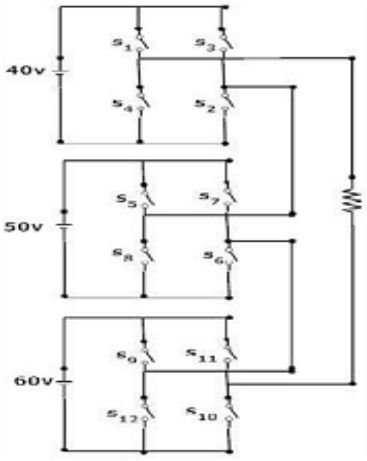
Multilevel Inverter) has the disadvantage that the preliminary modularity is vanished. Each module must be intended for the equivalent voltage class. When the DC source voltages are uneven but only ±20 % unlike from each other, the number of different output voltage levels is also superior. As an instance, we believe a case where one cell has 100 % of its nominal DC voltage, other has 120% and the third one has 80%.

The DC source voltages are in relation of 4:5:6 in this scheme. As can be seen, the voltage levels are approximately the same as in the 1:3:9 case, apart from some levels not there at high complete values of output voltage. In order to consider the possible benefits of using unlike DC voltages, the 4:5:6 relation is used as an instance in the following part. For a first estimation it is abandoned if these differences are introduced by the moment behavior of the DC voltages, or if they are introduced by design and thus can be supposed to be stable. The second case is considered at this time for the sake of simplicity.

The below figure shows the output wave forms the proposed asymmetrical converter. It is clearly seen that the level of inverter varies with the change in the ratios of input voltage. The inverter gives 7 level output voltage when the ratio is 1: 1:1, while it gives 23 level output voltage when the ratio is 4:5:6 and it gives 27 level output voltage when the ratio is 1:3:9. This inverter having 3 bridges connected in series gives different levels of output voltages without changing the circuit except the ratios of input voltages. Switching of the converter is done by following the staircase control technique. Pulse width Modulation technique can also be applied by appropriate calculation of the switching time period.

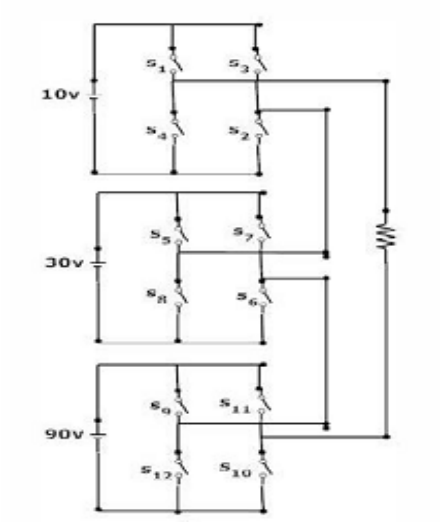


(a)



(b)

International Journal of Research
Available at https://edupediapublications.org/journals
p-ISSN: 2348-6848
e-ISSN: 2348-795X
Volume 03 Issue 11
July2016



(c)

Fig. 2. Proposed asymmetrical cascaded multilevel inverter with different voltage ratios

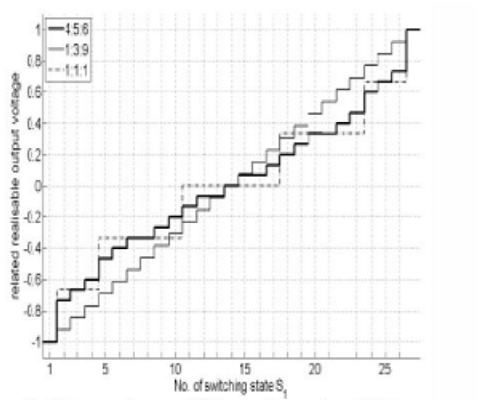


Fig.3.0utput voltages of different voltage ratios of CHB

III. CONTROL SCHEME

This section will discuss in detail a converter consisting of three modules with a DC voltage ratio of Vi11:Vi12:Vi13 = 4Voc : 5Voc : 6Voc. As can be seen in Fig. 3, this results in a huge number of diverse output voltage levels with an incredibly good voltage resolution. This composition will be compared with the predictable approach with identical DC voltage sources, and with the Hybrid Multilevel Inverter using a 1:3:9 voltage relation. Two different control methods for a single phase converter are offered. Both algorithms imagine a steady sampling interval of the control, Ts. The first one uses a stable switching state during a full sampling interval (step or staircase method), whereas the second one is implemented with a Pulse Width Modulation (PWM method). Both methods receive that the DC source voltages are not steady but variable in time. The definite voltages on the capacitors are therefore calculated, and the phase voltage vector Vii is created. In order to compute all attainable output voltages Vol, the phase voltage vector is multiplied with all 311 possible switching states SI. This results in an unsorted vector containing all feasible output voltages.

TABLE I. SWITCHING SEQUENCE OF 23-LEVEL CHB INVERTER

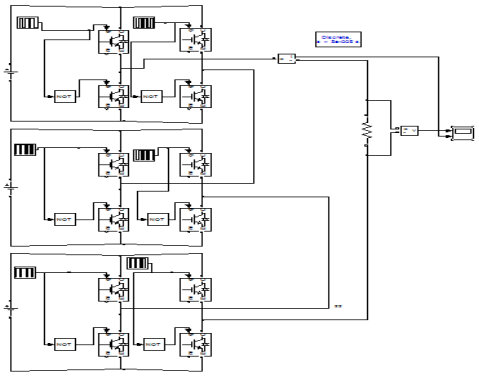
International Journal of Research
Available at https://edupediapublications.org/journals
p-ISSN: 2348-6848
e-ISSN: 2348-795X
Volume 03 Issue 11
July2016

Switches / Voltage Levels	S1	S2	S3	S4	S5	S6	S7	S8	S9	S10	S11	S12
V_{dc}	1	0	1	0	0	0	1	1	1	1	0	0
$2V_{dc}$	0	0	1	1	1	0	1	0	1	1	0	0
$3V_{dc}$	1	1	0	0	1	1	0	0	0	0	1	1
$4V_{dc}$	1	1	0	0	1	0	1	0	1	0	1	0
$5V_{dc}$	1	0	1	0	1	1	0	0	1	0	1	0
$6V_{dc}$	1	0	1	0	1	0	1	0	1	1	0	0
$7V_{dc}$	0	0	1	1	1	1	0	0	1	1	0	0
$9V_{dc}$	1	1	0	0	1	1	0	0	1	0	1	0
$10V_{dc}$	1	1	0	0	1	0	1	0	1	1	0	0
$11V_{dc}$	1	0	1	0	1	1	0	0	1	1	0	0
$15V_{dc}$	1	1	0	0	1	1	0	0	1	1	0	0
$0V_{dc}$	1	0	1	0	1	0	1	0	1	0	1	0
$-V_{dc}$	1	0	1	0	1	1	0	0	0	0	1	1
$-2V_{dc}$	1	1	0	0	1	0	1	0	0	0	1	1
$-3V_{dc}$	0	0	1	1	0	0	1	1	1	1	0	0
$-4V_{dc}$	0	0	1	1	1	0	1	0	1	0	1	0
$-5V_{dc}$	1	0	1	0	0	0	1	1	1	0	1	0
$-6V_{dc}$	1	0	1	0	1	0	1	0	0	0	1	1
$-7V_{dc}$	1	1	0	0	0	0	1	1	0	0	1	1
$-9V_{dc}$	0	0	1	1	0	0	1	1	1	0	1	0
$-10V_{dc}$	0	0	1	1	1	0	1	0	0	0	1	1
$-11V_{dc}$	1	0	1	0	0	0	1	1	0	0	1	1
$-13V_{dc}$	0	0	1	1	0	0	1	1	0	0	1	1

TABLE II. SWITCHING SEQUNCE OF 27-LEVEL CHB INVERTER

Switches / Voltage Levels	S1	S2	S3	S4	S5	S6	S7	S8	S9	S10	S11	S12
V_{dc}	1	1	0	0	0	1	0	1	0	1	0	1
$2V_{dc}$	0	0	1	1	1	1	0	0	0	1	0	1
$3V_{dc}$	0	1	0	1	1	1	0	0	0	1	0	1
$4V_{dc}$	1	1	0	0	1	1	0	0	0	1	0	1
$5V_{dc}$	0	0	1	1	0	0	1	1	1	1	0	0
$6V_{dc}$	0	1	0	1	0	0	1	1	1	1	0	0
$7V_{dc}$	1	1	0	0	0	0	1	1	1	1	0	0
$8V_{dc}$	0	0	1	1	0	1	0	1	1	1	0	0
$9V_{dc}$	0	1	0	1	0	1	0	1	1	1	0	0
$10V_{dc}$	1	1	0	0	0	1	0	1	1	1	0	0
$11V_{dc}$	0	0	1	1	1	1	0	0	1	1	0	0
$12V_{dc}$	0	1	0	1	1	1	0	0	1	1	0	0
$13V_{dc}$	1	1	0	0	1	1	0	0	1	1	0	0
$0V_{dc}$	0	1	0	1	0	1	0	1	0	1	0	1
$-V_{dc}$	0	0	1	1	0	1	0	1	0	1	0	1
$-2V_{dc}$	1	1	0	0	0	0	1	1	0	1	0	1
$-3V_{dc}$	0	1	0	1	0	0	1	1	0	1	0	1
$-4V_{dc}$	0	0	1	1	0	0	1	1	0	1	0	1
$-5V_{dc}$	1	1	0	0	1	1	0	0	0	0	1	1
$-6V_{dc}$	0	1	0	1	1	1	0	0	0	0	1	1
$-7V_{dc}$	0	0	1	1	1	1	0	0	0	0	1	1
$-8V_{dc}$	1	1	0	0	0	1	0	1	0	0	1	1
$-9V_{dc}$	0	1	0	1	0	1	0	1	0	0	1	1
$-10V_{dc}$	0	0	1	1	0	1	0	1	0	0	1	1
$-11V_{dc}$	1	1	0	0	0	0	1	1	0	0	1	1
$-12V_{dc}$	0	1	0	1	0	0	1	1	0	0	1	1
$-13V_{dc}$	0	0	1	1	0	0	1	1	0	0	1	1

IV.MATLAB/SIMULATION RESULTS



International Journal of Research
Available at https://edupediapublications.org/journals
p-ISSN: 2348-6848
e-ISSN: 2348-795X
Volume 03 Issue 11
July2016

Fig 4 Matlab/simulation circuit of symmetrical cascaded multilevel inverter

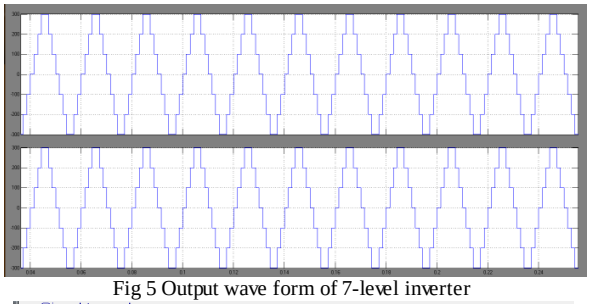


Fig 5 Output wave form of 7-level inverter

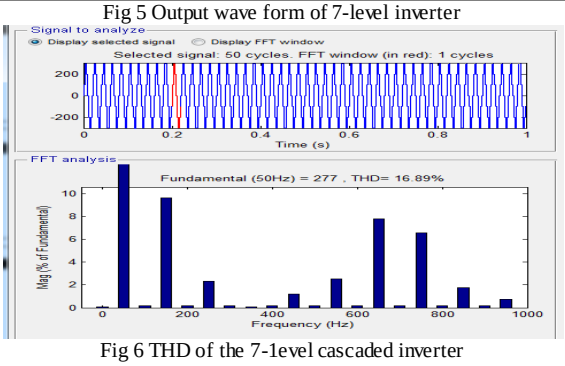


Fig 6 THD of the 7-1evel cascaded inverter

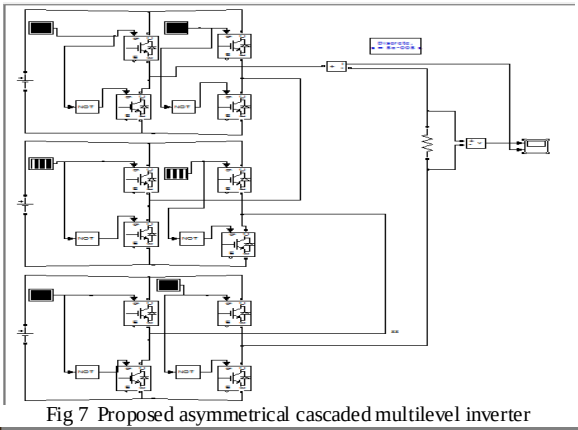


Fig 7 Proposed asymmetrical cascaded multilevel inverter

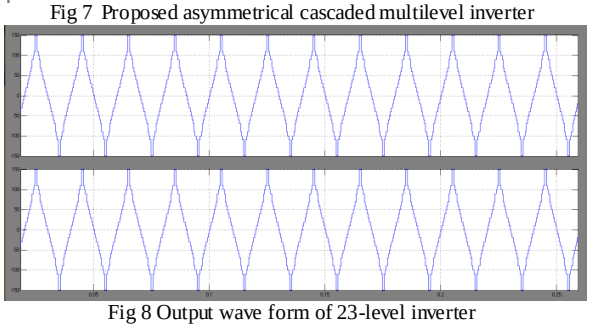


Fig 8 Output wave form of 23-level inverter

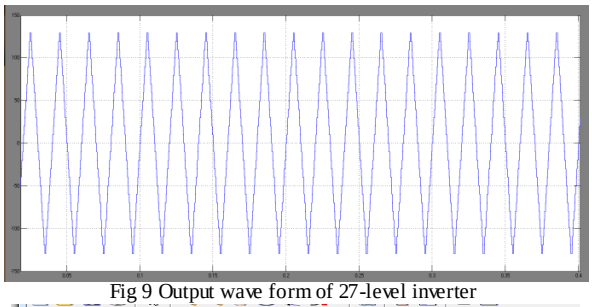


Fig 9 Output wave form of 27-level inverter

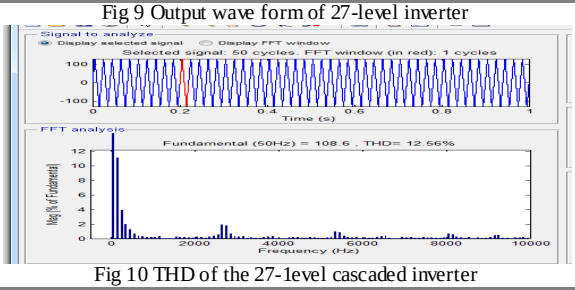


Fig 10 THD of the 27-1evel cascaded inverter

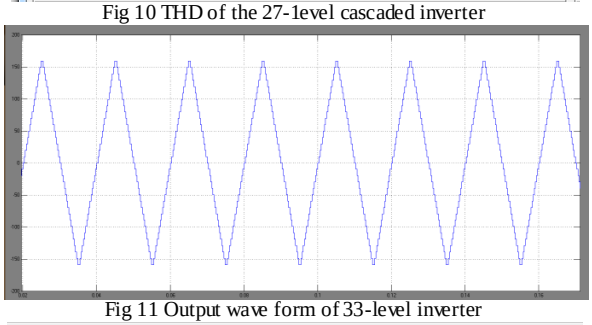


Fig 11 Output wave form of 33-level inverter

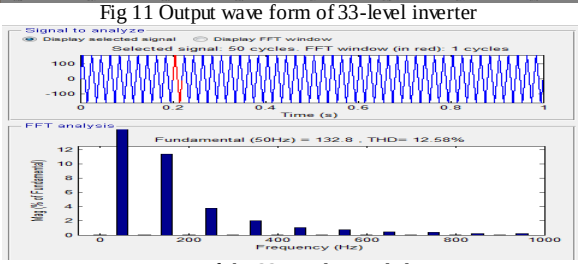


Fig 12 THD of the 33-1evel cascaded inverter

V.CONCLUSION

The simulation results show that in this paper 3-phase 23-level and 27-level asymmetrical cascaded H-bridge inverter are studied. The output voltage of three phase Asymmetrical 23-level CHB gives 16.59% THD, whereas 27-level asymmetrical CHB gives 12.56% THD without PWM technique. Hence compared to 23-level CHB,27-level and 33-level CHB unequal de voltage ratios consists of minute number of harmonics and increased output voltage quality. Finally the proposed system is

connected to induction motor for future industrial and automotive applications and the simulation results are shown.

REFERENCES

[I] 1. A Santiago-Gonzalez, 1.Cruz-Colon, R. otero-De-leon, V. lopezSantiago, E.I. Ortiz-Rivera, " Thre phase induction motor drive using flyback converter and PWM inverter fed from a single photovoltaic panel," Proc. IEEE PES General Meeting, pp. 1-6,20II.

[2] M. A Vitorino et aI. , "An efficient induction motor control for photovoltaic pumping," IEEE Trans. Industrial Electron., vol. 54, no.4, pp. 1162-1170, April. 2011.

[3] ADiaz, R. Saltares, C. Rodriguez, R. F. Nunez, E.!. OrtizRivera, and 1. Gonzalez-Llorente, "Induction motor equivalent circuit for dynamic simulation," Proc. IEEE Electric Machines and Drive Conference, (lEMDC), May 2009.

[4] E. Babaei and S. H. Hosseini, "Charge balance control methods for asymmetrical cascade multilevel converters," in Proc. ICEMS, Seoul, Korea, 2007, pp. 74-79.

[5] K. Wang, Y. Li, Z. Zheng, and L. Xu, "Voltage balancing and fluctuation suppression methods of floating capacitors in a new modular multilevel converter," IEEE Trans. Ind. Electron., vol. 60, no. 5, pp. 1943-1954, May 2013.

[6]L.M Tolbert, F. Z.Peng and T.G Habelter, "Multilevel Converter for large electric drives," IEEE trans.lnd.Appl.VoI35, no.I, pp. 36-44, Jan/Feb.1999.

[7].K. Nakata, K. Nakamura, S. lto and K. Jinbo, "A three level traction inverter with IGBTs for EMU", in Conf.Rec.lEEE lAS Annu.meeting, 1994, voU, pp. 667- 672.