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Design and Implementation of Five Level Inverter based MPPT Using Self Lift SEPIC Converter

N. KIRAN KUMAR
M-tech Student Scholar
Department of Electrical & Electronics Engineering,
Avanthi's St. Theressa Engineering and Technology,
Garividi;
Vizianagaram(Dt); Andhra pradesh, India.

B. SANKARA PRASAD.,M.Tech.
Associate Professor
Department of Electrical & Electronics Engineering,
Avanthi's St. Theressa Engineering and Technology,
Garividi;
Vizianagaram(Dt); Andhra pradesh, India.

Abstract: The conventional power conditioning units require a DC-DC converter followed by an inverter circuit to deliver the required power to the load. This increases the required power conversion stages, system cost, size and reduces the overall system efficiency. Therefore, to maximize the efficiency of the renewable energy system, it is necessary to track the maximum power point of the input source. This paper presents the modeling and simulation of incremental conductance (IncCond) Maximum Power Point Tracking (MPPT) using Multi level Single Ended Primary Inductance Converter (SEPIC) converter and compared its performance with self lift SEPIC converter. The solar panel model is developed using the basic circuit equations of photovoltaic cell. The MPP of a solar panel varies with irradiation and temperature. The IncCond algorithm is used to track the maximum power from the solar panel. The unregulated voltage from the panel will be regulated by using the Multi level SEPIC at the same time it can also supply the medium voltage and high voltage loads. The efficiency of the Multi level SEPIC converter over the self lift SEPIC converter has been tested by using Matlab/Simulink.

Index Terms— Microcontroller, Incremental conductance (IncCond) Maximum Power Point Tracking (MPPT), self lift SEPIC, photovoltaic (PV) system.

I. INTRODUCTION

According to the realization of high efficiency and low costphotovoltaic (PV) modules, interest in photovoltaic powergeneration system has increased over the past decade as aclean and infinite energy [1-2]. The PV modules have maximumoperating points corresponding to the surrounding conditionsuch as intensity of the sunlight, the temperature of the PVmodules, cell area, and load. When solar energy is used as apower source, the output power has to be maximized byimproving the efficiency of the power conditioningequipment used and implementing an adaptive powercontroller that automatically tracksthe system to the point of maximum power delivered fromthe solar panel under all conditions. It is well known that aPV module consists of several PV cells connected in seriesin order to ensure a useful output voltage level. Assumingthat the cells are identical, this level is calculated bysumming each cell voltage. The functioning parameters [3-7]of the module depend mainly on the solar irradiance and onthe cells temperature, as well as on the Semiconductor material properties. For each meteorological condition thereis a maximum power point (MPP) at which the system mustwork in order to deliver the optimal power to its load. The objective of the maximum power point trackers (MPPT) isto make the system [8] work in this point or near.To track the maximum power a dc/dc converter isrequired with load voltage control. Dual converters areuseful when dual output voltage levels are required fromsingle input supply voltage with MPPT. Fly back converter iscapable to produced dual output voltage levels but it required transformer. The gain of fly back converter isdepends upon the turns ratio of transformer. Sepic converteris used for step up and step down application [9]. High gainmultilevel boost converter is used to step up the voltagelevel with large conversion ratio [10]. More number of switches and elements are required for generating dual output voltage level from conventional converters. Due toincreases in number of switches and elements, convertercircuit becomes more expensive and complex [11].

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II. PHOTOVOLTAIC MODELING

The simplest model of a PV cell consists of an ideal current source in parallel with an ideal diode is shown in Figure.1. The current source of PV cell represents the current generated by photons and its output is constant under constant temperature and constant incident radiation of light.A solar cell is the building block of a PV panel. A solar cell module is formed by connecting many solar cells in series and parallel. Considering only a single solar cell, it can bemodeled by using a current source, a diode and two resistors. This model is known as a single diode model of a PV cell.

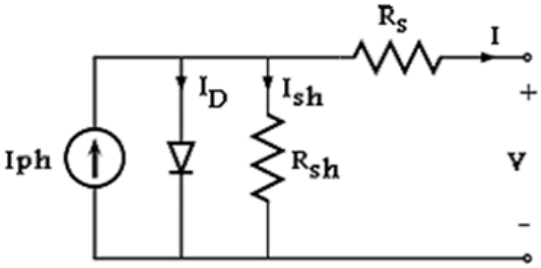

Fig.1. Equivalent circuit of PV cell.

The output current from the PV cell is found by applying the Kirchoff's current law on the equivalent circuit.

$$I=I_{ph}-I_D \quad (1)$$

Where I is the output current from PV cell, $I_{ph}$is the photon current, Id is the diode current. The ideal diode equation is given as follows:

$$I_D=I_s(e^{qVd/kT}-1) \quad (2)$$

Where I_D is the diode current, I_S is the saturation current, q is the electron charge, k is the Boltzmann constant and T is the actual temperature. By substituting Eq. 2 in Eq. 1, wecan get the value of the photon current I_{ph} The photocurrent mainly depends on the solar insulation and cell's working temperature, which is described as

$$I_{ph}=[I_{sc}+K_i(T-298)]\frac{\lambda}{1000} \quad (3)$$

where I_{ph} is the photon current , I_{sc} is the cell's short circuit current, K_i is the cell's short-circuit current temperature coefficient, T is the solar cell's actual temperature, and λ is the solar insulation. The reverse saturation current is expressed as

$$I_{rs}=I_{sc}/[\exp(qV_{oc}/N_skAT)-1] \quad (4)$$

where I_{rs} is the reverse saturation current, V_{oc} is the open circuit voltage, N_s is the number of cells connected series, A is the ideality factor, k is the Boltzmann constant, q is the electron charge and T is the actual temperature.

The module saturation current I_s varies with the cell temperature, which is given by

$$I_s=I_{rs}[(T/T_r)^3\exp\{qE_g/Ak\{(1/T_r)-(1/T)\}] \quad (5)$$

Where I_s is the saturation current, E_g is the band-gap energy of the semiconductor used in the cell, $T_r$is the reference temperature. The current output of PV module is

$$I_{pv}=N_pI_{ph}-N_pI_s[\exp\{q(V_{pv}+I_{pv}R_s)/N_sAkT\}-1] \quad (6)$$

Where I_{pv} is the photovoltaic current and N_p is the number of cells connected in parallel. In fact, the PV efficiency is sensitive to small change in R_s but insensitive to variation in R_{sh}. For a PV module, the series resistance becomes apparently important and the shunt resistanceapproaches infinity which is assumed to be open, where $V_{pv}=V_{oc}$, $N_p=1$ and Ns=36. The P-V and I-V curves of a solar cell are highly dependent on the solar irradiation values and temperature which is shown in Figure.2 and Figure 3.3. With increase in the solar irradiation the opencircuit voltage increases. Increase in temperature is accompanied by a decrease in the open circuit voltage value.

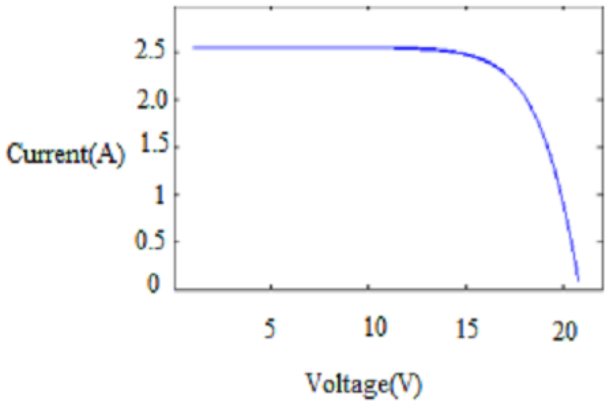

Fig.2 I-V curve of a solar cell.

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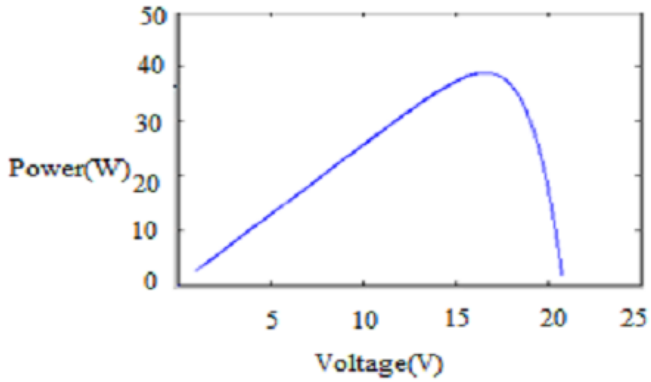

Fig.3. P-V curve of a solar cell.

Increase in temperature causes increase in the band gap of the material and thus more energy is required to cross this barrier. Thus the efficiency of the photovoltaic cell is reduced.

III. MAXIMUM POWER POINT TRACKING

A typical solar panel converts only 30 to 40 percent of the incident solar irradiation into electrical energy. Maximum power point tracking technique is used to improve the efficiency of the solar panel. According to Maximum Power Transfer theorem, the power output ofa circuit is maximum when the Thevenin impedance of the circuit (source impedance) matches with the load impedance. Hence our problem of tracking the maximum power point reduces to an impedance matching problem. In the source side we are using a self lift SEPICconverter connected to a solar panel in order to enhance the output voltage so that it can be used for different applications like motor load. By changing the duty cycle ofthe self lift SEPIC converter appropriately we can match the source impedance with that of the load impedance.

A. Incremental Conductance Algorithm

Incremental conductance method uses voltage and current sensors to sense the output voltage and current of the PV array. At MPP the slope of the PV curve is 0.

$$\frac{dI}{dV} = -\frac{I}{V} \quad \left(\frac{dP}{dV} = 0\right) \tag{7}$$

The left hand side of the equation represents incremental conductance of the PV module, and the right hand side of the equation represents the instantaneous conductance of the PV panel. From the Equation 7, it is obvious that when the ratio of the change in the output conductance is equal to the negative output conductance, then maximum power point is reached.

$$\frac{dI}{dV} > -\frac{I}{V} \quad \left(\frac{dP}{dV} > 0\right) \tag{8}$$

$$\frac{dI}{dV} < -\frac{I}{V} \quad \left(\frac{dP}{dV} < 0\right) \tag{9}$$

Equation 8 and Equation 9 are used to determine the direction in which a perturbation must occur to move the operating point toward the maximum power point, and the perturbation is repeated until Equation 7 is satisfied. Once the MPP is attained, the MPPT continues to operate at thispoint until a change in current is measured.

The present value and the previous value of the PV voltage and current are used to calculate the values of dI and dV. If dV>0 and dI>0, then the amount of sunlight has increased, by increasing the MPP voltage.

Figure.4 shows the flowchart for the incremental conductance algorithm. Here we will measure both the voltage and current simultaneously. Hence the error due to change in insulation is eliminated. IncCon method is the simplest method when comparing to other MPPT methods.

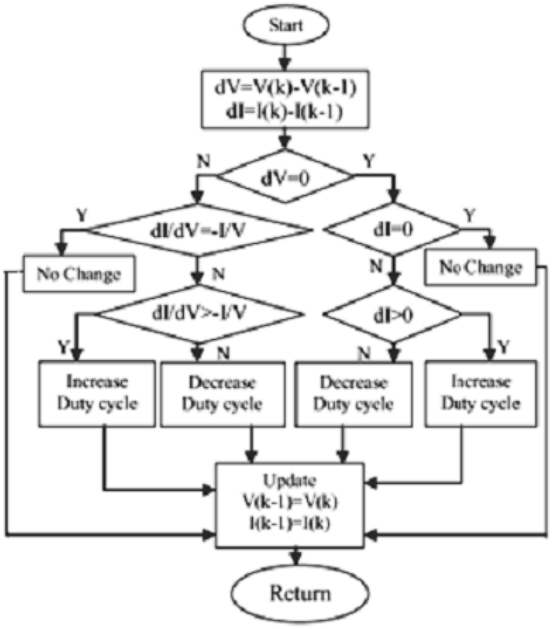

Fig.4. Flowchart of the IncCond method.

Incremental Conductance method is the best methods because it does not produce steady state o oscillations and it provides precise control under rapidly vary atmospheric condition. It can track the maximum power from the sun.

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IV.SELECTING PROPER CONVERTER

There are a number of different topologies for DC-DC converters. The buck topology is used to step down the voltage. The boost topology is used for stepping up the voltage. Then, there are topologies able to step up and down the voltage such as: buck-boost, cuk converter and SEPICconverter. Thus, the additional boost capability can slightly increase the overall efficiency. The SEPIC and the self lift SEPIC converter can be able to step up and step down the voltage. Figure.5 shows the circuit diagram of SEPIC converter. Figure.6 shows the electrical circuit of self lift SEPIC converter.

A. SEPIC Converter

The Single Ended Primary Inductance Converter (SEPIC) is a DC/DC-converter topology that provides a positive regulated output voltage from an input voltage that varies from above to below the output voltage. The capacitor C is used to transfer the energy and it is connected alternately to the input and to the output of the converter via the commutation of the transistor and the diode.

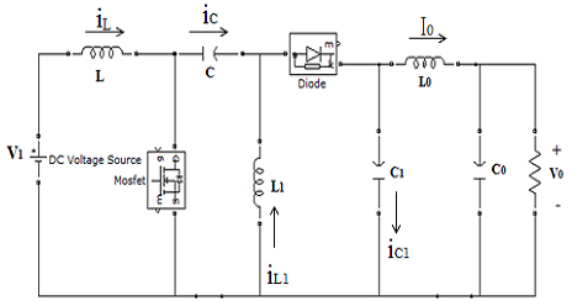

Fig.5. SEPIC converter

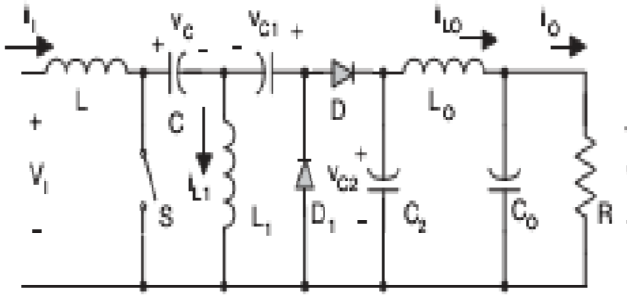

Fig.6. Electrical circuit of self lift SEPIC converter.

The maximum voltage obtained from the panel is unregulated. The unregulated voltage can be converted to regulated voltage by using a self lift SEPIC converter. Self lift SEPIC converter is one of the types of voltage lift converters. It is the improved version of SEPIC converter. Inthis converter the input current and the output current is continuous. The output voltage ripple produced in this converter is very less when compared to SEPIC converter.

As for component stress, it can be seen that the self lift SEPIC converter has smaller voltage and current stresses than the SEPIC converter. It has low switching losses and highest efficiency when compared to SEPIC converter. Figure.6 shows the self lift SEPIC converter equivalent circuit. Figure.7 and Figure.8 shows its operating modes, which acts like an interface between PV panel and the resistive load.

B. Operating Modes of Self Lift SEPIC Converter

This converter performs DC-DC voltage increasing conversion in simple structure. The self lift SEPIC converter has two modes of operation.

1) Mode 1: During the first mode of operation the switch will be turned on. The switch S, D_1 are on and diode D is off. During switch-on period, the voltage across the capacitors C and C_1 are equal.

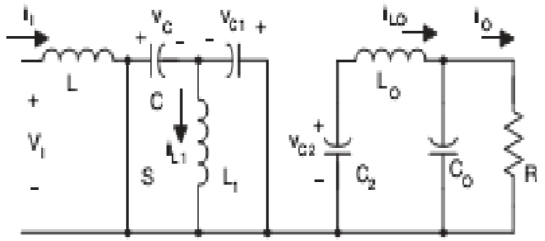

Fig.7. Electrical circuit of self lift SEPIC converter during switch ON period.

The equations for the switch conduction mode are as follows:

$$V_{c1} = V_c = V_1 \quad (10)$$

In steady state, the average voltage across inductor L_0 over a period is also zero.

Thus,

$$V_0 = V_{c2} = V_{c0} \quad (11)$$

The inductor current increases during switch on and it starts to decrease during switch off. The corresponding voltages across inductor L are input voltage V_1 and – (Vc Vc1+Vc2-V1).

Therefore,

$$kTV_1 = (1\text{-}k)T\,(V_c - V_{c1} + V_{c2} - V_1) \quad (12)$$

and hence

$$V_0 = V_{c2} = V_{c0} = \frac{V1}{(1-k)} \quad (13)$$

Since all the components are ideal, the power loss associated with all the circuit elements is neglected. Therefore the output power P_o is considered to be equal to the input power P_{IN}:

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$$V_o I_o = V_1 I_1 \quad (14)$$

$$I_L = I_1 = \frac{I_o}{(1-k)} \quad (15)$$

2) Mode 2: During the switch-off condition, diode D is on, switch S and diode D1 are off. The inductor current decreases and diode D is forward biased and the capacitor C is charged by using the input supply.

The capacitor C_0 acts as a low pass filter so that

$$I_{LO} = I_o \quad (16)$$

The current i_L increases during switch-on. The voltage across it during switch-on isV_1, therefore its peak to peak current variation is

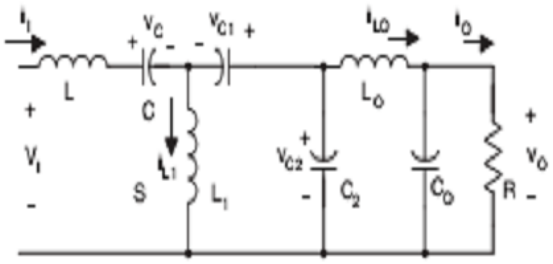

Fig.8. Electrical circuit of self lift SEPIC converter during switch OFF period.

$$\Delta i_L = \frac{kTV_1}{L} \quad (17)$$

During the steady state condition the average inductor voltage and the capacitive current waveforms are zero. The relationship between the output and input currents are givenin the following:

$$\frac{I_1}{I_o} = \frac{1}{(1-k)} \quad (18)$$

The peak to peak variation of the voltage V_c is

$$\Delta v_c = \frac{I_o}{fC} \quad (19)$$

Assuming 5% of ripple in the capacitor voltage, we can find the value of capacitor C. The peak to peak variation of the voltage v_{c1} is

$$\Delta v_{c1} = \frac{I_o}{fC_1} \quad (20)$$

Assuming 5% of ripple in capacitor voltage ΔV_{c1}, we can find the value of C1. The peak to peak variation of the voltage v_{c2} is

$$\Delta i_{LO} = \frac{kV_o}{8f^2 L_O C_2} \quad (21)$$

Assuming 5% of ripple in the inductor current, we can find the value of L_0. The peak to peak variation of voltage v_0 and v_{c0} is

$$\Delta v_O = \Delta v_{CO} = \frac{I_o k}{64 f^3 L_O C_2 C_O} \quad (22)$$

Assuming 5% of ripple in capacitor voltage Δv_{c0} we can find the value of filter capacitor c_0.

V.DIODE-CLAMP MULTILEVEL INVERTER

The most commonly used multilevel topology isthe diode clamped inverter, in which the diode is used as theclamping device to clamp the dc bus voltage so as toachieve steps in the output voltage. Thus, the main conceptof this inverter is to use diodes to limit the power devicesvoltage stress. The voltage over each capacitor and eachswitch is Vdc. An n level inverter needs (n-1) voltagesources, 2(n-1) switching devices and (n-1) (n-2) diodes. Byincreasing the number of voltage levels the quality of theoutput voltage is improved and the voltage waveformbecomes closer to sinusoidal waveform

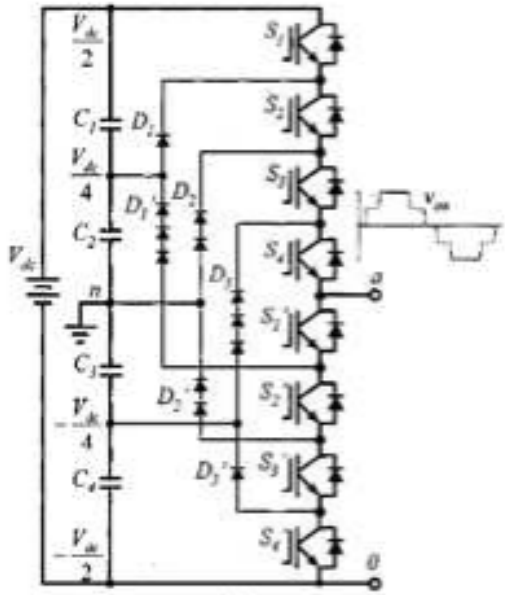

Figure.9.Diode-Clamped Multilevel Inverter Circuit Topologies.

Figure.9.shows a five-level diode-clamped converter inwhich the dc bus consists of four capacitors, C1, C2,

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C3,and C4. For dc-bus voltage Vdc, the voltage across eachcapacitor is Vdc/4 and each device voltage stress will belimited to one capacitor voltage level Vdc/4 throughclamping diodes. The order of numbering of the switches for phase a is S1, S2, S3, S4, S1', S2', S3' and S4'.For example to have Vdc/2 in the output, switchesS1 to S4 should conduct at the same time. For each voltagelevel four switches should conduct. As it can be seen inTable.1 the maximum output voltage in the output is half ofthe DC source. It is a drawback of the diode clampedmultilevel inverter. This problem can be solved by using atwo times voltage source or cascading two diode clampedmultilevel inverters. The output voltage of a 5-level diodeclamped multilevel inverter all of the voltage level shouldhave the same voltage value.The switching angles should be calculated in such away that the THD of the output voltage becomes as low aspossible. The switching angle calculation method that isused in this thesis is the harmonic elimination method. Inthis method the lower dominant harmonics can beeliminated by choosing calculated switching angles.Table-1 shows the output voltage levels and thecorresponding switch states for one phase of the chosen fivelevel DCMLI. The switches are arranged into 4 pairs (S1,S1'), (S2, S2'), (S3, S3'), (S4, S4'). If switching sequence asgiven in table 1. State condition 1 means switch ON and 0means switch OFF.

Table1: The switching state of diode clamp multilevel inverter.

V_0	S_1	S_2	S_3	S_4	S_1'	S_2'	S_3'	S_4'
$V_{dc}/2$	1	1	1	1	0	0	0	0
$V_{dc}/4$	0	1	1	1	1	0	0	0
0	0	0	1	1	1	1	0	0
$-V_{dc}/4$	0	0	0	1	1	1	1	0
$-V_{dc}/2$	0	0	0	0	1	1	1	1

The steps to synthesis the five level phase a output voltagein this work are as follows:

1. For phase a output voltage of Van=0, two upper switchesS3, S4 and two lower switches S1' and S2'are turned on.
2. For an output voltage of Van=Vdc/4, three upper switchesS2, S3, S4 and one lower switch S1' are turned on.
3. For an output voltage of Van=Vdc/2, all upper switches S1through S4 are turned on.
4. To obtain the output voltage of Van= -Vdc/4, upper switchS4 and three lower switches S1', S2'and S3'are turned on.
5. For an output voltage of Van = -Vdc/2, all lower switchesS1'through S4' are turned on.

The phase a output voltage Van has five states: Vdc/2, Vdc/4,0, - Vdc/4 and - Vdc/2. The gate signals for the chosen five level DCMLI are developed using MATLAB-SIMULINK.The gate signal generator model developed is tested forvarious values of modulation index. Diode clampedmultilevel inverter is a very general and widely usedtopology. DCMLI works on the concept of using diodes tolimit voltage stress on power devices.

VI. MATLAB/SIMULATION RESULTS

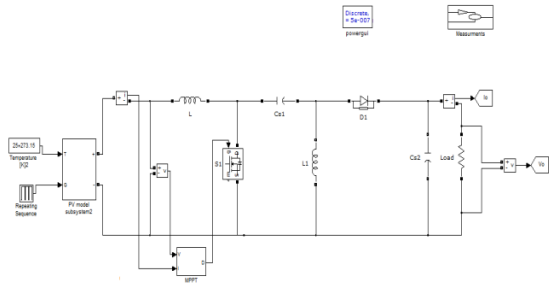

Fig.10.Simulink model of the PV panel connected to the SEPIC converter with MPPT.

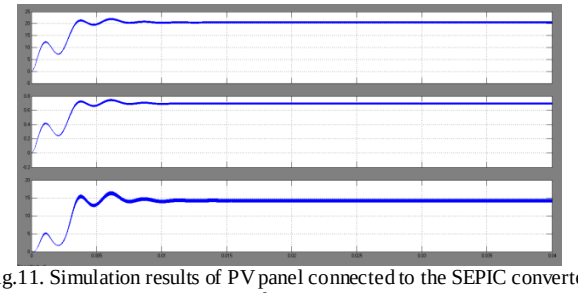

Fig.11. Simulation results of PV panel connected to the SEPIC converter with MPPT.

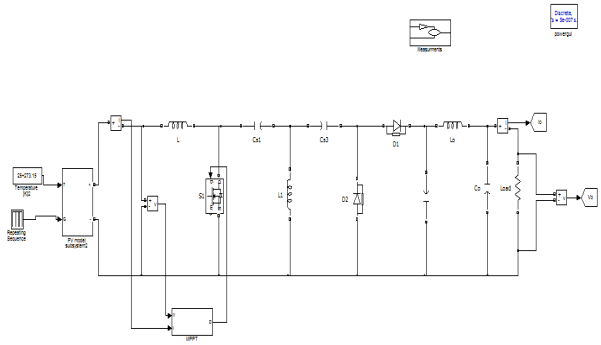

Fig.12.Simulink model of the PV panel connected to the self lift SEPIC converter with MPPT.

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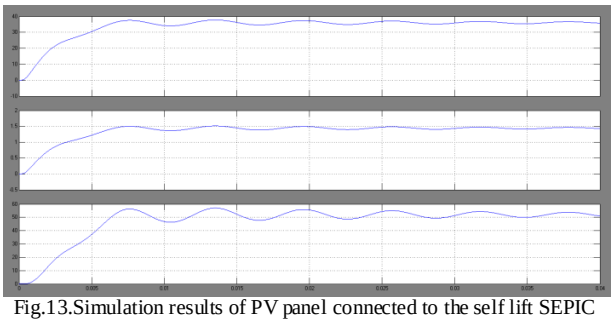

Fig.13.Simulation results of PV panel connected to the self lift SEPIC converter with MPPT.

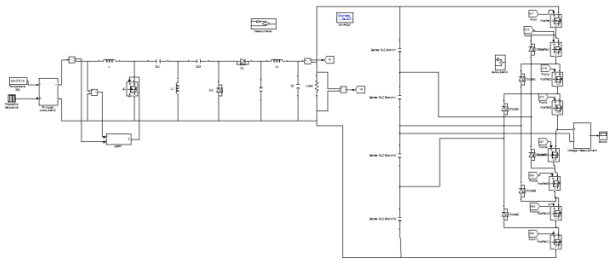

Fig.14.Simulink model of the PV panel connected to the self lift SEPIC converter with MPPT and single phase five level inverter.

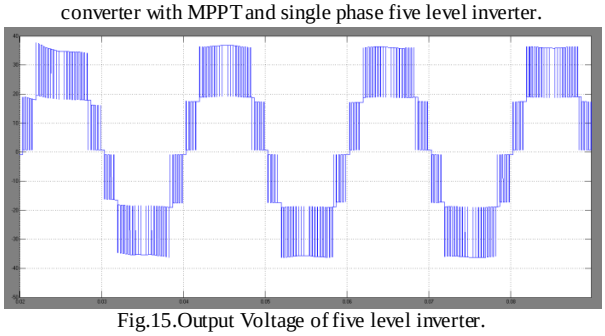

Fig.15.Output Voltage of five level inverter.

VII. CONCLUSION

This paper proposes a simple MPPT method that requiresonly measurements of voltage and current. The proposedIncremental conductance MPPT algorithm increases theefficiency and it tracks the maximum power from the sun. This method computes the maximum power and controlsdirectly the extracted power from the PV by changing theduty cycle in the self lift SEPIC converter. This method computes the maximum power and controls directly the extracted power from the PV by changing the duty cycle in the Multi level SEPIC converter.The voltage produced by High Gain Multi level SEPIC converter is higher when compared to Self lift SEPIC converter. The proposed method offers different advantages which are: good tracking efficiency, response is high and well control for the extracted power and also for load voltage control.

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