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Speed control of BLDC motor for five-level DC-DC converter with asymmetrical control strategy

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Abstract - In this project, an asymmetrical duty cycle control strategy was proposed to the TPTL dc/dc converter. The modified converter remains all the advantages of original control strategy; meanwhile, soft-switching can be achieved using the energy stored in output filter inductance and leakage inductances of transformers (or resonant inductances).Three-phase three-level (TPTL) dc/dc converter has the advantages of lower voltage and current stress on switches, which is suitable for high power and high input voltage applications. Adopting a symmetrical control strategy, the ripple frequency of input and output current can be increased significantly, resulting in a reduced filter requirement. However, all the switches are hard-switching, leading to a considerable switching loss. Full-bridge dc/dc converters have been used widely in the medium-to-high-power applications for the pulse width = modulation (PWM) control, soft-switching characteristics, and lower power rating on switches. To further reduce the current stress on switches for higher power level requirements, a prominent three-phase full-bridge topologies was first put forward by Ziogas for medium-voltage-level applications [1], in which three-phase bridges consisting of six switches and a three-phase transformer are adopted. With the three-phase architecture, the converters has the superior features, including lower current rating of switches, reduced input and output current ripple allowing small size filter requirement and better utilization of transformer core. The improved resonant converter features zero-voltage-switching (ZVS) realization under wide load range and higher conversion efficiency. However, wide variation in switching frequency should be concerned in the applications with wide input/output voltage range. Other alternative solutions are the non resonant soft-switching three-phase converters. in order to obtain ZVS commutation for all switches and control the output voltage, Nevertheless, the upper and lower commutation cell switches are subjected to different current stresses) is improved by using MAT Lab/Simulink. The proposed concept can be implemented with five levels the proposed concept can be implemented for speed control of BLDC motor using Matlab/Simulink software

***Index Terms*—Asymmetrical duty cycle control, dc/dc converter, three-level, three-phase, zero-voltage switching.**

I. INTRODUCTION

Over the years single phase full-bridge (FB) and three-phase FB pulse width modulation (PWM) dc to dc soft switched converters have become popular in the field of dc to dc conversion system. For these converters metal oxide semiconductor field effect transistors (MOSFETs) are generally preferred over insulated gate bipolar transistors (IGBTs), because they can be operated at higher switching frequency and they do not have the problem of long tail current. However, these FB PWM soft switched converters are not suitable for switch mode power supply applications, where the input voltage is high. This is because the MOSFETs have to sustain high input dc link voltage. Moreover, service of auxiliary circuits is required to operate devices in soft switched mode. This requires extra components, devices and hence it leads to incurring additional cost while reducing the system reliability. In order to reduce the voltage stress to half of the input dc voltage, a three-level topology has been considered in [1] and [2] for inverter application and it has been used for realizing a dc to dc converter in [3]–[5]. The soft commutation is achieved by using phase shift PWM modulation [4], [5] which is having simple control structure and high power density can be achieved. However at high power levels, these components experience considerable current stress. In order to overcome this problem, topologies consisting of three-phase inverter coupled to a three-phase high frequency transformer followed by three-phase high frequency bridge-rectifier have been proposed [6]–[9]. This results in an increase in the input current and output current frequencies by a factor of three as compared to the full bridge converter. This also results in lower current rating for the components and also a considerable reduction in size for the isolation transformer. However, the devices experience high

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voltage stress and the control structure is also quite involved. In an effort to overcome the aforementioned limitations a new converter topology involving three-phase, three-level, (TPTL) phase shifted PWM converter involving six switches operating as zero voltage switching (ZVS) and six switches operating as zero current switching (ZCS) has been presented in this paper. It should be mentioned that in this case soft switching of the semiconductor devices is achieved without taking help from any additional auxiliary circuitry comprising of active or passive elements. In the proposed topology the output rectifier is a center tapped full wave current tripler [10], [11] producing either two or three-level output voltage depending on the operating duty cycle. This leads to considerable reduction in size of the output filter compared to that of the conventional full bridge topology.

II. MODIFIEDTPTL CONVERTER ANDASYMMETRICAL DUTYCYCLECONTROL

Fig.1 shows the circuit configuration of TPTL converter in [19], in which, a three-phase transformer with Δ–Y connection is employed for the smaller turns ratios and transformer VA rating [20]. As shown, L_{ra}, L_{rb} and L_r care the additional resonant inductances to widen the ZVS commutation load range. L_{lka},L_{lkb}, and L_{lkc} are the equivalent primary leakage inductances of each phase. Df1 andDf2 are freewheeling diodes. C_{ss} is the flying capacitor, which is in favor of decoupling the switching transition ofQ_1,Q_3,Q_4, andQ_6. DR1−DR6 are rectifier diodes. The output filter is composed of Lf and C_f, and R_{Ld} is the load.

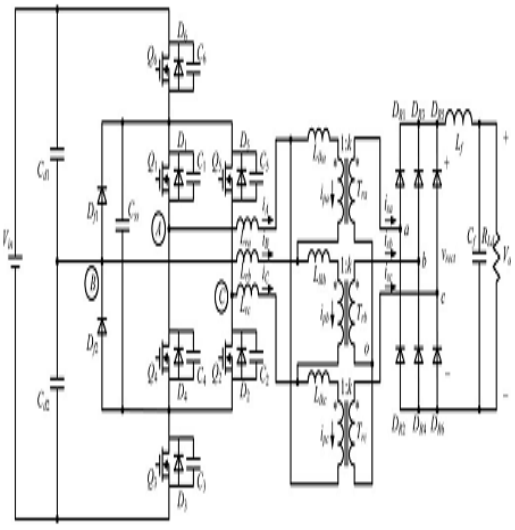

Fig.1. Topology configuration of TPTL dc/dc converter.

Fig.2 shows the switching sequences of the original control strategy and the modified control strategy, as shown in Fig. 2(a), Q1−Q6 are switched on in turn with interval of one-sixth switching period, the duty cycles of all switches are equal, and each switch has a maximum conduction period of 120◦. The required range for the duty cycle of any switch is from 0.167 to 0.33. Obviously, the two interleaved switches have a simultaneous turn-off interval, during which, the intrinsic capacitors of two switches will resonate with the leakage inductances of transformers for several periods. As the duty cycle of the switches varies with the input voltage and the load, the incoming switch cannot be ensured to turn on exactly when its drain-to-source voltage resonates to zero within the operation range; therefore, the switches suffer hard-switching and a considerable switching loss occurs. To realize the soft-switching for switches, the original interleaved switches should be designed in a complementary manner, and a short delay time t_d is necessary to be introduced between the two complementary switches to provide an interval for the ZVS commutation, which is similar to the control strategy of asymmetrical half-bridge converter. Accordingly, the duty cycles ofQ1,Q3, andQ5are served to regulate the output voltage, while the drive signals ofQ4,Q6, and Q2 are complementary to that of theQ1,Q3, and Q5, respectively. The obtained control strategy is illustrated in Fig. 2(b).

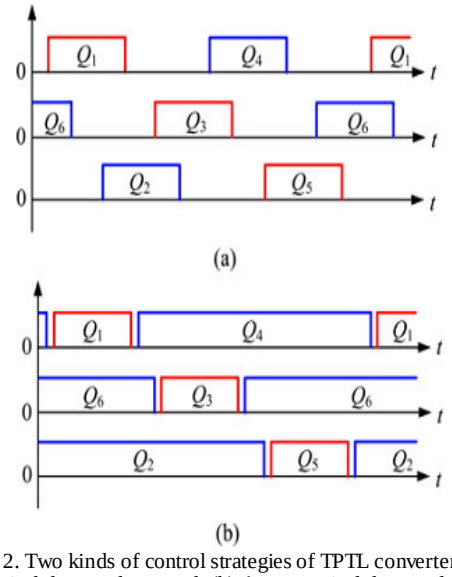

Fig. 2. Two kinds of control strategies of TPTL converter. (a) Symmetrical duty cycle control. (b) Asymmetrical duty cycle control.

III. OPERATION PRINCIPLE

This section will analyze the operation principles of the TPTL converter under the modified control scheme.

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The following assumptions are made for the simplicity before the analysis:

1) all power devices and diodes are ideal;

2) all capacitors and inductances are ideal;

3) the output filter inductance is large enough to be treated as a constant current source during a switching period; its value equals to output current Io;

4) the inductances of each phase are identical, i.e., $L_{lka} = L_{lkb} = L_{lkc} = L_{lk}, L_{ra} = L_{rb} = L_{rc} = L_r$;

5) $C_1 = C_2 = C_3 = C_4 = C_5 = C_6 = C_p$.

Fig. 3 shows the key waveforms of the TPTL converter with asymmetrical duty cycle control, as seen, the operation of the TPTL converter can be classified by different modes, according to the duty cycle range and the load current. The corresponding operation modes are defined as the small duty cycle mode (SDCM), the medium duty cycle mode (MDCM), and the large duty cycle mode (LDCM), respectively, when the duty cycle varies between (0, 1/3), (1/3,Dr), and(Dr, 1/2), where Dr is a critical duty cycle that depends on the load current and the parameters of converter. The related waveforms in different operation modes are referred to Fig. 3(a)–(c). For simplicity, only the operation principle under SDCM will be described in this paper. As shown in Fig. 3(a), the converter has 18 operation stages during a switching period.

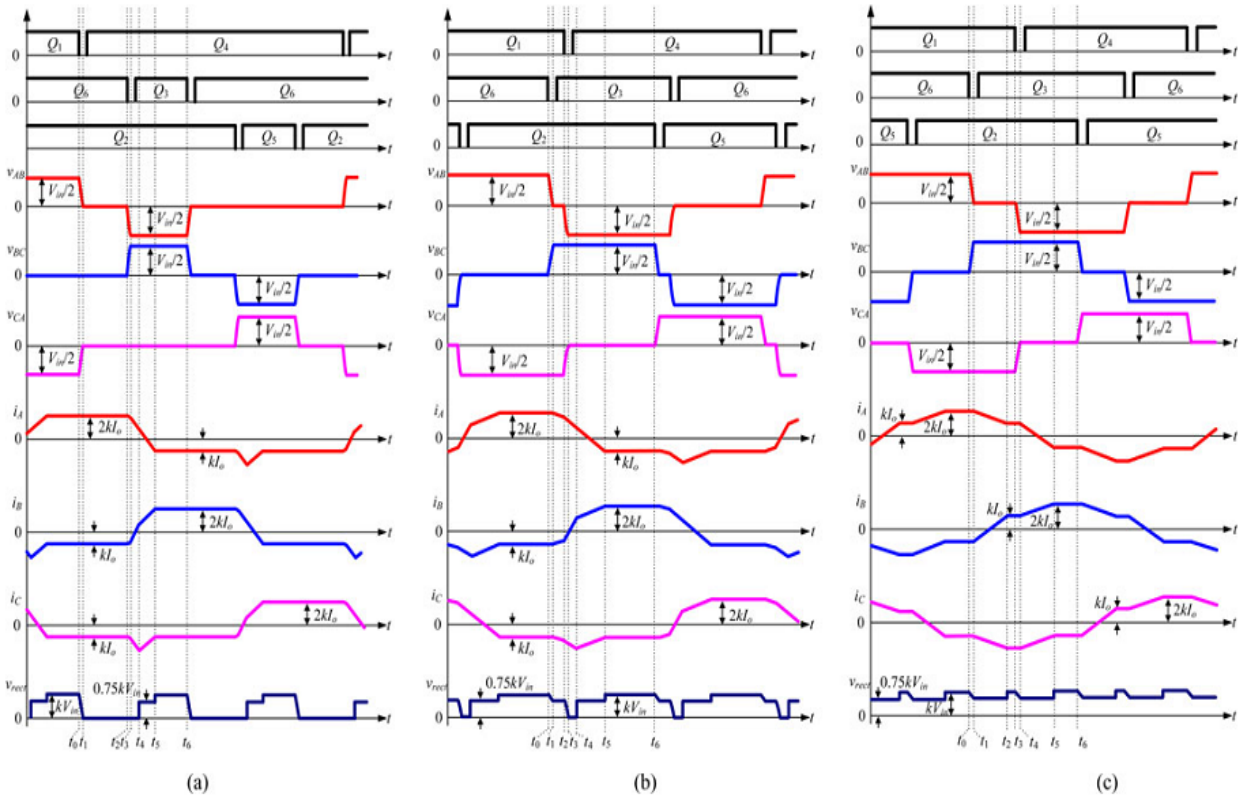

Fig.3. Key waveforms of the TPTL converter with asymmetrical duty cycle control. (a) SDCM. (b) MDCM. (c) LDCM

Fig. 4 shows seven operation stages of the converter under rated conditions. The other operation stages during the rest of a switching period are not depicted but they are symmetrically equivalent, expect for the fact that they are phase shifted.

The basic equations of the voltages and currents of the transformer are listed as follows:

$$v_{AB} + v_{BC} + v_{CA} = 0 \tag{1}$$

$$i_{sa} + i_{sb} + i_{sc} = 0 \tag{2}$$

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$$\frac{di_{pa}}{dt} = k\frac{di_{sa}}{dt} = \frac{v_{Llka}}{L_{lk}},\ \frac{di_{pb}}{dt} = k\frac{di_{sb}}{dt} = \frac{v_{Llkb}}{L_{lk}},\ \frac{di_{pc}}{dt} = k\frac{di_{sc}}{dt} = \frac{v_{Llkc}}{L_{lk}} \quad (3)$$

Where k represents the secondary-to-primary turns ratios of the transformer. The voltage across the leakage inductance of transformer can be derived from (2) and (3) and is given as follows:

$$v_{Llka} + v_{Llkb} + v_{Llkc} = 0. \quad (4)$$

Stage1 [prior to t_0] [see Fig. 3.4(a)]: Prior to t0, Q_1, Q_2, Q_6, and $D_{f2}$are conducting at the primary side, andDR1andDR6 are conducting at the secondary side. v_{AB}=Vin/2, v_{BC}=0, and v_{CA}=−Vin/2. From (1), (2), (4), and other constraints between voltages and currents of transformers, the following expressions can be obtained:

$$v_{pa} = \frac{V_{\text{in}}}{2}, \qquad v_{pb} = 0, \qquad v_{pc} = -\frac{V_{\text{in}}}{2} \quad (5)$$

$$v_{\text{rect}} = v_{sa} - v_{sc} = k \cdot V_{\text{in}} \quad (6)$$

Where v_{pi} and v_{si} are the primary voltage and secondary voltage of transformers, I represents the subscripts a, b, and c.

Stage 2 [t_0,t_1] [see Fig. 4(b)]:At t_0,Q_1 is turned off, the line current $i_A$chargesC_1 and dischargesC_4 linearly, and the rectified voltage decreases. As C_1 limits the rising rate of the voltage acrossQ_1, Q_1 is zero-voltage turn-off. The voltages across$C_1$and C_4 are

$$v_{C1}(t) = \frac{1}{C_p} \cdot k \cdot I_o \cdot (t - t_0) \quad (7)$$

$$v_{C4}(t) = \frac{V_{\text{in}}}{2} - \frac{1}{C_p} \cdot k \cdot I_o \cdot (t - t_0) \quad (8)$$

At t_1,v_{C1} rises to V_{in}/2, and v_{C4} decays to zero; therefore, D_4conducts naturally, and v_{rect} decreases to zero.

Stage3[t_1,t_2] [see Fig. 4(c)]:After C_1 is fully charged, the current flowing throughC_1 transfers to C_{ss} and begins to charge C_{ss}. The voltage across C_{ss} will increase and blockDf2 to be off. During this stage, v_{AB}=v_{BC}=v_{CA}=0. D_4 conducts and clamps the voltage across Q_4 at zero, so Q_4 can be turned on at zero-voltage condition. D_{R1} and D_{R6} conduct, and v_{rect} is still zero.

Stage4[t2,t3] [see Fig. 4(d)]: At t2, Q6 is zero-voltage turned-off, and vAB increases reversely. If vpa keeps constant, the polarity of the voltage applied on Llka will be non associated with the current flowing through Llka; as a result, ipa will decrease and cannot provide the load current, then DR3 begins to conduct, and the current commutation between DR1 and DR3 occurs. In the primary stage,C3 and C6 resonate with the leakage inductances and the resonant inductances, and the following expressions will be obtained:

$$v_{C3}(t) = \frac{V_{\text{in}}}{2} - \frac{1}{2}k \cdot I_o \cdot Z_r \cdot \sin\left[\omega_r (t - t_2)\right] \quad (9)$$

$$v_{C6}(t) = \frac{1}{2}k \cdot I_o \cdot Z_r \cdot \sin\left[\omega_r (t - t_2)\right] \quad (10)$$

$$i_A(t) = \frac{3}{2}k \cdot I_o + \frac{1}{2}k \cdot I_o \cdot \cos\left[\omega_r (t - t_2)\right] \quad (11)$$

$$i_B(t) = -k \cdot I_o \cdot \cos\left[\omega_r (t - t_2)\right] \quad (12)$$

$$i_C(t) = -\frac{3}{2}k \cdot I_o + \frac{1}{2}k \cdot I_o \cdot \cos\left[\omega_r (t - t_2)\right] \quad (13)$$

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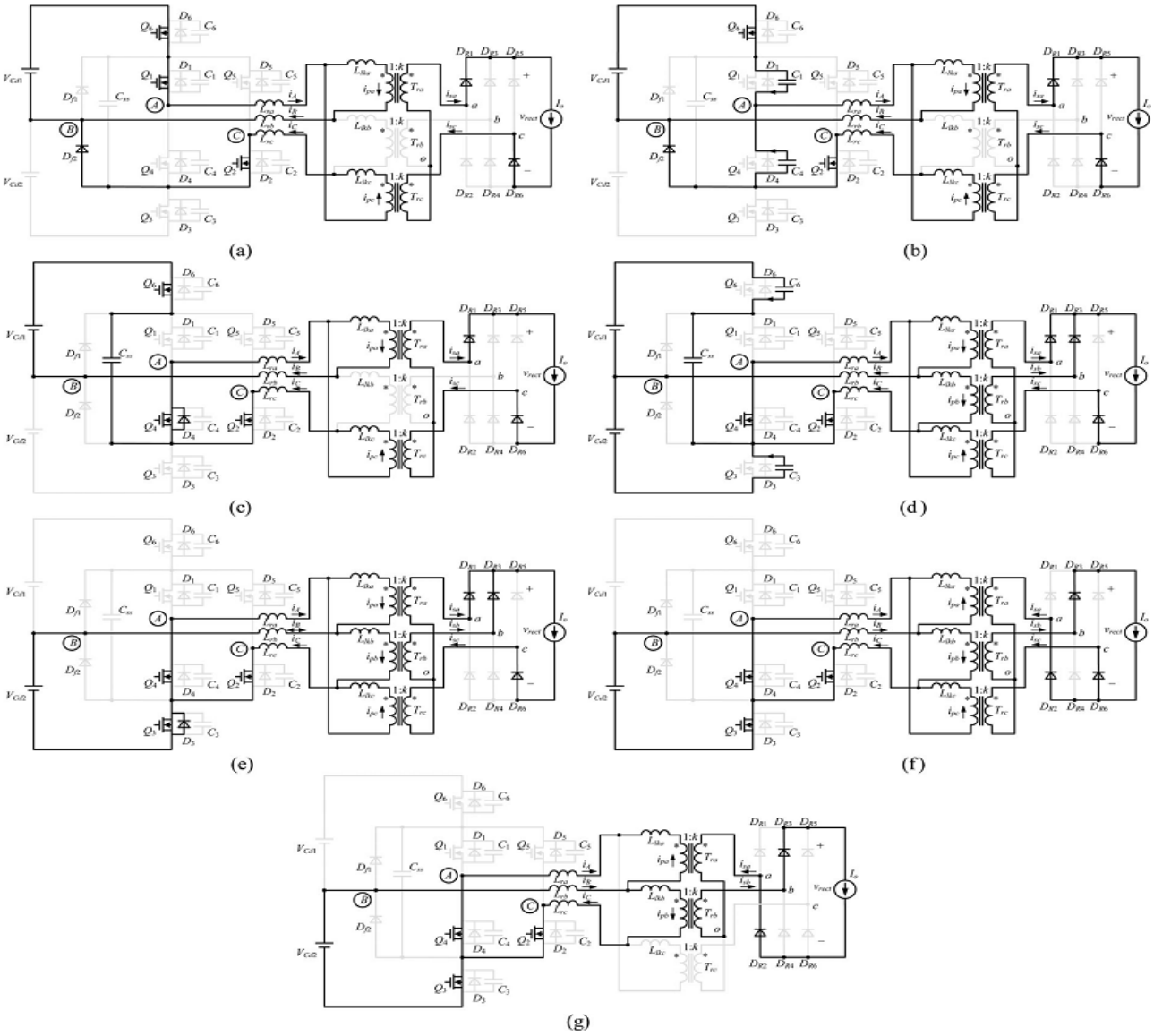

Fig. 4. Equivalent circuits under different operation stages. (a) Prior tot$_0$.(b)[t_0,t_1]. (c)[t_1,t_2]. (d)[t_2,t_3]. (e)[t_3,t_4]. (f)[t_4,t_5]. (g)[t_5,t_6].

Where $Z_r = \sqrt{L_p/C_p}, \omega_r = \sqrt{1/(L_p \cdot C_p)}$ and L_p $=L_{lk}+3L_r$. During this stage, v_{rect} remains at zero. When v_{C3} decays to zero, D_3 conducts naturally.

Stage 5 [t_3,t_4] [see Fig. 4(e)]: As D_3 is conducting, the voltage across Q_3 is clamped at zero; therefore, Q_3 is turned on at zero-voltage condition. During this stage, Q_2, Q_3, and Q_4 conduct in the primary stage, v_{AB}=−Vin/2,v_{BC}=Vin/2, and v_{CA}=0. D_{R1}, D_{R3}, and D_{R6} conduct in the secondary stage, and v_{rect} =0. From (3.1), (3.2), (3.4), and other constraints between voltages and currents of transformers, the expressions of the phase currents are given in (3.14)–(3.16)

$$i_{pa}(t) = i_{pa}(t_3) - \frac{V_{\text{in}}}{2L_p} \cdot (t - t_3) \quad (14)$$

$$i_{pb}(t) = i_{pb}(t_3) + \frac{V_{\text{in}}}{2L_p} \cdot (t - t_3) \quad (15)$$

$$i_{pc}(t) = -kI_o \quad (16)$$

Stage 6[t_4,t_5] [see Fig. 4(f)]: During this stage, v_{AB}=−Vin/2, v_{BC}=Vin/2, v_{CA}=0. From the constraints between voltages and currents of transformers, the following expressions can be obtained:

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$$i_A(t) = k \cdot I_o - \frac{V_{\text{in}}}{2L_p} \cdot (t - t_4) \quad (17)$$

$$i_B(t) = k \cdot I_o + \frac{V_{\text{in}}}{4L_p} \cdot (t - t_4) \quad (18)$$

$$i_C(t) = -2k \cdot I_o + \frac{V_{\text{in}}}{4L_n} \cdot (t - t_4) \quad (19)$$

I_{sc} flows through D_{R6}, i_{sc} and decreases with i_{pc}. When i_{sc} decreases to zero,D_{R6} turns off, the primary and secondary currents of transformer T_{rc} are both zero. The time interval of this stage is given by

$$t_{45} = \frac{4k \cdot I_o \cdot L_p}{V_{\text{in}}} \quad (20)$$

Hereafter,Q_2, Q_3, and Q_4conduct at the primary side, while DR2 andDR3 conduct at the secondary side, and the rectified voltage is k V_{in}, which is similar to the stage 1.

IV.THEORETICALANALYSIS

A. Input Capacitor Balancing Analysis

It has been known that by using PWM to control the converter, the input capacitor balancing is a function of the duty cycle and the charging/discharging current. If the symmetrical duty cycle control is utilized, each input capacitor presents one-half of the input voltage. While using an asymmetrical duty cycle control, an analysis of the input capacitor energy must be made. Fig. 5 shows the ideal charging/discharging waveforms for the input capacitor under different operation modes, in which the influence of the leakage inductance and the resonant inductance are omitted without detriment to the analysis. Table I presents the steady-state analysis of the input capacitors energy during the power transfer stages. In this analysis it is assumed that the load current is constant in a switching period. The symbol "↑" means that the capacitor is delivering energy, therefore, its voltage is decreasing, while "↓" means that the capacitor is receiving energy and its voltage is increasing. From Fig. 5 and Table I, it can be seen that the capacitorCd1 is discharged in the interval ΔT_1 and is charged in the interval ΔT_2; here,$\Delta T_2=2\Delta T_1$and the charging current is one-half of the discharging current. The opposite operation occurs in Cd_2.

As a result, the total energy variations of input capacitors are equal to zero, considering that the amount of energy variations is equal in two intervals. Therefore, during a switching period the total voltage variation in each input capacitor is equal to zero, and all input capacitors voltages remain equal to one-half of the input voltage.

TABLE I
ENERGY BALANCE OF INPUT CAPACITORS UNDER DIFFERENT OPERATION MODES

Small duty cycle mode			Medium duty cycle mode		
Time interval	ΔT_1	ΔT_2	Time interval	ΔT_1	ΔT_2
C_{d1}	↑	↓	C_{d1}	↑	↓
C_{d2}	↓	↑	C_{d2}	↓	↑
Total energy	0	0	Total energy	0	0

B. Output Filter Inductance

With three-phase architecture, the converter with modified control strategy can reduce the output current ripple and further minimize the output filter requirement. Figs. 6 and 7 show the waveforms of the rectified voltage vrect and the output filter inductance current iLf under SDCM and MDCM, respectively. From Figs. 6 and 7, the expressions of the output filter inductance are given in (3.31)

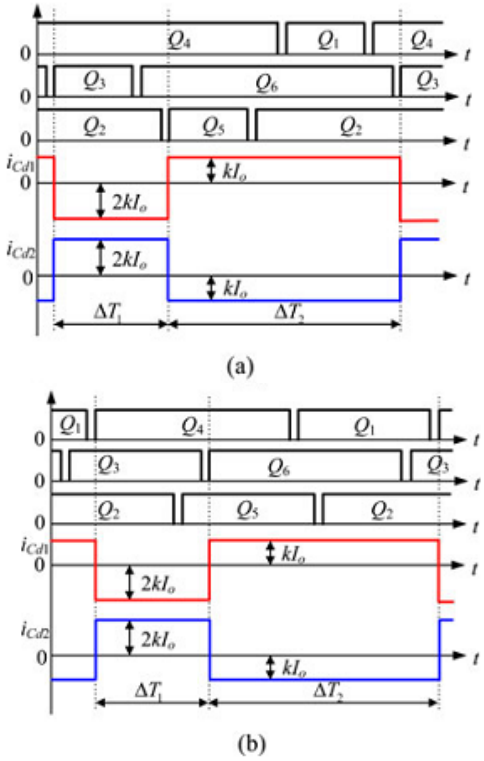

Fig. 5. Ideal charging/discharging waveforms under different operation modes. (a) SDCM. (b) MDCM.

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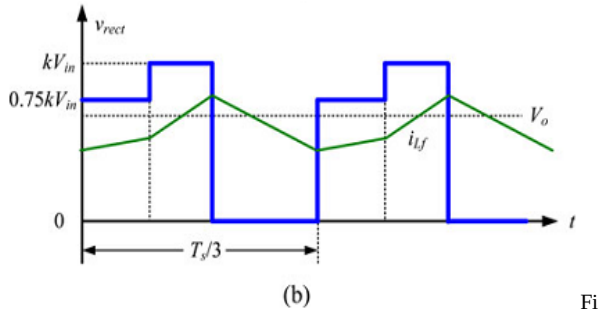

Fig. 6. Waveforms of the rectified voltage and output filter inductance current under SDCM. (a)0.75kVin <Vo <kVin.(b)Vo <0.75kVin

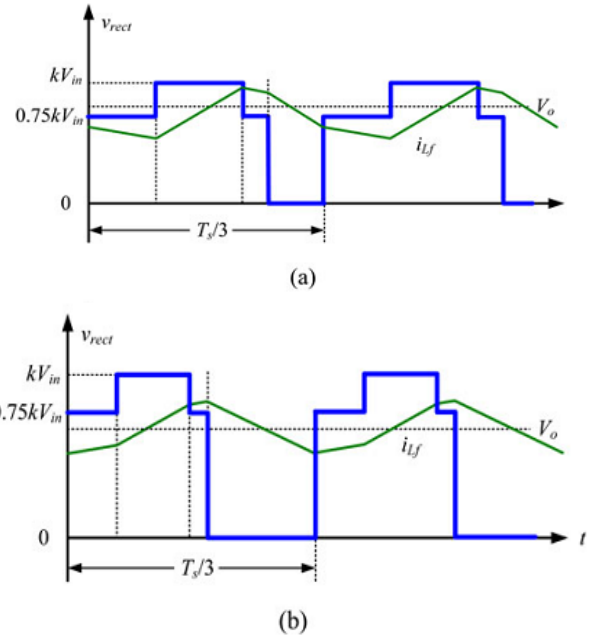

Fig.7. Waveforms of the rectified voltage and output filter inductance current under MDCM. (a)0.75kVin <Vo <kVin.(b)Vo <0.75kVin.

To illustrate the good performance of the proposed converter, the half-bridge TL converter is adopted to make the comparison. The output filter inductance of half-bridge TL converter is

$$L_{f\_HB} = \frac{V_o \cdot (1 - 2V_o / k_{HB} \cdot V_{\text{in}})}{2\Delta i_{Lf} \cdot f_s}. \quad (21)$$

Where k_{HB} is the turns ratio of the transformer in half-bridge TL converter, k_{HB}=4Vo/(Vinmin· DHBmax), and DHB max is the maximum duty cycle that is set at 0.45. Fig. 8 shows quantitatively the savings in the inductance requirement as a function of the range of input variation, and the Y-coordinate is the ratio of L_f TP to the maximum Lf HB, where input voltage Vin =540–660 V, output voltage Vo=48 V, output current Io =20 A, switching frequency fs =50 kHz, and Δi_{Lf} =4 A. As shown, the TPTL converter with modified control scheme can save the output filter inductance effectively, which is reduced by a factor of about 52% compared with the half-bridge TL converter.

D. Current Stress and Voltage Stress on Switches

To demonstrate the reduction of current stress on switches under the modified control strategy, the ideal current waveforms of switches in different operation modes are illustrated in Fig. 9, in which the leakage inductance and the current ripple of output filter inductance are neglected. From Fig. 9, the rms current through the switches I_{rms} under rated load are given by

$$I_{rms\_Q1} = \begin{cases} k \cdot I_o \cdot \sqrt{4D - D_{\text{loss1}}} & (\text{SDCM}) \\ k \cdot I_o \cdot \sqrt{1 + D - D_{\text{loss2}}} & (\text{MDCM}) \end{cases} \quad (22)$$

$$I_{rms\_Q4} = \begin{cases} k \cdot I_o \cdot \sqrt{2 - 4D + D_{\text{loss1}}} & (\text{SDCM}) \\ k \cdot I_o \cdot \sqrt{1 - D + D_{\text{loss2}}} & (\text{MDCM}) \end{cases} \quad (23)$$

Likewise, the half-bridge TL converter could be used for comparison. If the phase-shifted control is employed, the rms current through the switches will be given by

$$I_{rms\_HB} = k_{HB} \cdot I_o \cdot \sqrt{\frac{1}{2}}. \quad (24)$$

Using the specifications given previously, Fig. 10 illustrates quantitatively the savings in the rms current through switches as a function of input variation range, and the Y-coordinate is the ratio of I_{rms} to the I_{rms} HB. As shown, the rms current through power switches can be reduced compared with the half bridge TL converter, which means that the switches can sustain higher power in the modified TPTL converter. Meanwhile, the two complementary switches suffer different current stresses due to the asymmetrical duty cycle, and it should be considered in the practical design.

As for the voltage ratings on switches, thanking for the TL configuration and the automatic voltage balancing of input capacitors, the voltage stress on power switches will be limited at half of the input voltage, so the converter is suitable for high input voltage applications.

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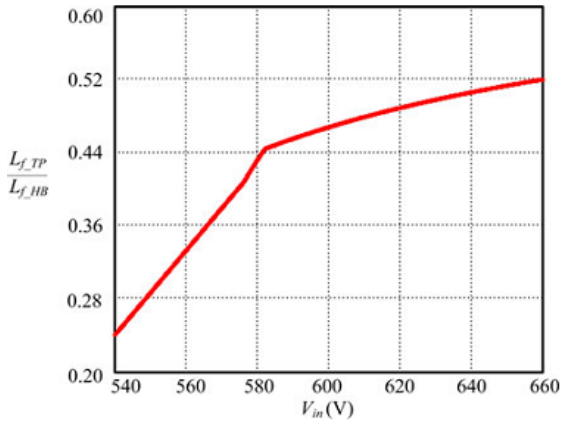

Fig.8. Ratio of $L_{f\,TP}$ and $L_{f\,HB}$ versus the input voltage

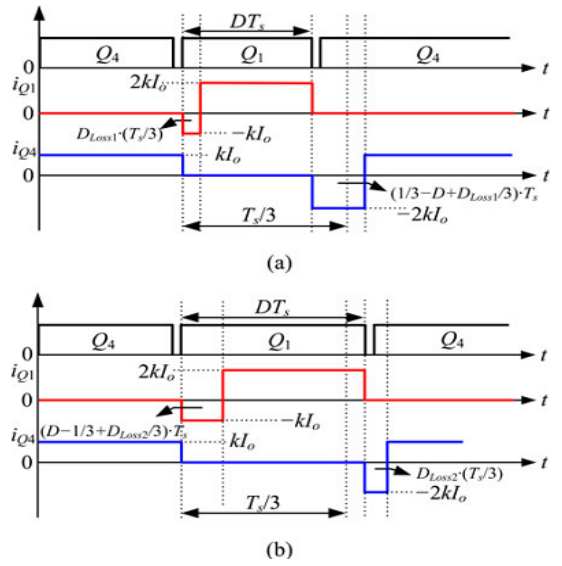

Fig.9. Ideal current waveforms of switches. (a) SDCM. (b) MDCM

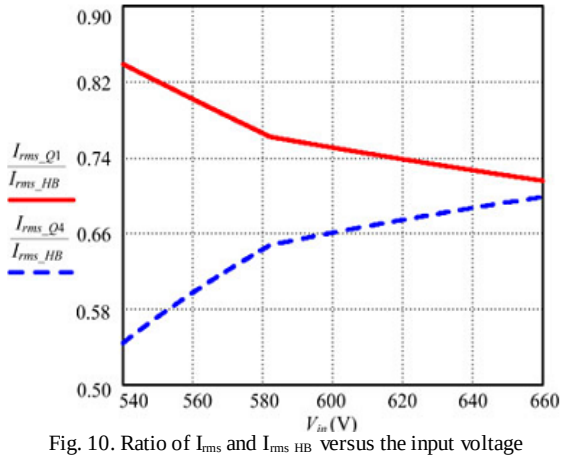

Fig. 10. Ratio of I_{rms} and $I_{rms\ HB}$ versus the input voltage

E. Conditions for Soft-Switching Realization

In order to achieve ZVS for the switches, enough energy is needed to fully charge/discharge the intrinsic capacitors of the switches prior to turning on the switches. Due to the different operation principles in two modes, the converter presents different ZVS characteristics. 1) SDCM: During the transition of Q_2, Q_4, and Q_6, as seen in Fig. 3(a), the charging currents for the intrinsic capacitors are proportional to the reflected load current, thus the voltage across the switches varies linearly, and the energy to achieve ZVS for the three switches is provided by the output filter inductance. To ensure zero-voltage turn-on, the intrinsic capacitor of the incoming switch should be fully discharged by the line current during the delay time. From (8), it can be known that the ZVS condition will be lost if the load current is below $Io_{\ minQ2(Q4,Q6)}$ expressed by

$$I_{o\_\min\_Q_2(Q_4,Q_6)} = \frac{V_{\text{in}} \cdot C_p}{2t_d \cdot k} \tag{25}$$

During the commutation Q_1, Q_3, and Q_5, the resonant inductances and the leakage inductances resonate with the intrinsic capacitors of these switches, and only the energy stored in the resonant inductances and the leakage inductances are used to achieve zero-voltage turn-on. From (3.9) and (3.10), the minimum load current to realize ZVS for Q_1, Q_3, and Q_5 is given by

$$I_{o\_\min\_Q_1(Q_3,Q_5)} = \frac{V_{\text{in}}}{Z_r \cdot k}. \tag{26}$$

The minimum load current to achieve ZVS under SDCM as the function of the input voltage is depicted in Fig. 11, from which we can see thatQ2,Q4, and Q6 can realize ZVS easier compared with Q1,Q3, and Q5, and the ZVS load range for Q1,Q3, and Q5 can be widen by increasing the resonant inductances.

2) MDCM: Similarly, from Fig. 3(b), the minimum load currents to achieve ZVS for switches under MDCM are given by

$$I_{o\_\min\_Q_1(Q_3,Q_5)} = \frac{V_{\text{in}} \cdot C_p}{t_d \cdot k} \tag{27}$$

$$I_{o\_\min\_Q_2(Q_4,Q_6)} = \frac{\sqrt{3}V_{\text{in}}}{4Z_{r1} \cdot k} \tag{28}$$

where $Z_{r1} = \sqrt{L_p/4C_p}$

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It should be noted that the critical point between SDCM and MDCM depends on the duty cycle and the load current according to (3.30). Substituting D=1/3 into the second expression in (3.30), the minimum load current that ensures the converter to operate under MDCM is given by

$$I_{o\_\min} = \frac{k \cdot V_{\text{in}} - V_o}{9k^2 \cdot L_p \cdot f_s} \qquad (29)$$

Fig. 4.12 illustrates the minimum load currents in (38)–(40) as a function of the input voltage, which indicates that the switches can realize ZVS within the operation range in MDCM, considering the minimum load current to satisfy the requirement of MDCM is larger than the minimum load current to achieve ZVS

F. Considerations on Dynamic Behavior of Modified Converter

The modified TPTL converter has almost the same problems to closing the feedback loop as the asymmetrical half-bridge converters. The phase lag caused by the double pole–double zero of the transfer function can cause stability problems, for the phase margin is small or even null under some loads. In the practical design, the following considerations should be emphasized to achieve a better dynamic performance: 1) Combination of multilayer capacitors in parallel with electrolytic capacitors in the input capacitor design. The combination of both type of capacitor can dump the effect of the double-pole double-zero effectively. 2) A lead–lag controller should be introduced into the closed-loop design, which put both zeros of the lead–lag controller at a frequency below the double-pole frequency. Thus, the phase margin at the frequencies near the double pole–double zero effect is quite large. With the lead–lag controller, the modified converter can achieve a larger phase margin and a higher band-width than that with a single PI controller, which will be favorable to obtain a more stable steady behavior and a faster dynamic response.

Proposed Concept with 5 level converter:

The 5 level converter reduces the harmonics, when it was first used in a three-level converter in which the mid-voltage level was defined as the neutral point. The 5 level converter uses capacitors in series to divide up the dc bus voltage into a set of voltage levels. To produce m levels of the phase voltage, an m level 5 level converter needs m-1 capacitors on the dc bus. A single-phase five-level converter is shown in Fig. 1.9. The dc bus consists of four capacitors, i.e., C1, C2, C3, and C4. For a dc bus voltage *Vdc*, the voltage across each capacitor is *Vdc*/4, and each device voltage stress will be limited to one capacitor voltage level, *Vdc*/4, through clamping diodes. DCMI output voltage synthesis is relatively straightforward.

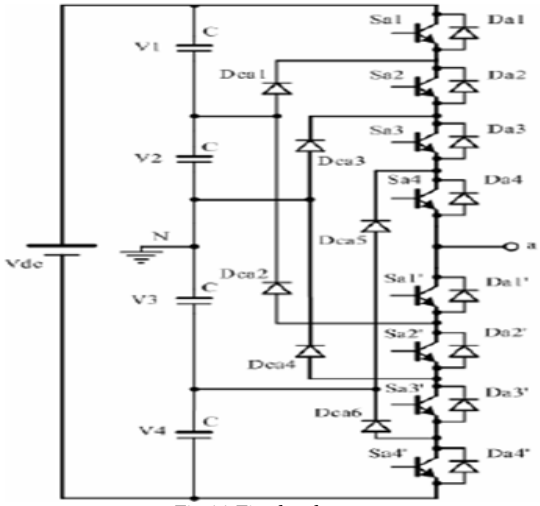

Fig.11.Five level converter

To explain how the staircase voltage is synthesized, point O is considered as the output phase voltage reference point. Using the five-level converter shown in Fig. 1.10, there are five switch combinations to generate five level voltages across A and O. Table 2.2 shows the phase voltage level and their corresponding switch states. From Table 2.2, state 1 represents that the switch is on, and state 0 represents the switch is off. In each phase leg, a set of four adjacent switches is on at any given time. There exist four complimentary switch pairs in each phase, i.e., Sa1-Sa1', Sa2-Sa2', and Sa4-Sa4'.

Table II: five-level converter voltage levels and their switch st*ates*

Output V_{AO}	Switch state							
	S_{a1}	S_{a2}	S_{a3}	S_{a4}	$S_{a1'}$	$S_{a2'}$	$S_{a3'}$	$S_{a4'}$
$V_5=V_{dc}$	1	1	1	1	0	0	0	0
$V_4=3V_{dc}/4$	0	1	1	1	1	0	0	0
$V_3=V_{dc}/2$	0	0	1	1	1	1	0	0
$V_2=V_{dc}/4$	0	0	0	1	1	1	1	0
$V_1=0.$	0	0	0	0	1	1	1	1

PRINCIPLE OF BLDC MOTOR

BLDC engine comprises of the perpetual magnet rotor and an injury stator. The brushless engines are controlled utilizing a three stage inverter. The

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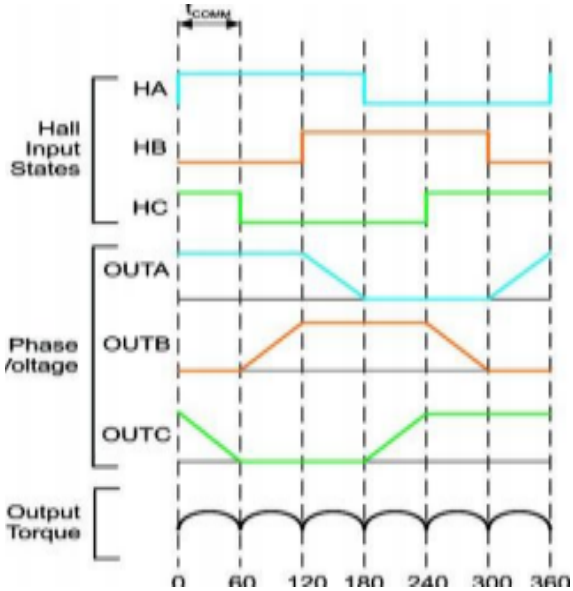
engine obliges a rotor position sensor for beginning and for giving legitimate compensation arrangement to turn on the force gadgets in the inverter extension. In light of the rotor position, the force gadgets are commutated consecutively every 60 degrees. The electronic compensation takes out the issues connected with the brush and the commutator plan, in particular starting and destroying of the commutator brush course of action, along these lines, making a BLDC engine more rough contrasted with a dc engine. Fig.1 demonstrates the stator of the BLDC engine and fig.2 shows rotor magnet plans.

BLDC motor stator construction

BLDC motor Rotor construction

The brush less dc engine comprise of four fundamental parts Power converter, changeless magnet brushless DC Motor (BLDCM), sensors and control calculation. The force converter changes power fro m the source to the BLDCM which thus changes over electrical vitality to mechanical vitality. One of the remarkable highlights of the brush less dc engine is the rotor position sensors, in view of the rotor position and order signals which may be a torque charge, voltage summon, rate order etc; the control calculation s focus the entryway sign to every semiconductor in the force electronic converter.

The structure of the control calculations decides the sort of the brush less dc engine of which there are two principle classes voltage source based drives and current source based drives. Both voltage source and current source based commute utilized for perpetual magnet brushless DC machine. The back emf waveform of the engine is demonstrated in the fig. 3. Be that as it may, machine with a non sinusoidal back emf brings about diminishment in the inverter size and lessens misfortunes for the same influence level.



Hall signals & Stator voltages

V. MATLAB/SIMULINK RESULTS

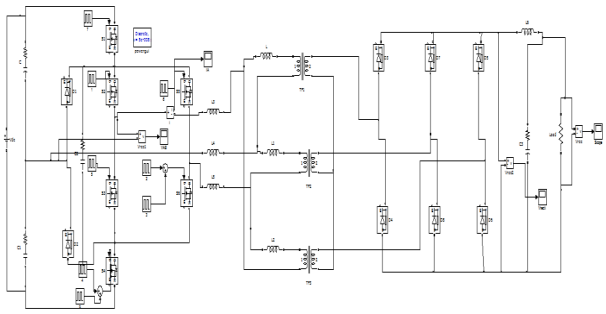


Fig.12.Simulation result for TPTL dc/dc converter

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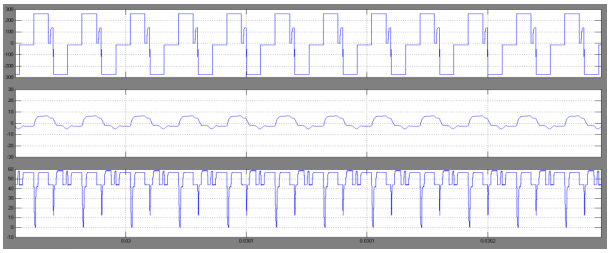


Fig.13.Simulation result for Vab , Ia, Vrect at medium duty cycle mode (MDCM)

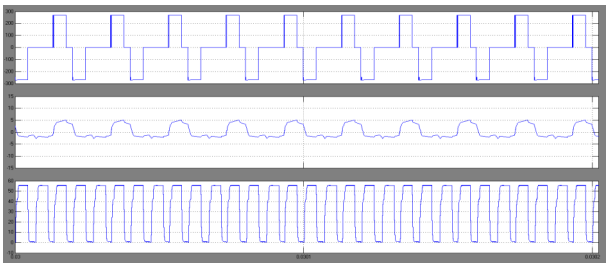


Fig.14.Simulation result for Vab , Ia, Vrect at small duty cycle mode (SDCM)

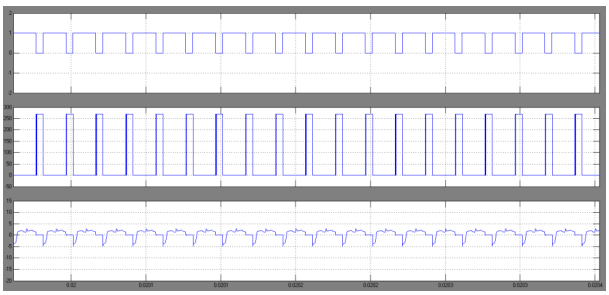


Fig.17.Simulation result for gate signal, Vds and Id for Q2 for SDCM

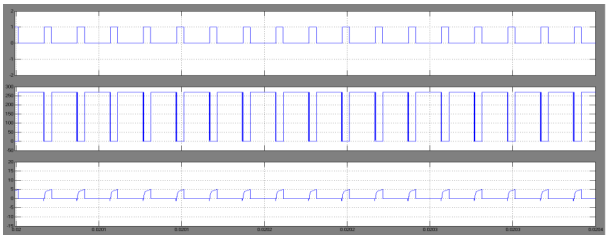
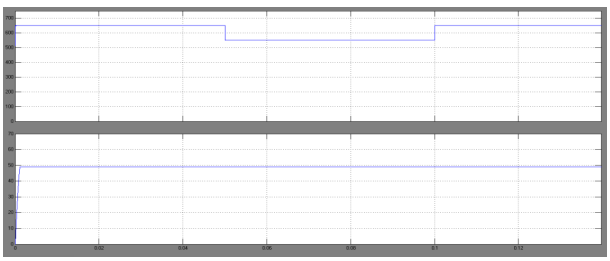


Fig.18.Simulation result for gate signal, Vds and Id for Q5 for SDCM



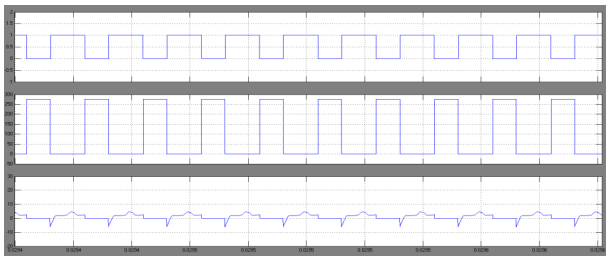


Fig.15.Simulation result for gate signal, Vds and Id for Q2 for MDCM

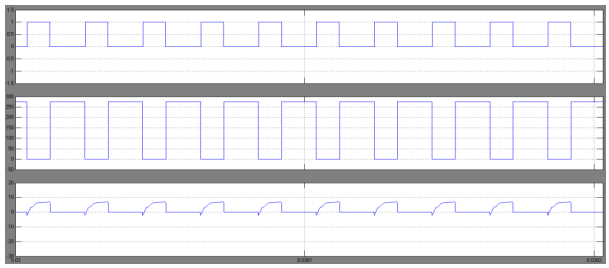


Fig.16.Simulation result for gate signal, Vds and Id for Q5 for MDCM

Fig.19.Simulation result for input and output voltage during step change in voltage

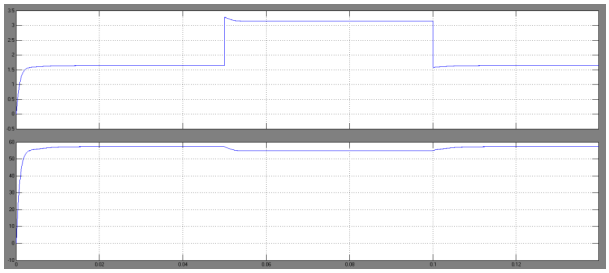


Fig.20. Simulation result for input and output voltage during step change in current

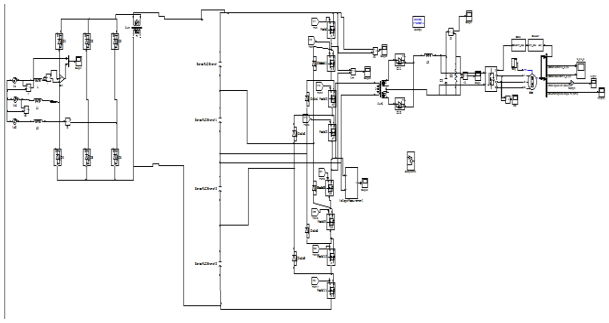


Fig.21.Simulink design for five level converters with BLDC Motor

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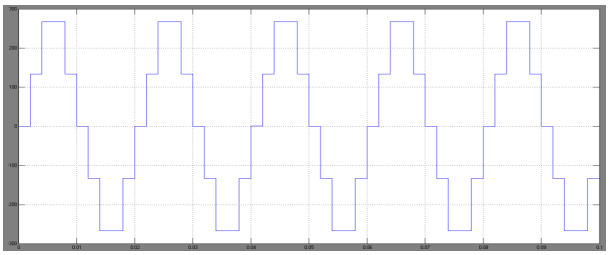

Fig.22.Simulation result for five level converter

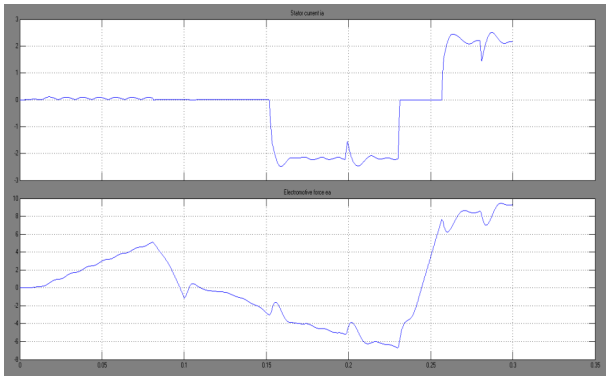

Fig.23.Simulation result for stator current and electromagnetic current

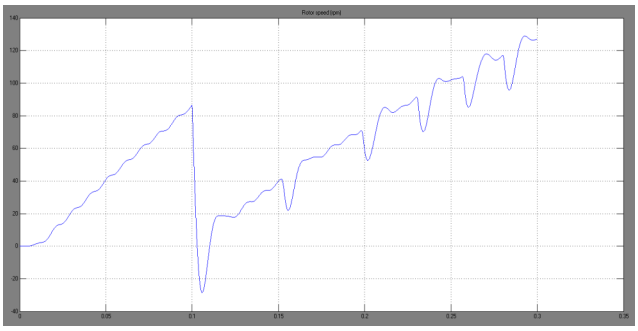

Fig 24 simulation wave form of BLDC motor speed

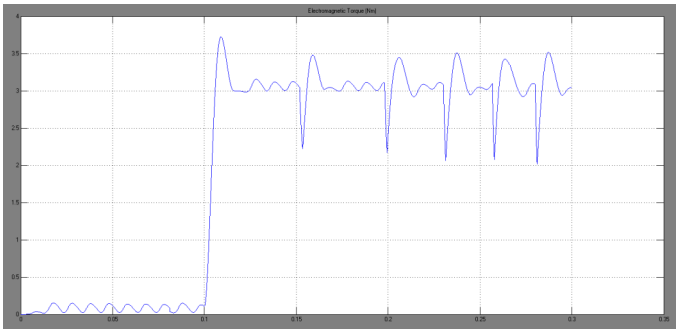

Fig 25 simulation wave form of BLDC motor torque

VI. CONCLUSION

A modified asymmetrical duty cycle control strategy with ZVS capability was proposed for the TPTL converter in this paper. The proposed control scheme features are- Compared with the symmetrical duty cycle control, the dominant advantages can be maintained including the lower power rating of switches and the reduced output filter requirement. The input capacitors can realize automatic and inherent voltage balancing, which ensures that all the switches sustain only one-half of the input voltage. The TPTL converter will operate in three operation modes along with the variation of duty cycle and output current, i.e., SDCM, MDCM in which, the output voltage cannot be modulated under LDCM. Three level converters has higher harmonic order so we replaced with five level converter with BLDC motor drive for reduction of harmonics and analysis to speed ,current and torque

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