International Journal of Research
Available at https://edupediapublications.org/journals
p-ISSN: 2348-6848
e-ISSN: 2348-795X
Volume 03 Issue 12
August 2016

Implementation of Parallel-Prefix Adders using Reverse Converter

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Abstract:

In this project, the implementation of residue number system reverse converters based on well-known regular and modular parallel prefix adders is analyzed. The VLSI implementation results show a significant delay reduction and area × time2 improvements, all this at the cost of higher power consumption, which is the main reason preventing the use of parallel-prefix adders to achieve high-speed reverse converters in nowadays systems. Hence, to solve the high power consumption problem, novel specific hybrid parallel-prefix-based adder components that provide better tradeoff between delay and power consumption are here in presented to design reverse converters. A methodology is also described to design reverse converters based on different kinds of prefix adders. This methodology helps the designer to adjust the performance of the reverse converter based on the target application and existing constraints.

I. INTRODUCTION

The Residue Number System plays a significant role in the battery based and portable devices because of its low power features and its competitive delay. The Residue number system reverse converter is designed with parallel prefix addition by

using new components methodology for higher speed operation[1].The RNS consists of two main components forward and the reverse converter that are integrated with the existing digital system. The forward converter performs the operation of converting the binary number to the modulo number whereas the reverse converter performs the operation of reverse converting the modulo number to the binary number which is the hard and time consuming process compared with the forward converter. The fundamental RNS concepts such as 1)RNS definition with properties and their applications,2)consideration of modulo set selection,3)design of forward converter,4)modulo arithmetic units,4)design of reverse converter are discussed[2]. The voltage over scaling (VOS) technique is applied to the residue number system to achieve high energy efficiency.

The VOS technique introduces soft errors which degrades the performance of the system. To overcome these soft errors a new technique is implemented called joint RNS-RPR (JRR) which is the combination of RNS and the reduced precision redundancy. This method provides the advantage of satisfying the basic properties of RNS includes shorter critical path, reduced complexity and low power[3].New architectures are presented for the moduli sets(2n-1,2n,2n+1) for the conversion from the residue to the binary equivalents[4].Here the speed and the cost are major concern. Distributed arithmetic principles are used to perform the inner product computation in[5].The input data which are in the residue domain which are encoded using the Thermometer code format and the outputs are encoded using the One hot code format. Compared to the conventional method which used Binary code format, the proposed system which achieves higher operating speed.

The residue number system which provides carry free addition and fully arithmetic operation [6], for several applications such as digital signal processing and cryptography[7]-[11]. In this brief, we present a comprehensive method which uses the parallel prefix adder in selected position, thereby using the shift operation on one bit left to design a multiplier on the same design

module to achieve a fast reverse converter design. The usage on parallel prefix structure in the design leads to higher speed in operation meanwhile it increases the area and power consumption. In order to compensate the tradeoff between the speed, area and power consumption, a novel specific hybrid parallel prefix based adder components are used to design the reverse converter. These hybrid design which provides the significant reduction in the power delay product (PDP)metric and leads to considerable improvements in the area x time² product(AT^2) in comparison with the traditional converters without using parallel prefix adders.

II. PARALLEL PREFIX STRUCTURE

The Residue number system mainly composed of three main parts such as, forward converter, modulo arithmeticunits and reverse converter. On comparing with the other parts the reverse converter design is a complex and non modular structure. So more attention is needed in designing the reverse converter thereby preventing the slow operation and compromise the benefits of the RNS. The parallel prefix structure helps to achieve the faster operation in the reverse converter design but causes increased power consumption. In the existing system the novel specific hybrid parallel prefix adder based components are used to replace the existing components thereby reducing the power consumption and getting faster operation.

A. Parallel Prefix Block

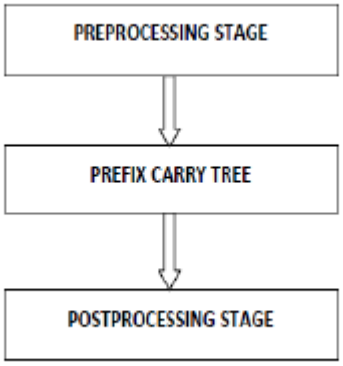

Fig.1. Basic Parallel prefix structure.

The Parallel prefix structure consists of three main blocks, they are preprocessing block, prefix carry tree and post processing block. The parallel prefix adder operation begins with preprocessing stage by generating the Generate (Gi) and Propogate (Pi) equation [1] & [3]. The prefix carry tree get proceeded with the previous block signal to yield all carry bit signal and these stage contains three logic complex cells such as Black cell, Gray cell and Buffer cell. Black

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cell compute both the propogate (P(i,j)) and generate (G(i,j)) by using the equation[3] &[4].The Gray cell executes only the generate(G(i,j)).The carry bits generated in the second stage get passed to the post processing block thereby generating the sum using the equation[5].The block diagram is shown in the

Fig.1

$$Gm{:}n = A_n \text{ AND } B_n \quad (1)$$

$$G_0 = C_{in} \quad (2)$$

$$P_m{:}n = A_n \text{ XOR } B_n \quad (3)$$

$$P_0 = 0 \quad (4)$$

$$G_m{:}n = G_n{:}k \text{ OR } P_n{:}k \text{ AND } G_k\text{-}1{:}n \quad (5)$$

$$P_m{:}n = P_n{:}k \text{ AND } P_k\text{-}1{:}j \quad (6)$$

$$S_n = P_n \text{ XOR } C_{in} \quad (7)$$

The Brent Kung adder prefix structure is employed to achieve the higher speed with reduced power consumption. On comparing with the other parallel prefix adder structure the BK adder is chosen mainly for minimum fan out and should be higher speed in operation than others.Fig.2 shows the example BK adder prefix structure which uses the three basic cells in the prefix structure. These structure is elaborated for the proposed design having the modulo addition of (4n+1) for n=5.

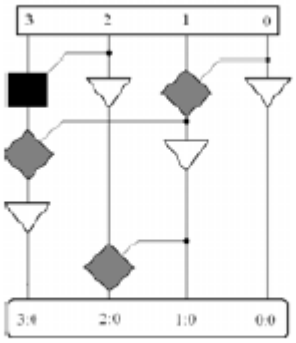

Fig.2. 4-bit BK adder prefixes structure.

B. HRPX Structure: (Hybrid Regular Parallel Prefix XOR/OR Adder Component)

Fig. 4 shows HRPX Structure. The regular parallel prefix adder is used to do the first part of addition and the simplified RCA logic is used to do the second part where the corresponding bits of the operand are fully variable. Full adder can be designed with XOR/OR gates because of the constant operand. In these reverse converter design the carry chain is not needed and can be ignored. For most modulo sets $(2^n\text{-}1)$ addition is an necessary operation. The End Around Carry(EAC) for $(2^n\text{-}1)$ addition is

represented with two zero, but for the reverse converter design one zero representation is required. To correct these zero representation problem, a detector circuit was employed in the design but it incorporates additional delay. So, the Binary to excess one converter(BEC) is used to solve the double zero representation issue.

C. HMPE Structure (Hybrid Modular Parallel Prefix Excess One Adder Component)

The HMPE Structure consists of two parts: Regular prefix adder and the Modified Excess One unit as shown in Fig.3. The first two operands are added using the parallel prefix adder and the result is conditionally incremented based on the control signal generated by the prefix structure to assure the single zero representation.

III. PROPOSED METHODOLOGY

A. Introduction

The RNS (Residue Number System) can provide carry free and fully parallel arithmetic operations for several applications, including digital signal processing and cryptography. In this brief, for the first time, we present a comprehensive methodology to wisely employ parallel-prefix adders in carefully selected positions in order to design fast reverse converters. The usage of the parallel-prefix adders to implement converters highly increases the speed at the expense of additional area and remarkable increase of power consumption. The reverse converter consists of a complex and non-modular structure. Therefore, more attention should be directed to its design to prevent slow operation and compromise the benefits of the RNS. Both the characteristics of the moduli set and conversion algorithm have significanteffects on the reverse converter performance. In addition to the moduli set, hardware components selection is key to the RNS performance.

Prefix: The outcome of the operation depends upon the initial inputs.

Parallel: involves the execution of an operation in parallel. This is done by segmentation into smaller pieces that are computed in parallel.

Operation: any arbitrary operator that is associative is parallelizable.

It is very fast because the processing is accomplished in a parallel fashion. In brief,

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the use of modular and regular parallel-prefix adders proposed in this brief in reverse converters highly decrease the delay at the expense of significantly more power and circuit area, whereas the proposed prefix-based adder components allows one to achieve suitable tradeoffs between speed and cost by choosing the right adders for the parts of the circuits that can benefit from them the most.

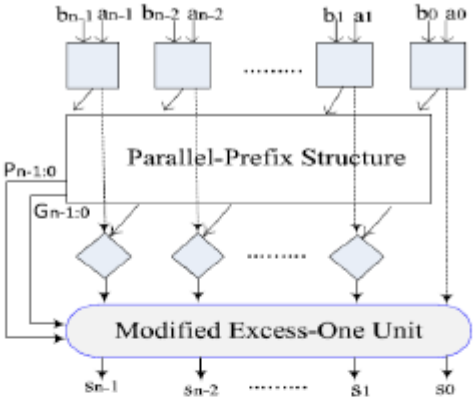

Fig.3. HMPE structure.

Assuming the addition of A= a_0, a_1.....a_n with B = b_0, b_1.....b_n the carry generate term gi, the carry propagate term $p_i = a_i + b_i$, which can also be defined as $p_i = h_i = a_i \copyright b_i$, where © denotes the exclusive-OR operation. The sum is given by S = A©B.

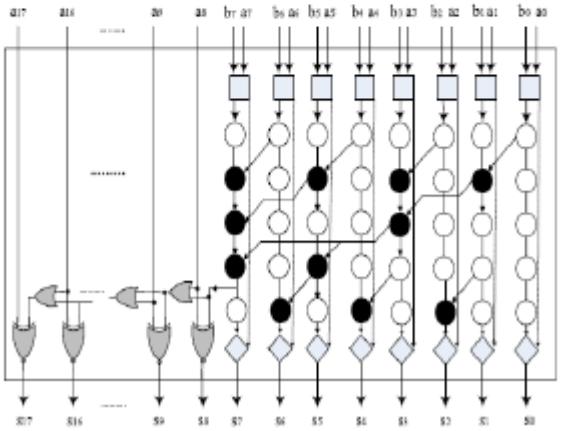

Fig.4. HRPX structure with BK prefix network.

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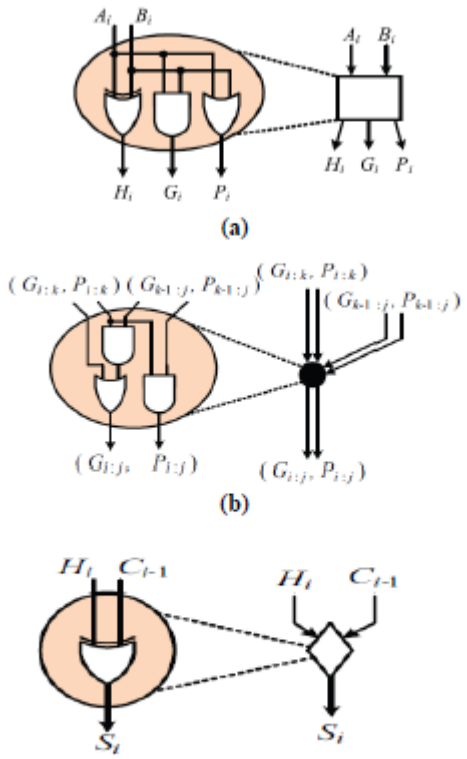

Fig.5. The logic-level implementation of the basic ce used in parallel-prefix adders.

The basic cells used for the parallel prefix operations in these projects are as shown in the above fig.5. If high speed is the designer goal, the CPAs with EAC and the regular CPAs should be replaced by traditional parallel prefix modulo 2n – 1 adder and regular parallel-prefix adders, respectively. However, for the VLSI designers, a suitable tradeoff between speed, power, and area is often more important. a regular parallel-prefix adder with the desirable prefix structure can be used to perform the first part of the addition, for which the corresponding bits of the operands are fully variable, and a RCA with simplified logic to do the second part (full adder becomes XNOR/OR gates because of the constant operand). The proposed hybrid regular parallel-prefix XOR/OR (HRPX) adder component to perform the (4n + 1)-bit addition. It should be noticed that due to the architecture of the reverse converter, the carry output of the XNOR/OR chain is not needed and can be ignored as shown in Fig.6.

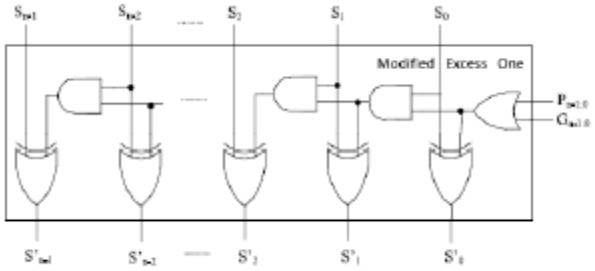

Fig.6. Modified excess-1 unit.

The regular CPA with end around carry is by default a moduli 2n − 1 adder with double representation of zero, but in reverse converters a single representation of zero is required. So, a one detector circuit has to be used to correct the result, which imposes an additional delay. However, there is a binary-to-excess-one converter, which can be

modified to fix the double-representation of zero issue.

B. Kogge Stone Prefix Adder

KSA is a parallel prefix form Ripple carry adder. It generates carry in O (logn) time and is widely considered as the fastest adder and is widely used in the industry for high performance arithmetic circuits as shown in Fig.7. In KSA, carries are computed fast by computing them in parallel at the cost of increased area. The complete functioning of KSA can be easily comprehended by analyzing it in terms of three distinct parts:

1. **Pre Processing:** This step involves computation of generate and propagate signals corresponding too each pair of bits in A and B. These signals are given by the logic equations below:

$$p_i = A_i \text{ xor } B_i \quad (8)$$

$$g_i = A_i \text{ and } B_i \quad (9)$$

2. **Ripple Carry Adder Network:** This block differentiates KSA from other adders and is the main force behind its high performance. This step involves computation of carries corresponding to each bit. It uses group propagate and generate as intermediate signals which are given by the logic equations below:

$$P_i{:}j = P_i{:}k+1 \text{ and } P_k{:}j \quad (9)$$

$$G_i{:}j = G_i{:}k+1 \text{ or } (P_i{:}k+1 \text{ and } G_k{:}j) \quad (10)$$

3. **Post Processing:** This is the final step and is common to all adders of this family (carry look ahead). It involves computation of sum bits. Sum bits are computed by the logic given below:

$$S_i = p_i \text{ xor } C_i\text{-}1 \quad (11)$$

4. **Implementation:** The schematic of KSA is implemented by using following building blocks:

Bit Propagate and Generate: This block implements the following logic:

$$G_i = A_i \textbf{ AND } B_i \quad (12)$$

$$P_i = A_i \textbf{ XOR } B_i \quad (13)$$

Group Propagate and Generate: This block implements the following logic:

$$G_2 = G_1 \textbf{ OR } (G_0 \textbf{ AND } P_1) \quad (14)$$

$$P_2 = P_1 \textbf{ AND } P_0 \quad (15)$$

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Group Propagate and Generate: This block implements the following logic:

$$\overline{G_2} = G_1 \textbf{ OR } (G_0 \textbf{ AND } P_1) \quad (16)$$

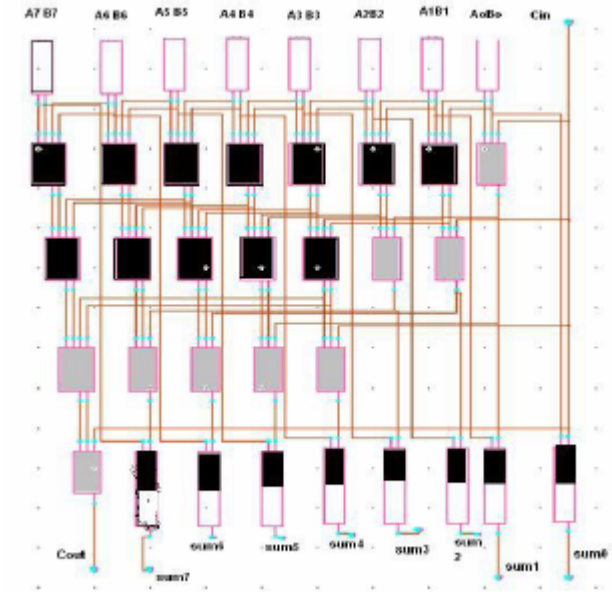

Fig.7. Complete schematic of 8-bit KSA.

IV. SIMULATION RESULTS

In this chapter all the simulation results which are done using Xilinx ISE 9.1 are shown in below results.

A. AREA Reports Hybrid regular parallel-prefix adder implementation in the reverse converter was as shown in the below fig.8.

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Device Utilization Summary				
Logic Utilization	Used	Available	Utilization	Note(s)
Number of 4 input LUTs	46	7,168	1%	
Logic Distribution				
Number of occupied Slices	24	3,584	1%	
Number of Slices containing only related logic	24	24	100%	
Number of Slices containing unrelated logic	0	24	0%	
Total Number of 4 input LUTs	46	7,168	1%	
Number of bonded IOBs	24	173	13%	
Total equivalent gate count for design	297			
Additional JTAG gate count for IOBs	1,152			

Fig.8. Hybrid regular parallel-prefix adder implementation.

Area report for kogge stone adder implementation in the reverse converter was as shown in the below fig.9.

Device Utilization Summary				
Logic Utilization	Used	Available	Utilization	Note(s)
Number of 4 input LUTs	31	7,168	1%	
Logic Distribution				
Number of occupied Slices	17	3,584	1%	
Number of Slices containing only related logic	17	17	100%	
Number of Slices containing unrelated logic	0	17	0%	
Total Number of 4 input LUTs	31	7,168	1%	
Number of bonded IOBs	32	173	18%	
Total equivalent gate count for design	201			
Additional JTAG gate count for IOBs	1,536			

Fig.9. Area report for kogge stone adder implementation.

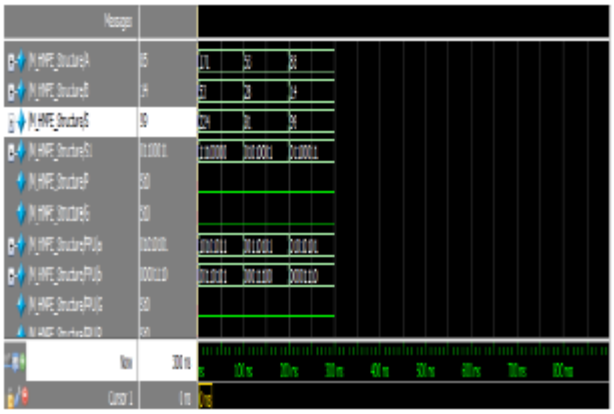

Fig.13. Simulation results of Final HMPE structure.

V. CONCLUSION This project presents a method that can be applied to most of the current reverse converter architectures to enhance their performance and adjust the cost/performance to the application specifications. The use of modular and regular parallel-prefix adders proposed in this brief in reverse converters highly decrease the delay at the expense of significantly more power and circuit area, whereas the proposed prefix-based adder components allows one to achieve suitable tradeoffs between speed and cost by choosing the right adders for the parts of the circuits that can benefit from them the most. Performance increased by using kogge stone adder implementation.

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