

Three Phase Hybrid Multilevel Inverter Using Switched Capacitor Units Fed with Industrial Drive Applications

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Abstract—Recently multilevel inverters (MLI) gained researchers interest due to efficient power conversion with multiple voltage steps resulting in improved power quality, reduced switching losses, higher electromagnetic compatibility and better voltage capability. This paper highlights a hybrid multilevel inverter for A.C electrical drives. In recent days multilevel inverters has become very popular for motor drive applications of industry. This hybrid topology has more advantageous of industrial applications. In this paper two new topologies have been proposed for multilevel inverters. The proposed topologies consist of a combination of the conventional series and the switched capacitor inverter units. The bad quality of voltage as well as current of a traditional Inverter fed Induction machine is on account of the availability of harmonics. This is exactly overwhelmed in multilevel inverter with significant measures which may produce premium quality voltage waveforms. The multilevel inverter output possesses diminished harmonics and also greater torque. Moreover it minimizes the heat produced in the stator winding of the induction motor. The proposed method introduces 17, 25 levels and three phase 25level Inverter fed Induction Motor drive. With the use of high level inverter, resolution is increase and also the harmonics is highly reduced. The simulation results are presented by using Matlab/simulink software.

Index Terms—Multilevel inverter, series-parallel connections, series inverters, switched capacitor, induction motor.

I. INTRODUCTION

Power electronic converters, especially dc/ac PWM inverters have been extending their range of use in industry because they provide reduced energy consumption, better system efficiency, and improved quality of product, good maintenance and so on. It should be noted that lower switching frequency usually means lower switching loss and higher efficiency [1-3]. Large electric drives and utility applications require advanced power electronics converter to meet the high power demands. As a result, multilevel power converter structure has been introduced as an alternative in high power and medium voltage situations [4]. A multilevel converter not only achieves high power ratings, but also improves the performance of the whole system in terms of harmonics, dv/dt stresses, and stresses in the bearings of a motor. Several multilevel converter topologies have been also developed i) diode clamped, ii) flying capacitors, and iii) cascaded or H-bridge. Referring to the literature reviews,

the cascaded multilevel inverter (CMI) with separated DC sources is clearly the most feasible topology for use as a power converter for medium & high power applications due to their modularization and extensibility [5]. The H-bridge inverter eliminates the excessively large number of (i) bulky transformers required by conventional multilevel inverters, (ii) clamping diodes required by multilevel diode-clamped inverters and (iii) flying capacitors required by multilevel flying-capacitor inverter. As a preliminary study the thesis examined and compared the most common multilevel topologies found in the published literature [6-8]. Starting from the essential requirements, the different approaches to the construction of multilevel inverter are explained and compared.

Over many years, Induction motor drives have been popularly used for variable speed control applications in industries [9]. This is because the induction motor is simple in construction and requires less maintenance. In recent times, multilevel inverters (MLI) are gaining popularity and widely used for induction motor drive applications [10]. It is especially used for medium to high voltage and high current drive applications. There are many advantages of multilevel inverters as compared to conventional inverters. Main advantages are low total harmonics distortion (THD), low switching losses, good power quality and reduced electromagnetic interference (EMI) [11-13].

II. PROPOSED SWITCHED CAPACITOR TOPOLOGY

Fig.1. shows the proposed switched capacitor unit. This topology is yield from series combination of several basic units. In this figure, the switches S_i ($i=1, 2, n$) connect the capacitors in series, and the switches P_i connect the capacitors in parallel with the dc voltage sources. To produce zero and negative voltage levels, an H-bridge has been used at the output. The blocked voltage by each switch in Fig.1. is V_{dc} .

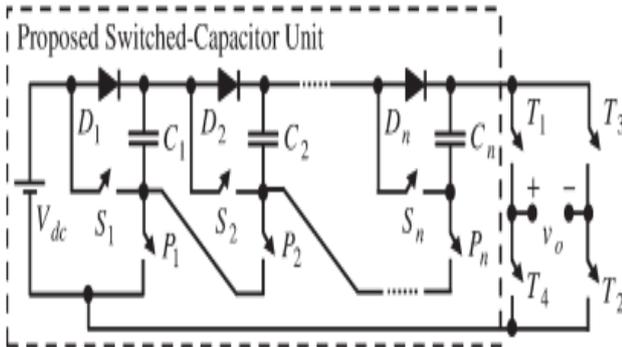


Fig.1. Proposed switched capacitor unit.

Thus, the proposed switched capacitor unit is also proper for a high frequency application that is not the aim of this paper. The other advantage of the proposed topology is the boosting ability of the input dc voltage without using any transformer. This feature reduces the size and cost of the system and increases its efficiency. The maximum numbers of output voltage levels (N-step), required insulated-gate bipolar transistors (IGBTs) (NIGBT), and diodes (N-diode) for the proposed topology shown in 3.3 are calculated by the following equations, respectively,

$$N_{step} = 2n + 3 \quad (1)$$

$$N_{IGBT} = 2n + 4 \quad (2)$$

$$N_{diode} = n \quad (3)$$

Where n is the number of capacitors. The maximum output voltage that can be produced (V_{omax}) is equal to

$$V_{o,max} = (n + 1)V_{dc} \quad (4)$$

In order to reduce the capacitor voltage drop during the series connection, the pulse width-modulation switching pattern can be used between the i th and $(i+1)$ th consecutive voltage levels ($i=0, 1, 2, n$), which, in turn, will increase the losses. On the other hand, more capacitors are needed to produce more levels at the output. Greater number of series capacitors increases their voltage drop. Thus, generating desirable voltage waveform without using of filtering elements will be difficult and requires more complex switching schemes. To produce greater number of voltage levels at the output and reduce the capacitor voltage drop, several units shown in Fig.1. can be used in series. In this condition, the first unit, the second unit, and the k th unit have $n_1, n_2,$ and n_k capacitors and dc

voltage sources with magnitudes of $V_1, V_2,$ and V_k , respectively.

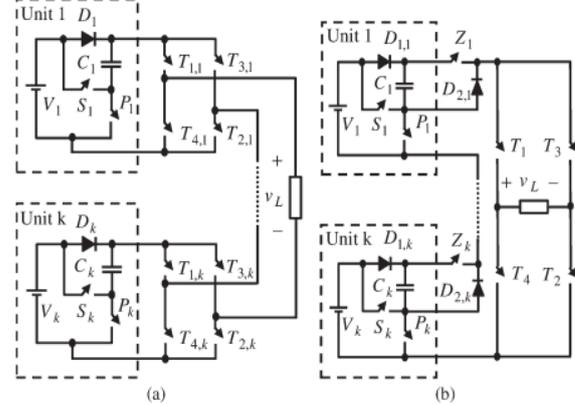


Fig.2. (a) First proposed topology. (b) Second proposed topology.

The general form of the equations that show the number of voltage levels and the number of IGBTs can be expressed as follows:

$$N_{step} = a \left[\prod_{j=1}^k (bn_j + c) \right] + d \quad (5)$$

$$N_{IGBT} = 2 \left(\sum_{j=1}^k n_j \right) + ek + f \quad (6)$$

Where a, b, c, d, e, and f are the integer numbers that depend on the unit connection order. In order to produce the maximum number of voltage levels at the output with using a specified number of IGBTs, (6) can be rewritten as follows:

$$N_{IGBT} = 2(n_1 + n_2 + \dots + n_k) + ek + f = cte \quad (7)$$

$$n_1 + n_2 + \dots + n_k = \frac{N_{IGBT} - ek - f}{2} = cte \quad (8)$$

Considering (5) and (8), the number of voltage levels in (5) will be maximum when the following condition is satisfied

$$n_1 = n_2 = \dots = n_k = n \quad (9)$$

From (8)–(10), N_{step} is obtained as follows

$$N_{step} = a(bn + c)^{\frac{N_{IGBT} - f}{2n + e}} + d \quad (10)$$

Equation (10) will be maximum when nets its minimum value. Thus, the proposed topologies produce the maximum number of voltage levels at the output form=1. This result is independent of the units' connection order. The proposed topologies have been presented in the next sections with considering $n=1$.

A. First Proposed Topology

Fig.2.(a) shows the first proposed topology. In this topology, the switched capacitor units have been connected in series by using H-bridges. Each unit can only produce positive voltage levels. The H-bridge produces zero and negative voltage levels. There are a lot of ways to determine the magnitude of the dc voltage sources. Some of these algorithms are not able to produce all voltage levels at the output, and some of them produce repetitive voltage levels. In order to prevent the mentioned problems and produce the maximum number of voltage levels, the magnitude of the dc voltage sources in the jth unit can be as follows:

$$V_j = (5^{j-1}) V_1 \quad (11)$$

Voltage and current ratings of the switches in a multilevel inverter play important roles in the total cost of the inverter. In all topologies, the currents of all switches are equal to the rated current of the load. This is, however, not the case for the voltage. Hence, there is a need for a criterion to evaluate the multilevel inverter from the viewpoint of blocked voltage by power switches and the total cost of system. This criterion is captioned as “standing voltage”. The standing voltage is equal to the sum of all blocked voltages by power switches in a converter. The standing voltage of the switches is equal to the sum of the blocked voltages by switches S and P and the H-bridge switches for all units.

B. Second Proposed Topology

Fig.2.(b) shows the second proposed topology. In this topology, each unit is bypassed when the switch Pj and the diode D2,j are on and the switch Zj is off. When the switch Zj is on, the diode D2, j becomes reverse biased. Thus, the diode D2,j prevents the backward current flowing during the unit bypassing when an inductive load is used at the output. In other words, the second proposed topology can produce the desirable voltage waveforms for resistive loads. On the other hand, by replacing the diode D2,j with a power electronic switch, the second proposed topology can be used for resistive-inductive loads. The magnitude of the dc voltage sources and the number of voltage levels can be calculated as follows:

$$V_j = (3^{j-1}) V_1 \quad (12)$$

The number of voltage levels (Nstep), the number of required IGBTs (NIGBT), the number of diodes (Ndiode), the maximum output voltage (Vo, max), the standing voltage of the switches (Vstand), the number of dc voltage sources (Ndc), and the variety of the dc voltage source magnitude (Nvariety) can be calculated for the first and second proposed topologies, as shown in Table I.

III. COMPARISON OF THE PROPOSED TOPOLOGIE SWITH OTHER CONVENTIONAL TOPOLOGIES

In this section, the first proposed topology has been compared with three main topologies of multilevel inverters, namely, the diode-clamped multilevel one, capacitor

TABLE I

Calculation of Different Parameters of the Proposed Topologies

Parameter	Proposed Topology			
	First		Second	
N_{step}	5^k	(13)	$(2 \times 3^k) - 1$	(20)
N_{IGBT}	$6k$	(14)	$3k + 4$	(21)
N_{diode}	k	(15)	$2k$	(22)
$V_{o,max}$	$2 \sum_{j=1}^k V_j$	(16)	$2 \sum_{j=1}^k V_j$	(23)
V_{stand}	$100 \left(\frac{1 + 5 + \dots + 5^{k-1}}{\dots} \right) V_1 = 5 \left(\frac{5^k - 1}{2} \right) V_1$	(17)	$11(1 + 3 + \dots + 3^{k-1}) V_1 = 11 \left(\frac{3^k - 1}{2} \right) V_1$	(24)
N_{dc}	k	(18)	k	(25)
$N_{variety}$	k	(19)	k	(26)

TABLE II

Comparison of The First Proposed Topology With The Topologies Presented In [9]

Topologies	N_{step}	N_{switch}	N_{diode}	$N_{capacitor}$	N_{dc}

First Topology	25	12	2	2	2
DCM	13	24	132	12	1
CCM	13	24	0	66	1
CMM	13	24	0	6	1
CBSCM	13	10	12	6	1
SCBM	13	11	3	2	1
HSSCM	13	21	4	5	3

Clamped multilevel one, and cascaded multi cell multilevel one. Also, the proposed topology has been compared with a cascade-boost switched capacitor converter multilevel inverter, a switched capacitor boost multilevel inverter, and a hybrid-source switched capacitor multilevel inverter [9]. Table II shows the numbers of switches, diodes, capacitors, and voltage levels for the proposed topology and the topologies presented in [9]. Table II proves the advantages of the proposed topology. In order to show the advantages of the proposed topologies in comparison with some recently presented topologies that use isolated dc voltage sources, the proposed topologies have been compared with the cascaded multilevel inverter using bidirectional switches (CMIBS), cascaded multilevel inverter using binary units (CMIBU), optimal topologies for cascaded sub multilevel inverters (OCSMI), cascaded multilevel inverter with reduced number of components for high-voltage applications (CMIHV), multilevel inverter with reduced number of power electronic components (MIRC) , and multilevel inverter using switched series/parallel dc voltage sources (MISSP) from different aspects. Fig.1. shows the number of required IGBTs for producing specified voltage levels at the output of the proposed topologies and the topologies presented. As can be seen, the proposed topologies need fewer IGBTs for realized N-step voltage levels at the output.

IV. INDUCTION MOTOR

In recent years the control of high performance induction motor drives for general industry applications and production automation has received widespread research interests. Induction machine modeling has continuously attracted the attention of researchers not only because such machines are made and used in largest numbers but also due to their varied modes of operation both under steady and dynamic states. Traditionally, DC motors were the work horses for the Adjustable Speed Drives (ASDs) due to their excellent speed and torque response. But, they have the inherent disadvantage of commutator and mechanical

brushes, which undergo wear and tear with the passage of time. In most cases, AC motors are preferred to DC motors, in particular, an induction motor due to its low cost, low maintenance, lower weight, higher efficiency, improved ruggedness and reliability. All these features make the use of induction motors a mandatory in many areas of industrial applications. The advancement in Power electronics and semiconductor technology has triggered the development of high power and high speed semiconductor devices in order to achieve a smooth, continuous and low total harmonics distortion (THD). Three phase induction motors are commonly used in many industries and they have three phase stator and rotor windings. The stator windings are supplied with balanced three phase ac voltages, which produce induced voltages in the rotor windings due to transformer action. It is possible to arrange the distribution of stator windings so that there is an effect of multiple poles, producing several cycles of magneto motive force (mmf) around the air gap. This field establishes a spatially distributed sinusoidal flux density in the air gap. In this paper three phase induction motor as a load. The equivalent circuit for one phase of the rotor is shown in figure. 3.

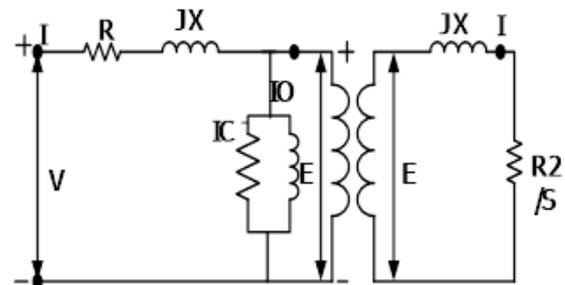


Fig. 3. Steady state Equivalent circuit of an induction Motor.

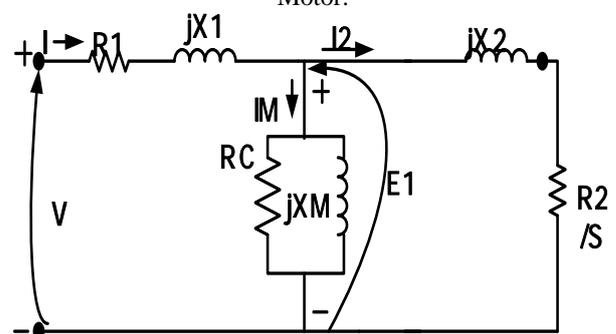


Fig.4. Equivalent circuit refer to stator.
The rotor current is

$$I_r = \frac{sE_r}{R_r + jX_r}$$

$$= \frac{E_r}{\frac{R_r}{s} + jX}$$

V.MATLAB/SIMULINK RESULTS

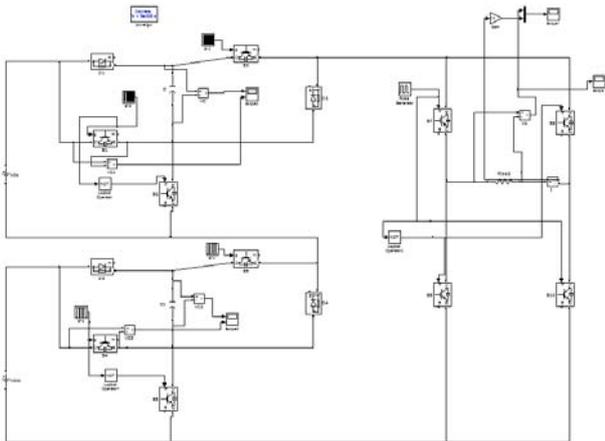


Fig.5. Matlab/Simulink model of 17-level inverter based proposed topology.

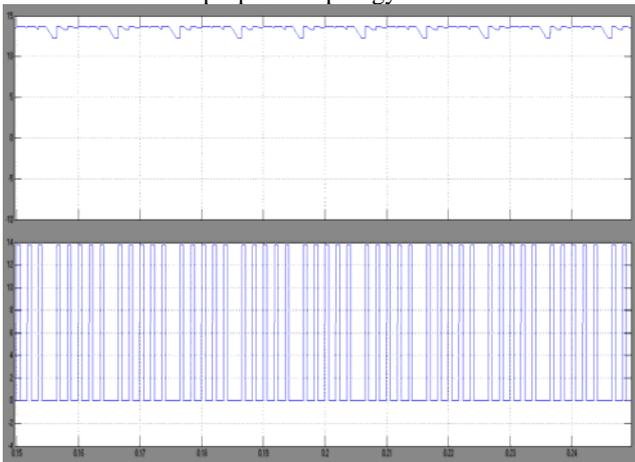


Fig.6. capacitor voltage (Vc1) and switch voltage (S1).

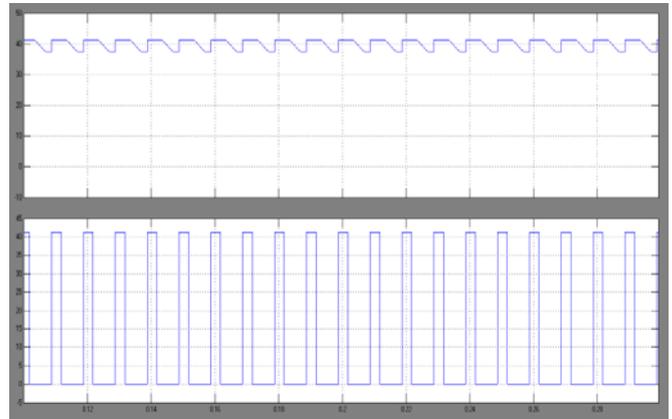


Fig. 7. capacitor voltage(Vc2) and switch voltage(S2).

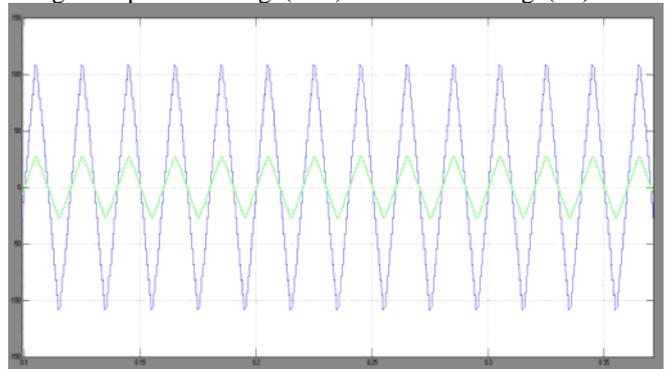


Fig. 8. Simulated load voltage and current waveforms for 17-level inverter.

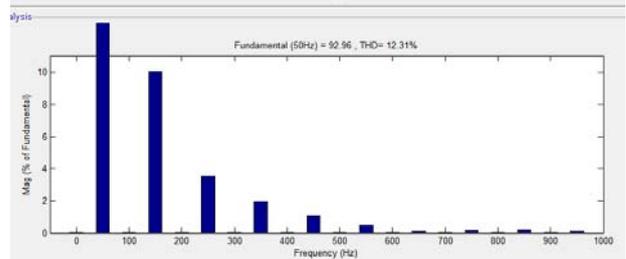
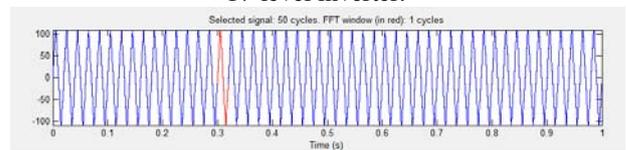


Fig.9.total harmonic distortions for 17 Level inverter.

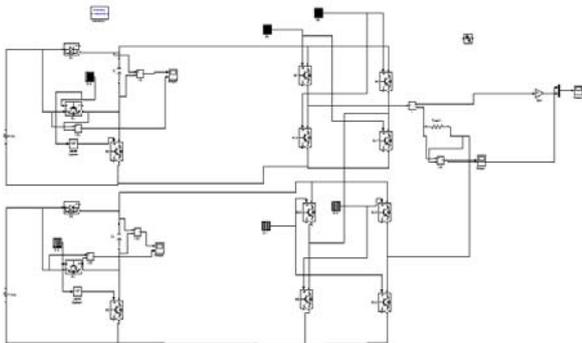


Fig.10. Matlab/Simulink model of 25-level inverter based proposed topology.

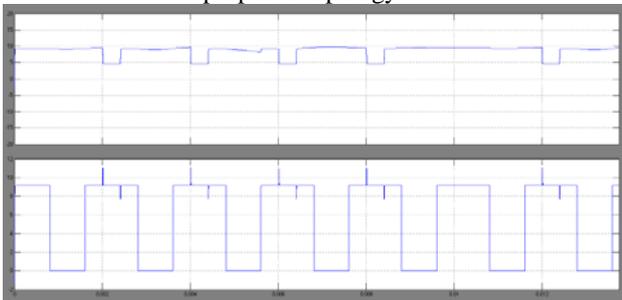


Fig.11. Capacitor voltage (Vc1) and switch voltage (S1).

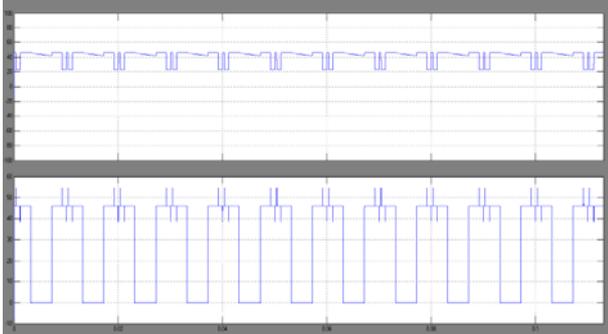


Fig.12. capacitor voltage (Vc2) and switch voltage (S2).

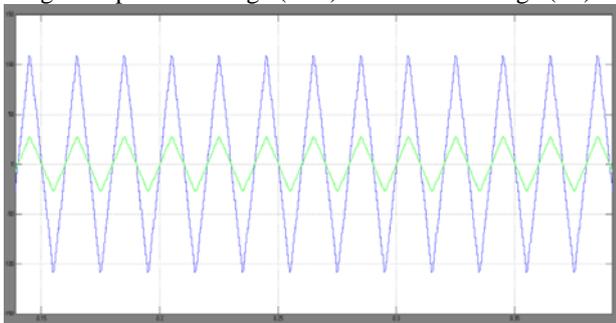


Fig.13. Simulated load voltage and current waveforms for 25-level inverter.

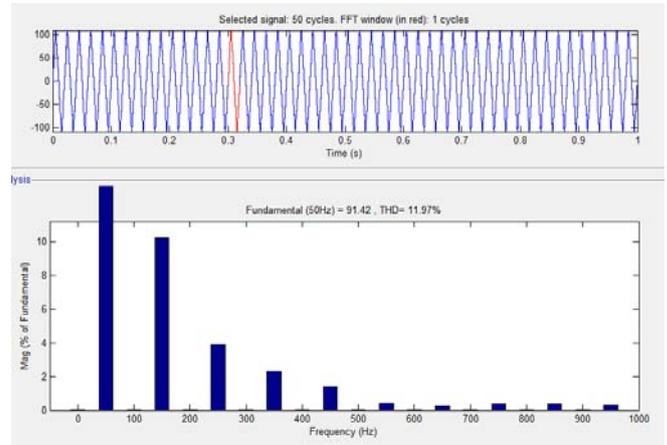


Fig.14. total harmonic distortions for 25 Level inverter.

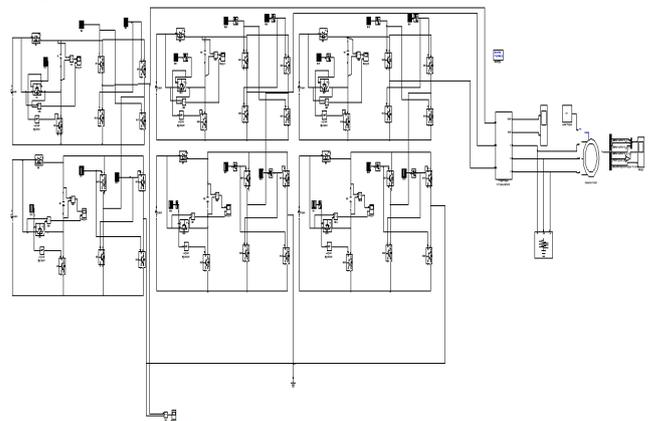


Fig.15. Matlab/Simulink Model of three phase 25-level inverter based proposed topology with Induction Motor.

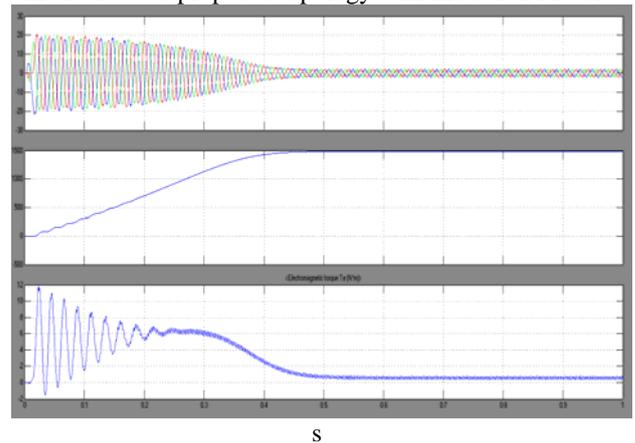


Fig.16. Stator Currents, Speed, Electromagnetic Torque. Fig.16. Stator Currents, Speed, Electromagnetic Torque of Proposed Three Phase 25 level inverter Applied to Induction machine Drive.

VI. CONCLUSION

In this paper, two new topologies have been proposed for multilevel inverters. The algorithms for the determination of the dc voltage source values have been presented, and the optimal number of switches and dc voltage sources to produce the maximum number of voltage levels at the output has been obtained. The loss calculations have been done. The number of on–off times in one cycle and the conduction intervals of switches have been calculated as a function of the output voltage levels. The proposed topologies reduce the number of switches and isolated dc voltage sources, the variety of the dc voltage source values, and size and cost of the system in comparison with conventional series topologies. The first proposed topology produces a 25-level voltage for all load power factors by using 12 IGBTs, 2 diodes, and 2 isolated dc voltage sources. It is also observed that the proposed topology decreased the number of required power electronic switches compared to a cascaded H-bridge inverter to obtain the same 17 and 25 level output voltage with lower THD. The induction motor performance curves such as speed, torque and current are presented. The simulation results show that the hybrid H-bridge fed Induction Motor drive has a satisfactory performance.

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