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Technology incorporate for Nano-Transistor

Ms. Sheetal Rana
sheetal.varsha@gmail.com
Department of Electrical Engineering, V.J. T.I Matunga,
Mumbai, Maharashtra, India

***Abstract* - In this paper, the major research efforts for nano-electronics by studying proposed technologies for replacing the transistor is consider. The limitation of conventional transistor has been demonstrated and new advance technology is proposed. The electronics industry is dependent on the ever-decreasing size of lithographic transistors; this scaling cannot be continuously undefined. Nano-electronics (circuits components are built with the scale of 10nm) seem to be the most promising Technology to lithographic based Transistor. Scaling of transistor gate lengths will be limited by off-state leakage current. Future transistor scaling will require the incorporation of new device structures, Carbon nano tube Field effect transistor (CNTFET) is one of the most promising device. In this paper technique to adjust the threshold voltage (Vt) of CNTFET and off state leakage current (I_{OFF}) has been discussed. The symmetric CNTFET has been adopted due to its inherent robustness to short-channel effects and improved current drive capability. Advantages of using alternative channel materials to facilitate scaling are mentioned.**

I. INTRODUCTION

In 1975 Gordon Moore, cofounder of Intel, predicted that the number of transistors that could be placed on a chip would double every two years. Chip manufacturers have relied on the continued scaling down of the transistor size to achieve the exponential growth in transistor counts, but the scaling will soon end. Three obstacles stand in the way: the rising costs of fabrication, the limits of lithography, and the size of the transistor. For example, parts of the latest transistors are only a few atoms thick, and shrink with the scaling of transistors. Thus, when these reach the limit of 1-2 atoms thick, the scaling will have to cease and a new technology will have to be adopted. One possible technology is lithography based integrated circuits is nanotechnology and the nano-scale electrical devices. The goal of scaling is to build an individual transistor that is smaller, faster, cheaper, and consumes less power. But unfortunately, the scaling down of lithographically patterned transistors cannot be continued further, but nano-electronics may be able to continue the scaling when transistors beat their limit.

The MOSFET has been the primary building block of integrated circuits for more than Forty years. It is the one of the most preferred transistor due to its unique property of scaling. Scaling allows reduction of device size by without affecting the performance. But there is limitations on scaling, beyond that the device does incorporate unexpected result. In mid- 1970 the gate length was 4µm and the gate oxide thickness was 50 nm. Since then, each new generation of technology has reduced gate length by about 30% and gate oxide thickness by about 25%. Smaller transistors allow more to be put on the same size chip, which has allowed integrations levels to rise from the hundreds of transistors. Shrinking the feature size also makes each transistor faster and consume less power.

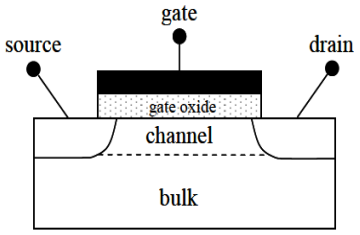

Figure 1: Illustration of a generic metal oxide semiconductor field-effect transistor (MOSFET).

The increase in speed comes from two factors: decreased capacitance and increased current. The capacitance of wires and gates lowers as these elements decrease in size, so the amount of charge a transistor has to place on a wire or gate decreases. The increase in current can be seen from the current flow equation for a transistor when the gate voltage is at its highest 4 value. A first order approximation of the current through the channel is given by the equation

$$I_D = \frac{\mu C_{ox} W}{2L}(V_{GS} - V_{th})^2$$

The important part of equation shows how different parameters of the MOSFET affect its performance. As the gate oxide thickness decreases, Cox increases, which leads to higher current. A smaller feature size also means that the length of the channel (L) also decreases, which reduces the channel resistance. However, as the transistor scales down, VGS (voltage gate to source) and Vth (threshold voltage that turns "on" transistor) are reduced. Up until recently, engineers have been reaping the benefits of the scaling down transistors without any significant disadvantages. That is beginning to change as the feature size is reduced to tens of nanometers.

The Important principle of MOSFET scaling is to decrease gate length and gate oxide thickness together. Scaling one without the other does not provide adequate performance improvement.

II. LIMITATION OF CONVENTIONAL TRANSISTOR

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The conventional MOSFET transistor does incorporate following limitation.

- Increasing power consumption, particularly through leakage currents
- less tolerance for process variation,
- Increasing cost

Leakage currents

An ideal transistor only has current flow when it is "on"; when the channel is "off" there is no current. This means that the transistor should consume no power if it is "off". Unfortunately, transistors are not ideal and, as they get smaller, they become less ideal.

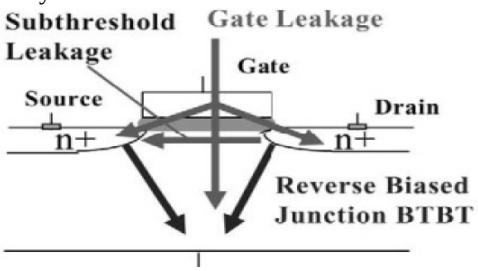

Figure 2: Limitation in MOSFET.

Leakage current, the flow of electrons through paths that should not conduct in an ideal transistor, now constitutes almost half of the power consumed by a chip. Leakage currents come from two primary sources. Gate oxide leakage occurs when electrons jump ("tunnel") from the gate to the channel through the gate oxide. Scaling reduces the thickness of the oxide, and the thinner the oxide, the higher the leakage due to tunneling becomes. Sub threshold leakage occurs when a current between the drain and source is present even though the gate voltage is below Vth and the channel should be "off". Sub threshold leakage becomes worse as Vth is lowered and as the channel length is decreased, both of which generally occur when a transistor is scaled down.

Total Chip Power

With the advent of portable computing devices, power consumption is becoming a primary focus of IC manufacturers. Power is the product of current and voltage. The voltage is set by the fabrication process, so power is essentially dependent on the current levels in a device. Currents are considered in two separate areas; dynamic and static currents (the leakage current discussed above is a portion of static current). Dynamic 5 current, and thus dynamic power, occurs when transistors are actively switching. Dynamic power per transistor is reduced with scaling, as less current is required to switch the transistor. However, the static currents, and thus static power, are increasing with scaling because of the leakage currents discussed above. Overall, power consumption is rising because of the increase in leakage currents, as well as the integration of more and more transistors. For example, the Intel Itanium 2 processor (90nm process) consumes about 177Watts at peak usage while the Intel Pentium (250nm process) consumes about 15Watts. Besides decreasing battery life of portable devices, power consumption creates heat, which degrades the chips' performance and must be dissipated. With increasing transistor density, localized heating can become a large problem. Heat increases the resistance of a transistor, thus decreasing its performance. This sets up the risk of thermal runaway, which can destroy a chip. Thermal runaway is a destructive cycle of increasing resistance causing increasing power consumption (heat generation), which in turn further increases the resistance.

Process Variation

Another drawback of scaling down the transistors is the decreased ability to handle fabrication process variations. As transistors and wires become smaller, fewer atoms make up the individual parts. For example, the gate oxide is currently only about five atoms thick. If merely a single atom is out of place, the gate oxide thickness varies by 20%. This lack of predictability significantly complicates the design process, and it will only become worse as scaling continues.

Costs

Probably the largest hurdle to further scaling of the MOSFET is simple economics. The cost of a fabrication facility is growing exponentially, along with the exponential growth of the number of transistors per chip. Currently (in 2005), a new fabrication facility costs around 3 billion US dollars to construct, and this is rising exponentially. The exponential increase in cost is a direct result of the increase in mechanical precision required to fabricate the integrated circuits. Since the cost of the fabrication plant is spread across the cost of each chip, this drives up either the cost-per-chip, or the number of chips that must be produced.

III. AVAILABLE TECHNOLOGY

Carbon Nano Tube

Currently, the most promising use of semiconducting CNTs is as a transistor component. As it is observe in Fig 3, carbon nano tube field effect transistors (CNTFET) appear very similar to MOSFETs, with the silicon channel replaced with a CNT. Most of the CNT transistors have been fabricated with SWCNTs because their band gap energy is in the range of a semiconductor. One group, however, found that MWCNTs could be used if the nanotubes were collapsed or crushed. This is probably impractical for large-scale systems, since each nanotube would have to be individually collapsed or selected amongst many "normal" nanotubes. Two varieties of CNT transistors have been fabricated. Figure 5a shows an illustration of a CNT transistor with a back gate, which uses the silicon substrate to control the conduction through the CNT. The use of a back gate is easier to fabricate,

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The single wall carbon nanotube (SW CNT) is a effective building block for future nanoelectronic Devices. These devices typically use a gate electrode to control the carrier density of a semiconducting SW CNT. The simplest configuration of a CNT FET is the bottom-gate FET, as shown in fig.3, in which, a SW CNT is dispersed or directly grown on a SiO2 /Si substrate, source drain contacts formed at the ends of the CNT and its transport properties controlled by applying a substrate voltage.

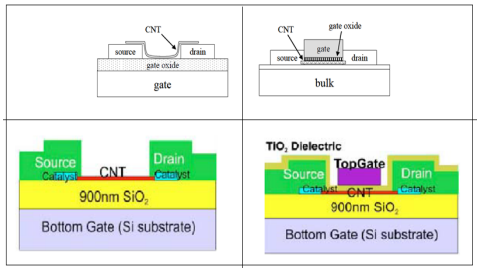

Figure 3: (a) Bottom gate CNTFET (b) Top gate CNTFET

Another variation is Top-gate CNT FETs in which the gate electrode and gate insulator are located on top of the SW CNT. To improve the device performance further a thinner gate insulator with a higher dielectric constant can be used. Recently, high k materials, such as, TiO2, ZrO2 and HfO2. The gate transfer characteristics of Bottom gated CNTFET is presented in Fig.4 At Vds=200 mV, the threshold voltage Vth is 0 V, on-current Ion=1*10^{-7} A, and off-current Ioff=1*10^{-12} A, giving this device an on/off ratio=10^{5}.

The subthreshold slope is 1000 mV/dec and transconductance 0.04 µ S|Vds=200 mV. As shown in fig.4 the subthreshold leakage current under condition (Vgs<Vt) is negligible. Variation in threshold voltage along with applied voltage one of most important property of Carbon nano tube. The gate transfer characteristics of Fig. 3 clearly shows a large Vthreshold hysteresis of 7 V depending on the direction the gate voltage A 5 nm TiO2 was deposited on top of the structure. The gate transfer characteristics of covered CNTFET were determined again as shown in Fig 5. At Vds=200 mV, the threshold voltage Vth is 0 V, on-current Ion=5*10^{-7} A, and off-current Ioff=4*10−11 A.

The on/off ratio is 10^{4} and the sub threshold slope improved to 320 mV/ deg. The Tran-conductance also increased to 0.38 µS|Vds=200 mV By simply covering the CNT but still maintaining the bottom-gate operation, we observed that the hysteresis in V Threshold was reduced to 2 V.

The top-gated CNT FET with a TiO2 high-k gate dielectric exhibits the highest transconductance (1.3 µS or 1000 µS/µm) a sub threshold swing 67–70 mV/dec. By simply covering the CNT but still maintaining the bottom-gate operation, we observed that the hysteresis in V Threshold was reduced by 5 V.

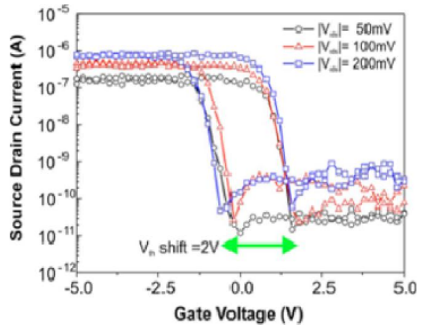

Figure.5 Gate transfer characteristics of Covered CNTFET

Fig.6 and 7 Shows the comparative study of Drain voltage vs drain current characteristics of CNTFET and MOSFET, having nano tube diameter 1nm and gate dielectric constant 3.9.

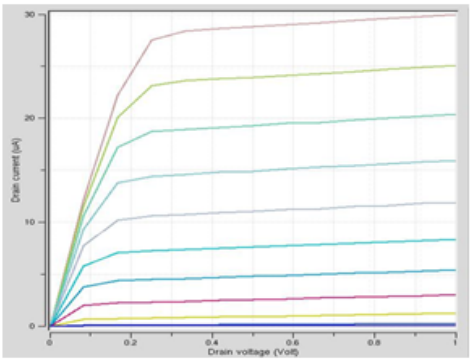

Figure 6: Id Vs Vd characteristics of CNTFET.

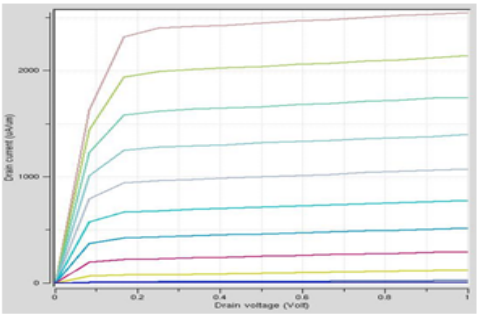

Figure 7: Id Vs Vd characteristics of MOSFET.

As compare to MOSFET; CNTFET has less current in saturation region. For the same drain voltage CNTFET has more control over drain current, while in MOSFET the drain current depend on the gate length. For the same gate voltage 0.2 voltage MOSFET drain current is around 1800 µA and CNTFET drain current is 18 µA. Improvement ratio in off state current(Ioff) is 100 times. CNTFET have better control over drain current having less off state leakage current and improved short channel effect. Also Less off state current further result in better sub threshold leakage.

IV. CONCLUSIONS

It has been observed the use of CNT allow us the further scaling. The use of low-k materials reduces sub threshold

leakage, permit to control the threshold voltage of transistor and low cost. Threshold voltage of a carbon nano tube field effect transistor can be adjusted by up to 2V approximate. These techniques enable device tuning for performance betterment and optimization.

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