International Journal of Research
Available at https://edupediapublications.org/journals
p-ISSN: 2348-6848
e-ISSN: 2348-795X
Volume 03 Issue 12
August 2016

Fuzzy Logic Controller based Hybrid Converter with Simultaneous DC and AC Outputs

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Abstract:

This Paper introduces new hybrid converter topologies which can supply simultaneously AC as well as DC from a single DC source. The new Hybrid Converter is derived from the single switch controlled Boost converter by replacing the controlled switch with voltage source inverter (VSI). This new hybrid converter has the advantages like reduced number of switches as compared with conventional design and provides DC as well as AC outputs with an increased reliability resulting from the inherent shoot through protection in the inverter stage. The hybrid grid reduces the process of multiple dc-ac-dc or ac-dc-ac conversions in an individual grid where the number of converter stations for converting ac to dc or dc to ac power is reduced. This hybrid can operate in both grid connected and autonomous mode. The proposed grid can operate in both standalone and grid connected mode. Fuzzy controller is used for smooth power transfer.

Index Terms—Boost-derived hybrid converter (BDHC), dc Nano grid, pulse width-modulated inverters.

I. INTRODUCTION

Nan grid architectures are greatly incorporated in the modern power system. In this system there is DC as well as AC loads supplied by different kinds of energy sources using efficient power electronic converters. Fig.1 shows the schematic of the system in which single DC source supplies both AC and DC loads. Fig. 1(a) shows the conventional architecture in which DC and AC load supplied by separate DC-DC converter and DC-AC converter from a single DC source respectively. Whereas in Fig. 1(b) referred as hybrid converter in which a single converter stage perform both operations. Such multi-output converters is very well suitable for systems with better power processing density and improved reliability for supplying simultaneous ac as well as dc outputs. This hybrid converter has the property of higher power processing capability and improved reliability resulting from the inherent shoot through protection. This paper investigates the use of single boost stage architecture to supply hybrid loads. The conventional VSI in Hybrid converter would involve the use of dead time circuitry to avoid the shoot through. Also misgating turn-on of switches may take place due to spurious noise resulting in damage of switches. For a compact system, spurious signal generation takes place commonly. So VSI in such application needs to be highly reliable with appropriate measures against shoot-through and EMI induced misgating [1-6].

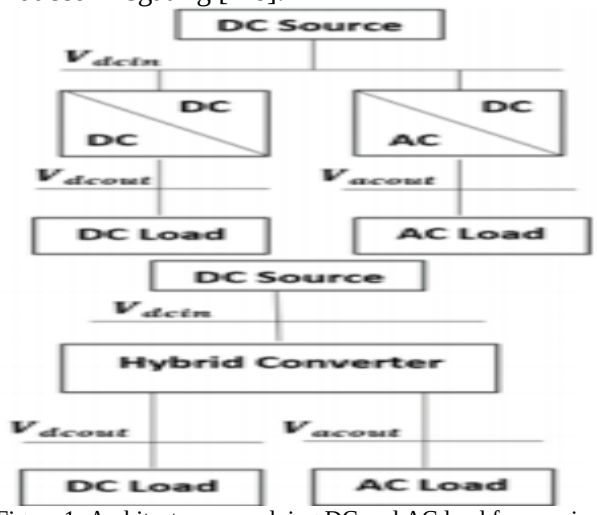

Figure 1: Architectures supplying DC and AC load from a single DC source. (a) Dedicated power converter based architecture and (b) Hybrid converter based architecture.

The simplest converters uses one input and one output which converts the level of input voltage, however for the complex task where more than one inputs with their different characteristics are needed

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to supply multiple loads of different requirements makes the designing of such converters very complex task which involve the designing of topologies with minimum number of switching components and their controlling strategies. There are a number of controlling techniques have been already proposed to control such Power converters, and the most common approach is either traditional proportional-integral (PI) controllers or linear negative feedback controllers. But these approaches have limited scope because they either required linear system (which is not always possible) or require the linearization procedure for nonlinear controlled system which is further complex task and produces only approximate model [7-12].

II. BDHC

A. Proposed Circuit Modification

Boost converters comprise complementary switch pairs, one of which is the control switch (controls the duty cycle) and the other capable of being implemented using a diode. Hybrid converter topologies can be synthesized by replacing the controlled switch with an inverter bridge network, either a single-phase or three-phase one. The proposed circuit modification principle, applied to a boost converter, is illustrated in the next section. The resulting converter, called BDHC, is the prime focus area of this paper.

B. Derivation of BDHC Topology

The control switch Sa of a conventional boost converter [shown in Fig. 2(a)] has been replaced by the bidirectional single-phase bridge network switches (Q1–Q4) to obtain the BDHC topology [shown in Fig. 2(b)]. This proposed converter provides simultaneous ac output (vacout) in addition to the dc output (vdcout) provided by the boost converter. For the BDHC, the hybrid (dc as well as ac) outputs have to be controlled using the same set of four controlled switchesQ1–Q4. Thus, the challenges involved in the operation of BDHC are the following: 1) defining the duty cycle (Dst) for boost operation and the modulation index (Ma) for inverter operation; 2) determination of voltage stresses and currents through different circuit components and their design; and3) control and channelization of total input power to both ac and dc loads. In the subsequent sections, all the aforementioned challenges will be discussed.

III. OPERATION OF BDHC

The schematic of the BDHC with the reference current directions has been shown in Fig. 2(b). In this paper, the continuous conduction mode of operation has been assumed (the boost inductor current (iL) never goes to zero). In this paper, lowercase letters represent instantaneous values, upper case letters represent dc or rms values, lower case letters with tilde (~) represent the ac component, and lower case letters with () represent the peak value of the variable.

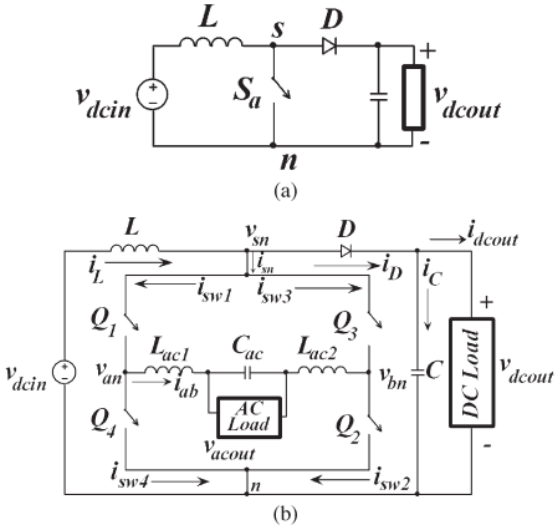

Fig. 2. (a) Conventional boost converter. (b) Proposed BDHC obtained by replacing Sa with a single-phase bridge network. The switch realization for the bridge can be done using bidirectional switches—either IGBTs with anti parallel diodes or MOSFETs.

A. Operating Principle

Each of the four bidirectional switches (Q1–Q4) of BDHC comprises the combination of a switch Si and an anti parallel diode Di (i = 1 to 4). The boost operation of the proposed converter can be realized by turning on both switches of any particular leg (either S1–S4 or S3–S2) simultaneously. This is equivalent to shoot-through switching condition as far as VSI operation is concerned, and it is strictly forbidden in the case of a conventional VSI. However, for the proposed modification, this operation is equivalent to the switching "on" of the switch "Sa" of the conventional boost converter [see Fig. 2(a)].The ac output of the BDHC is controlled using a modified version of unipolar sine-PWM switching scheme, described in Section IV. The BDHC, during inverter operation, has the same

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circuit states as a conventional VSI. when there is a power transfer with the source. In the other intervals, the current freewheels among the inverter switches and these states do not require the input to be at a fixed dc value and hence can be zero. In the BDHC, the switch node voltage (vsn) acts as the input to the inverter; it switches between the voltage levels—vdc out and zero. The switching scheme should ensure that the interval for power transfer with the source occurs only when vsn is positive, i.e., when vsn is clamped to the dc output voltage vdcout. Fig. 3illustrates this concept. The BDHC has three distinct switching intervals as described in the following.

1) Interval I—Shoot-through interval: The equivalent circuit schematic of the BDHC during the shoot-through interval is shown in Fig. 4(a). The shoot-through interval occurs when both the switches (either Q1–Q4 or Q3–Q2) of any particular leg are turned on at the same time. The duration of the shoot-through interval decides the boost converter duty cycle (Dst). The diode "D" is reverse biased during this period. The inverter output current circulates within the bridge network switches. Thus, BDHC allows additional switching states which are strictly forbidden in a VSI.

2) Interval II—Power interval: The power interval, shown in Fig. 4(b), occurs when the inverter current enters or leaves the bridge network at the switch node "s." The diode "D" conducts during this period, and the voltage at the switch node (vsn) is equal to the vdcout (neglecting the diode voltage drop). In this interval, either Q1–Q2 or Q3–Q4 is turned on.

3) Interval III—Zero interval: The zero interval occurs when the inverter current circulates among the bridge network switches and is not sourced or sunk. The diode "D" conducts during this interval. Fig. 4(c) shows the equivalent circuit for this interval. Table I shows the expressions for diode current (iD), capacitor current (iC), inverter output voltage (vab), and boost switch node voltage (vsn) for different operating modes. All these expressions have been defined in Fig. 2(b).

B. Steady-State Analysis

1) Gain Expression for DC and AC Outputs: Similar to conventional boost converters, the dc output of the BDHC can be regulated using the duty cycle, denoted by Dst, and is defined as the shoot-through time interval in a switching cycle, as shown in Fig. 4. For the purpose of analysis, we assume that the output dc capacitor voltage and the input inductor current have small ripple compared to their dc values. Hence, the expression for the voltage gain of the dc output is similar to that of a boost converter and can be derived as

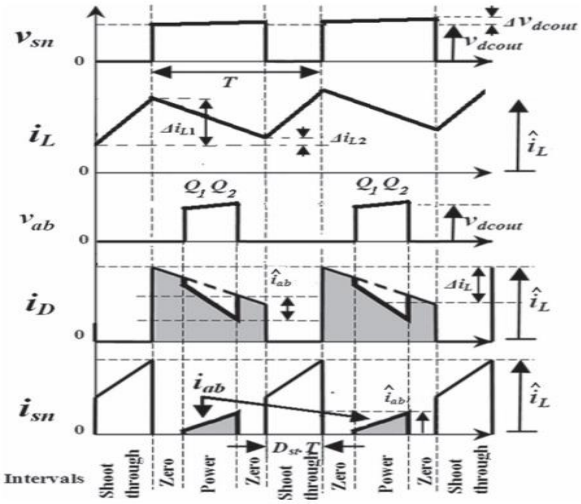

Fig. 3. Switch node voltage (vsn), inductor current (iL), inverter output voltage (vab), diode current (iD), and inverter input current (isn) for a positive inverter output current.

The reference directions for the voltages and currents have been shown in Fig. 2(b). The figure shows that the inductor current has a low-frequency component (at twice the power frequency) as described in

$$\frac{V_{\text{dcout}}}{V_{\text{dcin}}} = \frac{1}{1 - D_{st}} \qquad (1)$$

The modulation index, denoted by Ma ($0 \leq \text{Ma} \leq 1$), regulates the ac output voltage of the BDHC, and its definition is similar

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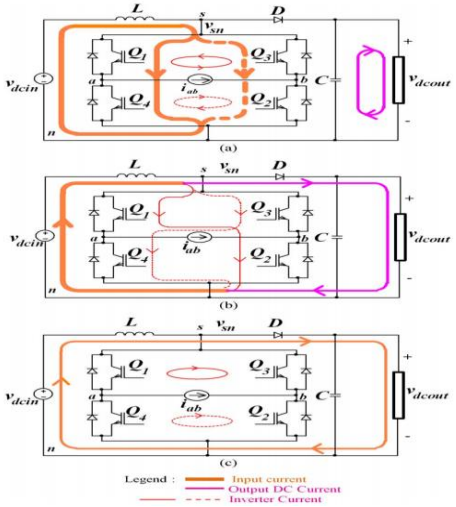

Fig. 4. Equivalent circuits and current directions of the BDHC during shoot-through interval, (b) power interval, and (c) zero intervals.

TABLE I
Steady-State Expressions of BDHC in Different Modes Of operation [Reference Directions Shown In Fig. 2(B)]

Interval	Shoot-through	Power	Zero
Diode Current	$i_D = 0$	$i_D = i_L - \lvert i_{ab}\rvert$	$i_D = i_L$
Capacitor Current	$i_C = -i_{dcout}$	$i_C = i_D - i_{dcout}$	$i_C = i_D - i_{dcout}$
Inverter output voltage	$v_{ab} = 0$	$v_{ab} = v_{dcout}$ if Q_1 and Q_2 are 'on' $v_{ab} = -v_{dcout}$ if Q_3 and Q_4 are 'on'	$v_{ab} = 0$
Switch node voltage	$v_{sn} = 0$	$v_{sn} = v_{dcout}$	$v_{sn} = v_{dcout}$

to that associated with conventional VSIs. The peak output ac voltage is related to the input as

$$\frac{\hat{v}_{\text{acout}}}{V_{\text{dcin}}} = \frac{M_a}{1 - D_{st}} \quad (2)$$

The maximum dc output gain achieved using the BDHC is similar to that of boost converters and is around four to five. The ac gain increases with the increase of modulation index (Ma) for any fixed value of duty cycle Dst. As the same set of switches controls both the dc and ac outputs, there is limitation to the maximum duty cycle or modulation index that can be achieved for this topology. The switching strategy must satisfy the following constraint:

$$\mathrm{M_a} + \mathrm{D_{st}} \leq 1 \quad (3)$$

Hence, the maximum value of ac gain is achieved at the equality condition of relation (3). At this condition, the peak value of the ac voltage is equal to the input voltage, and this is independent of the values of the duty cycle and modulation index. This can be obtained using (2) and (3). In order to achieve an ac voltage with voltage levels higher than the input voltage, either a step up transformer needs to be interfaced to the BDHC or a higher order boost converter needs to be used, as will be explained in Section VI.

2) DC and AC Output Power Expressions: From (1) and (2),the expressions for output dc (Pdc) as well as ac power (Pac)can be derived as follows:

$$P_{dc} = \frac{V_{\text{dcin}}^2}{R_{dc} * (1 - D_{st})^2} \quad (4)$$

$$P_{ac} = \frac{0.5 * V_{\text{dcin}}^2 * M_a^2}{R_{ac} * (1 - D_{st})^2} \quad (5)$$

Rdc and Rac are the dc and ac output resistances, respectively. Expressions (4) and (5) show that dc output power depends only on duty cycle (Dst), while ac output power depends upon both Dst and Ma.

3) Design of Passive Components: The ac output waveforms of the BDHC are similar to those of a conventional VSI. Therefore, the filter design principles associated with the design of conventional VSIs can be used for Lac (= Lac1 + Lac2) and Cac [see Fig. 2(b)]. As far as the dc–dc converter filters are concerned, the selection of inductor (L) and capacitor (C) values depends mainly on the amount of allowable ripple in the inductor current and capacitor voltage. One of the major differences between the BDHC and a conventional boost converter is that, in case of BDHC, since both dc and ac outputs are achieved, the inductor current (iL) and the capacitor voltage (vdcout) have both a high- and a low-frequency component (at twice the output ac power frequency), in addition to their dc values. The ripple content due to the low-frequency component

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e-ISSN: 2348-795X
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can be evaluated as follows. The instantaneous power input into the bridge network consists of a dc value (equal to Pac) and sinusoidal component varying at twice the power frequency. In conventional VSIs, a dc-link capacitor is often used at the input, and this maintains the instantaneous power balance. This results in ripple content at the dc-link voltage at twice the power frequency. For the proposed converter, this instantaneous power balance is maintained by both the reactive elements (capacitor C and inductor L). Neglecting switching frequency components, the equations related to the instantaneous power balance can be written as follows.

Let

$$v_{ab} = v_{an} - v_{bn} = \hat{v}_{ab}\sin(\omega t),$$
$$i_{ab} = \hat{i}_{ab}\sin(\omega t - \varphi)$$

where ϕ is the phase difference between the fundamental components of inverter output voltage (vab) and current (iab).Therefore, the instantaneous inverter input power

$$p_{ab} = v_{ab}i_{ab} = 0.5\,\hat{v}_{ab}\hat{i}_{ab}\cos\varphi - 0.5\,\hat{v}_{ab}\hat{i}_{ab}\cos(2\omega t - \varphi) \quad (6)$$

The above expression has a dc as well as a sinusoidal component. The dc component is equal to the real power demanded by the ac output (Pac). Thus, the average input current of the inductor (L) can be calculated as shown in

$$I_L = \frac{P_{dc} + P_{ac}}{V_{\text{dcin}}} = \frac{V_{\text{dcout}}I_{\text{dcout}} + 0.5\,\hat{v}_{ab}\hat{i}_{ab}\cos\varphi}{V_{\text{dcin}}} \quad (7)$$

The sinusoidal component of instantaneous power pab is balanced by the variation of the inductor current and the capacitor voltage. This results in a low-frequency ripple (at twice the power frequency) in the inductor current as well as the capacitor voltage. This power balance equation is shown in

$$\tilde{p}_{ab} = \frac{d\left(\frac{1}{2}Li_L^2(t) + \frac{1}{2}Cv_{\text{dcout}}^2(t)\right)}{dt} = 0.5\,\hat{v}_{ab}\hat{i}_{ab}\cos(2\omega t - \varphi) \quad (8)$$

Where p ˜ab is the double frequency power component of input power to the inverter bridge. The solution of (8) relates the maximum (iL,max, vdcout,max) and minimum (iL,min, vdcout,min) values of iL(t) and vdcout(t), as shown in

$$\frac{1}{2}L\left(i_{L,\max}^2 - i_{L,\min}^2\right) + \frac{1}{2}C\left(v_{\text{dcout,max}}^2 - v_{\text{dcout,min}}^2\right) = \frac{\tilde{p}_{ab}}{\omega}. \quad (9)$$

Equation (9) can be simplified to obtain the following design criterion:

$$L.I_L.\Delta i_{L,pk-pk} + C.V_{\text{dcout}}.\Delta v_{\text{dcout,pk-pk}} = \frac{\widetilde{P_{ab}}}{\omega} \quad (10)$$

Where Δi L,pk−pk and Δvdcout, pk−pk represent the peak-to peak ripple contents in iL(t) and vdcout(t),respectively. Thus, from (10), it can be concluded that, with the increase in ac output power, the ripple content (at twice the fundamental frequency) in both the inductor current iL and dc output capacitor voltage vdcout changes. Depending upon the active power level, the magnitude of this power frequency component can be greater than the ripple due to high frequency. The high-frequency ripple content has been illustrated in Fig. 3, where the inductor current does not reach its initial value after each switching interval due to the presence of the sinusoidal component in capacitor voltage. This, in turn, results in a sinusoidal ripple in the inductor current at twice the fundamental frequency. This low-frequency ripple content should hence be considered during the component design. For the BDHC, the inductor current is drawn from a dc source, and hence, the ripple content in the input current should be as low as possible. If the ripple in inductor current is fixed, the ripple in dc output can be calculated from (10)

4) Switch Stress and Current Expressions: The switchesQ1–Q4 and Q3–Q2 are complementary in operation except during the shoot-through interval. The input to the inverter bridge equals to vdcout(shown in Fig. 3) during both power and zero intervals. Thus, the maximum stress on each switch is equal to vdcout, the dc output voltage, neglecting the voltage drop across the conducting diode D. The stress across the diode D is equal to vdcout during the shoot-through interval. Thus, the selection of switch ratings is dependent upon the dc output voltage rather than the input voltage, contrary to the case for a conventional VSI.As opposed to a conventional boost converter, the diode current (iD) of BDHC is dependent upon the boost inductor current as well as the current drawn by the VSI bridge legs. This is due to the fact that, apart from the shoot-through interval, which is similar to the

International Journal of Research
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p-ISSN: 2348-6848
e-ISSN: 2348-795X
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boost interval of a boost converter, there is an additional power interval. The current is n [shown in Fig. 2(b)] is equal to iL during the shoot-through interval. During the power interval, is n equals the inverter output current iab. Since iab is time varying, the value of is n and, hence, diode current iD vary with time. This is shown in Fig. 3.The expressions for the currents in different intervals are shown in Table I and in The maximum current through the switchesˆ is w can be expressed as follows:

$$\hat{i}_{sw(i)} = i_{L,max} + |\hat{i}_{ab}|, \quad (\mathrm{i} = 1 \text{ to } 4) \qquad (11)$$

|ˆ iab| represents the maximum value of the inverter output current iab(t). Fig. 3 shows the nature of the switch node voltage(vsn), inductor current (iL), diode current (iD), and inverter bridge input current (isn) for a positive value of ac output current (iab).

IV. CONTROL STRATEGY

A. Modified Unipolar PWM Strategy for BDHC

The fundamental principle behind the operation of BDHC is based upon the fact that the inverter bridge input must be connected to a positive voltage during the power interval only. This means that the inverter output has to be modulated when vsn = 0 and boost operation occurs when vab = 0. The inverter output voltage assumes three different values, and hence, the PWM modulation strategy used is based upon unipolar sine PWM scheme, which provides three voltage levels for output. The PWM control scheme for the BDHC is based upon the switching scheme proposed in [7]. In this scheme, shown in Fig. 5(a), the shoot-through is realized by gating-on both the switches of a single leg at the same time. The switching strategy involves turning on only one leg at a time in order to achieve shoot-through. Another alternative is to turn on all the switches during shoot-through. This scheme has been proposed in [8] and [9], and the concept is illustrated using Fig. 5(b). As shown in the figure, turning on all the switches for shoot-through involves more switching during each switching period with their associated losses. The reliability of the circuit also reduces since the time between two successive switching [switches S1 and S2 in Fig. 5(b)] is dependent on tz, which can be close to zero. This may be impractical considering minimum switching times for the devices used. Thus, compared to Fig. 5(b), additional switching at S1 and S2 is absent in the proposed scheme of Fig. 5(a), and this scheme has been used for the control of the BDHC.

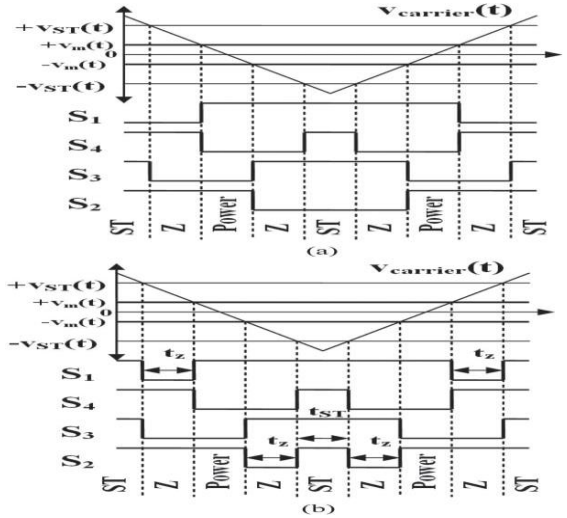

Fig. 5. Generation of gate signals for a positive value of reference signal (vm(t)). (a) Proposed PWM scheme used and (b) its variant where all switches are turned on during shoot-through. Here, ST is the shoot-through interval, and Z is the zero interval.

V. HIGHER ORDER BOOST-BASED HYBRID TOPOLOGIES

The maximum output-to-input gain achieved by the boost converter is limited to approximately four due to resistive losses[10]. Higher order boost converters with a single controllable switch have been described in [11], which achieve higher gains compared to a boost converter. Fig. 9 shows the schematic of the quadratic BDHC (QBDHC), which has been derived from the single-switch controlled quadratic boost converter. Thus, in general, the family of nth-order boost converters with single switch can be modified to form the corresponding family of hybrid boost Converters

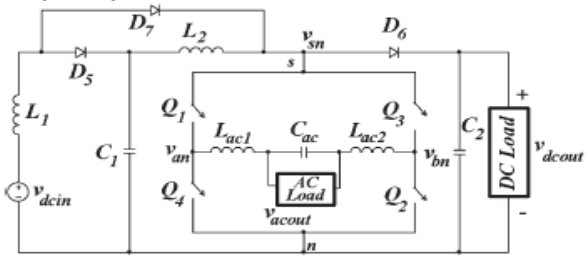

Fig.6. Higher gain can be achieved by using QBDHC.

VI. FUZZY LOGIC CONTROL

L. A. Zadeh presented the first paper on fuzzy set theory in 1965. Since then, a new language was

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developed to describe the fuzzy properties of reality, which are very difficult and sometime even impossible to be described using conventional methods. Fuzzy set theory has been widely used in the control area with some application to power system [5]. A simple fuzzy logic control is built up by a group of rules based on the human knowledge of system behavior. Matlab/Simulink simulation model is built to study the dynamic behavior of converter. Furthermore, design of fuzzy logic controller can provide desirable both small signal and large signal dynamic performance at same time, which is not possible with linear control technique. Thus, fuzzy logic controller has been potential ability to improve the robustness of compensator.

The basic scheme of a fuzzy logic controller is shown in Fig 7 and consists of four principal components such as: a fuzzy fication interface, which converts input data into suitable linguistic values; a knowledge base, which consists of a data base with the necessary linguistic definitions and the control rule set; a decision-making logic which, simulating a human decision process, infer the fuzzy control action from the knowledge of the control rules and linguistic variable definitions; a de-fuzzification interface which yields non fuzzy control action from an inferred fuzzy control action [10].

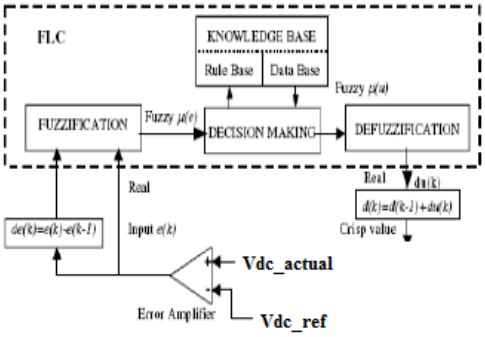

Fig.7. Block diagram of the Fuzzy Logic Controller (FLC) for proposed converter

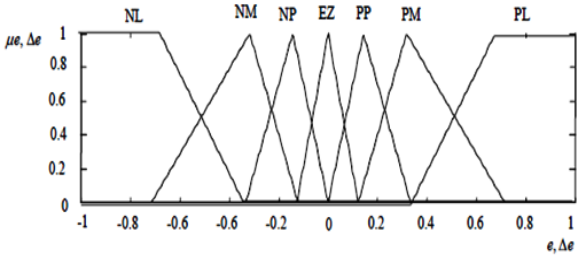

Fig.8. Membership functions for Input, Change in input, Output.

Rule Base: the elements of this rule base table are determined based on the theory that in the transient state, large errors need coarse control, which requires coarse in-put/output variables; in the steady state, small errors need fine control, which requires fine input/output variables. Based on this the elements of the rule table are obtained as shown in Table 1, with '*Vdc*' and '*Vdc-ref*' as inputs.

e / Δe	NL	NM	NS	EZ	PS	PM	PL
NL	NL	NL	NL	NL	NM	NS	EZ
NM	NL	NL	NL	NM	NS	EZ	PS
NS	NL	NL	NM	NS	EZ	PS	PM
EZ	NL	NM	NS	EZ	PS	PM	PL
PS	NM	NS	EZ	PS	PM	PL	PL
PM	NS	EZ	PS	PM	PL	PL	PL
PL	NL	NM	NS	EZ	PS	PM	PL

VII.MATLAB/SIMULATION RESULTS

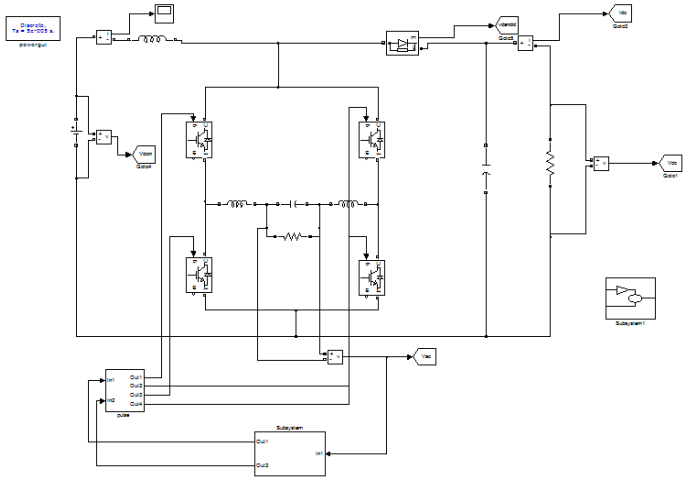

Fig.9.Matlab/Simulation model of Proposed BDHC obtained by replacing Sa with a single-phase bridge network.

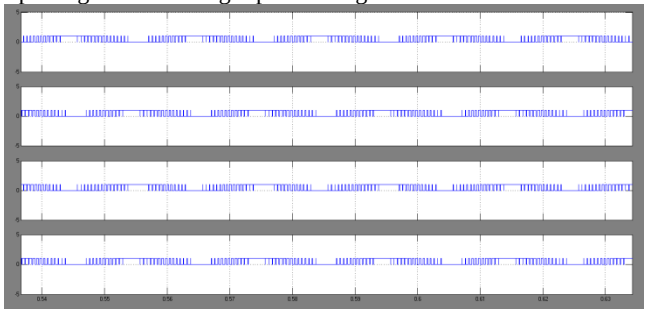

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Fig.10. Simulation results of the proposed PWM control.

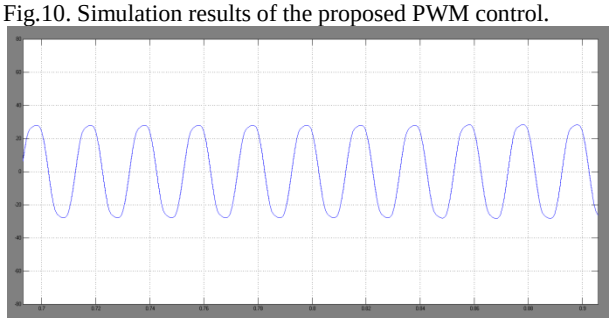

Fig.11. Steady-state input Voltage and ripple variation of the BDHC state Variables For input ac voltage Vac.

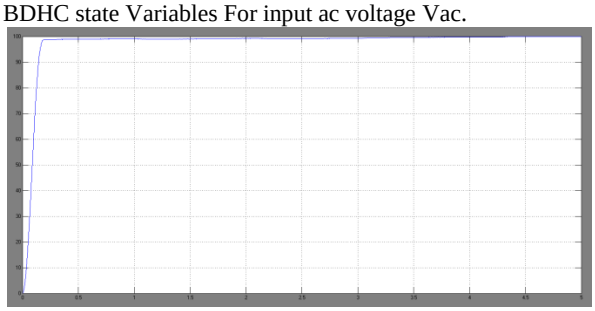

Fig.12. Steady-state input current and ripple variation of the BDHC state
Variables For output dc voltage Vdc.

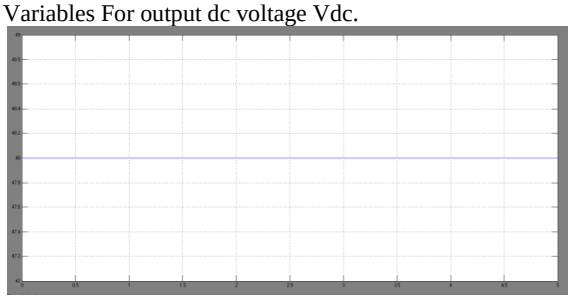

Fig.13. Steady-state input current and ripple variation of the BDHC state
Variables For input dc voltage Vdc.

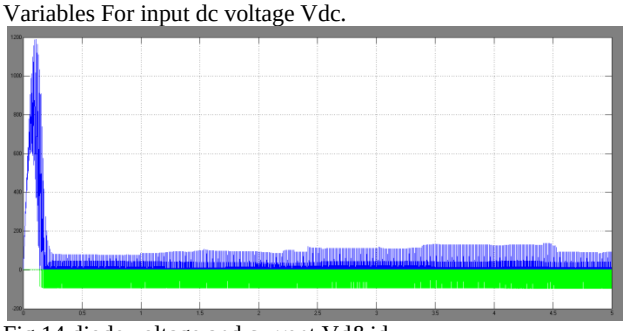

Fig.14.diode voltage and current Vd&id.

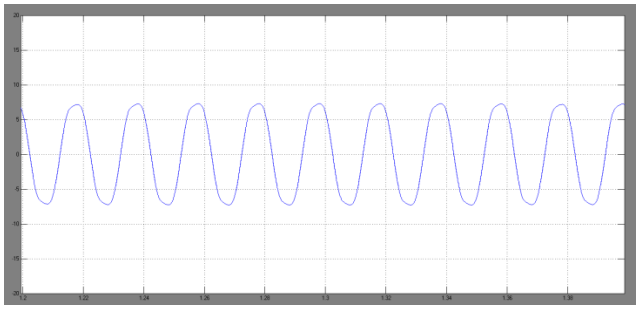

Fig.15.load current Il.

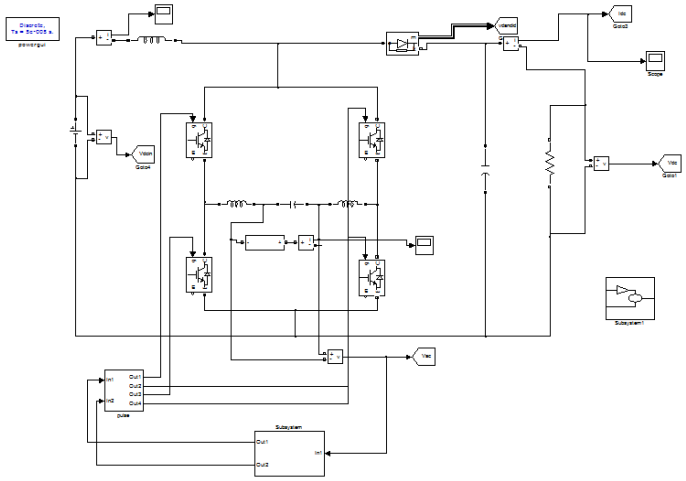

Fig.16.Matlab/Simulation model of Cross-regulation behavior of the BDHC when subjected to step change in loads (dc as well as ac).

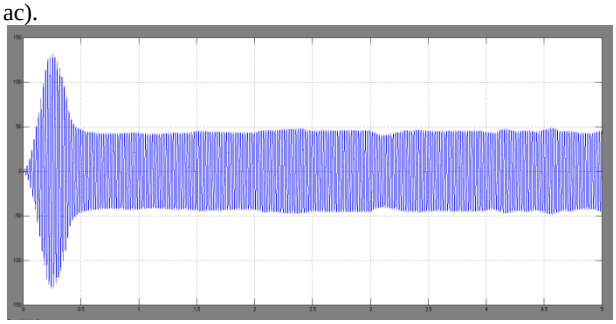

Fig.17.input voltage under step changes Vac.

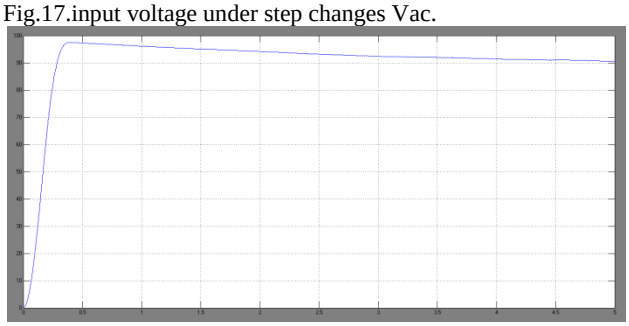

Fig.18.output dc voltage Vdcout.

International Journal of Research
Available at https://edupediapublications.org/journals
p-ISSN: 2348-6848
e-ISSN: 2348-795X
Volume 03 Issue 12
August 2016

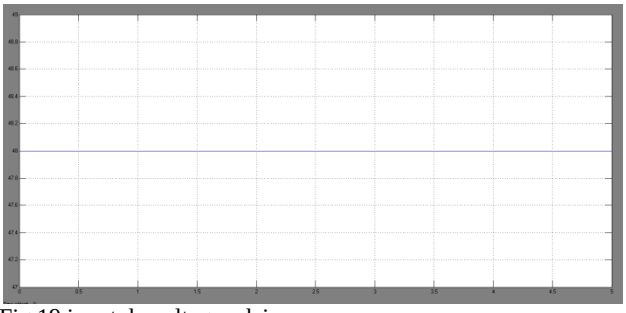

Fig.19.input dc voltage vdcin.

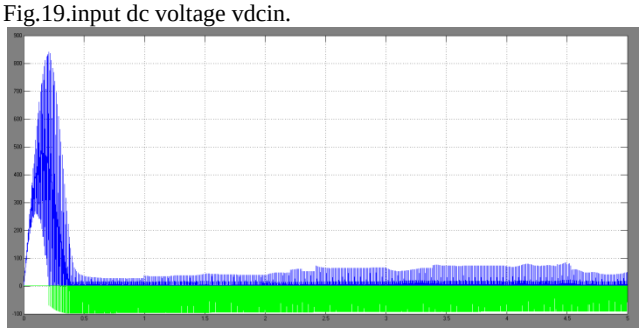

Fig.20.diode voltage and current Vd&id.

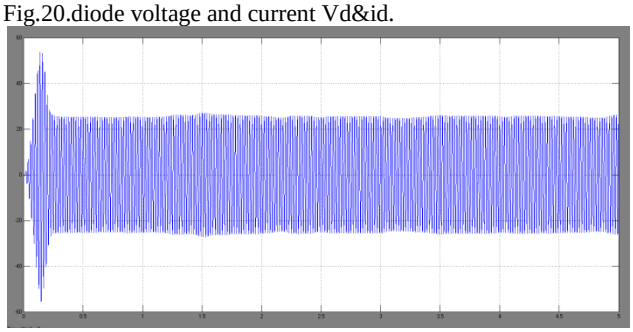

Fig.21. Steady-state input Voltage and ripple variation of the BDHC state Variables For input ac voltage Vac with fuzzy logic controller.

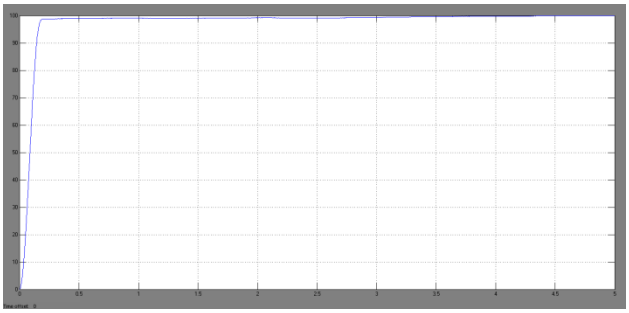

Fig.22. Steady-state input current and ripple variation of the BDHC state
Variables For output dc voltage Vdc fuzzy logic controller.

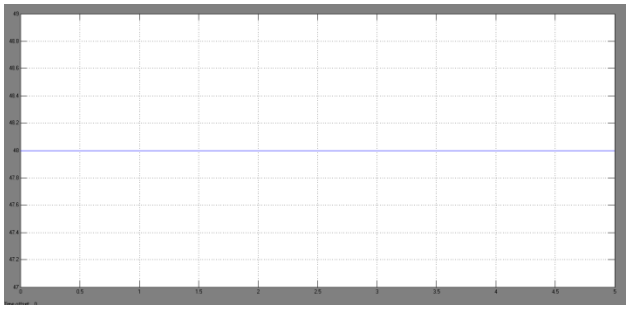

Fig.23. Steady-state input current and ripple variation of the BDHC state
Variables For input dc voltage Vdc.

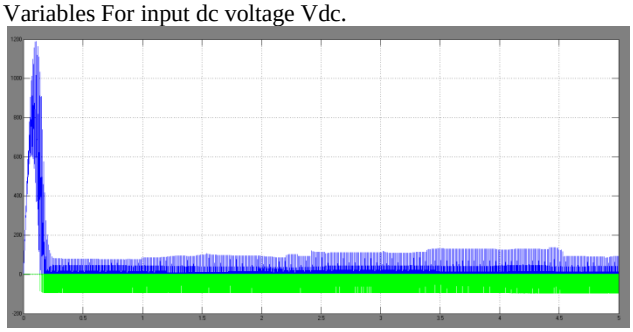

Fig.24.diode voltage and current Vd&id.

VIII. CONCLUSION

This paper has proposed hybrid power converter topologies which can supply simultaneous dc and ac loads from a single dc input. The various advantages of using this single converter stage like shoot-through protection have been described and compared to traditional VSIs. It has been shown that a class of converters can be achieved by describing the BDHC and QBDHC. Using a single converter for all the modes (charging, supplying and battery less operations) reduces the total volume and cost of the converter. The proposed algorithm are lies on fuzzy logic controller to estimate the switching activities of the transistors, which eliminates the need for complex system dependent PI controllers and can further reduce the system cost.

REFERENCES

[1] D. Boroyevich, I. Cvetkovic, D. Dong, R. Burgos, F. Wang, and F. Lee, "Future electronic power distribution systems—A contemplative view," in Proc. 12th Int. Conf. OPTIM Elect. Electron. Equip., Brasov, Romania, May 20–22, 2010, pp. 1369–1380.

[2] F. Blaabjerg, Z. Chen, and S. B. Kjaer, "Power electronics as efficient interface in dispersed power generation systems," IEEE Trans. PowerElectron., vol. 19, no. 5, pp. 1184–1194, Sep. 2004.

[3] O. Ray, S. Mishra, A. Joshi, V. Pradeep, and A. Tiwari, "Implementation and control of a bidirectional high-gain transformer-less standalone inverter," in Proc. IEEE Energy Convers. Congr. Expo., Raleigh, NC, USA, Sep. 2012, pp. 3233–3240.

[4] F. Z. Peng, "Z-source inverter," IEEE Trans. Ind. Appl., vol. 39, no. 2, pp. 504–510, Mar./Apr. 2003.
[5] C. J. Gajanayake, F. L. Luo, H. B. Gooi, P. L. So, and L. K. Siow, "Extended-boost Z-source inverters," IEEE Trans. Power Electron., vol. 25, no. 10, pp. 2642–2652, Oct. 2010.
[6] S. Upadhyay, R. Adda, S. Mishra, and A. Joshi, "Derivation and characterization of switched-boost inverter," in Proc. 14th Eur. Conf. Power Electron. Appl.—EPE, Birmingham, U.K., Aug. 2011, pp. 1–10.
[7] S. Mishra, R. Adda, and A. Joshi, "Inverse Watkins-Johnson topology based inverter," IEEE Trans. Power Electron., vol. 27, no. 3, pp. 1066– 1070, Mar. 2012.
[8] S. Mishra, R. Adda, and A. Joshi, "Switched-boost inverter based on inverse Watkins-Johnson topology," in Proc. IEEE ECCE, Phoenix, AZ, USA, Sep. 2011, pp. 4208–4211.
[9] R. Tymerski and V. Vorperian, "Generation, classification and analysis of switched-mode dc-to-dc converters by the use of switched-inductor-cells," in Proc. Int. Telecommun. Energy Conf., Oct. 1986, pp. 181–195.
[10] R. Adda, S. Mishra, and A. Joshi, "A PWM control strategy for switched boost inverter," in Proc. IEEE ECCE, Phoenix, AZ, USA, Sep. 2011, pp. 991–996.
[11] F. Z. Peng, M. Shen, and Z. Qian, "Maximum boost control of the Z-source inverter," IEEE Trans. Power Electron., vol. 20, no. 4, pp. 833– 838, Jul. 2005.
[12] M. Shen, J. Wang, A. Joseph, F. Z. Peng, L. M. Tolbert, and D. J. Adams, "Constant boost control of the Z-source inverter to minimize current ripple and voltage stress," IEEE Trans. Ind. Appl., vol. 42, no. 3, pp. 770–778, May/Jun. 2006.