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Energy and discipline effective Implementation for Parallel FIR Filters utilizing FFAs and DA

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***Abstract* – This paper describes the implementation of two parallel FIR filter based on traditional method costs considerable hardware power and area. The Finite Impulse Response (FIR) filters mainly contain delay elements, adders and multipliers. The usage of multipliers in the filter structure leads to increase in area and delay which may results ultimately in low speed and performance. A new design and implementation of two parallel FIR filter structure using Look Up Table (LUT) less Distributed Arithmetic (DA) is proposed in this paper which are beneficial to symmetric coefficients reducing half of the multipliers in sub-filter blocks of two parallel FIR filter. The LUT less method is used to decrease the amount of required memory units in the two parallel filter structure. In proposed structure, the multipliers are replaced with shifters and adders so that adders weight less than multipliers in terms of silicon. Overweigh from the additional adders in pre-processing and post-processing blocks stay fixed along with the filter length and they doesn't increase with tap length, this is the key merit of proposed filter architectures. Overall, the synthesis result shows that the proposed two parallel FIR structure can save more than 50% of significant power and area of circuit scale and can be applied to different types of filters with different coefficients for its flexibility and high reliability.**

***Index Terms*— Two Parallel FIR filter, LUT less Distributed Arithmetic (DA), Finite Impulse Response (FIR), Adders, Multipliers and Symmetric Coefficients.**

I. INTRODUCTION

Due to increase in multimedia applications, the demand for low power and high performance Digital Signal processing (DSP) is getting higher. Finite Impulse Response (FIR) and Infinite Impulse Response (IIR) digital filters are two kinds of filters used in DSP applications. Digital filters are used in variety of applications varying from wireless communications to audio, video, image processing and digital communication systems.

Finite Impulse Response (FIR) digital filters are the most fundamental devices performed in DSP systems. Parallel Architecture increase the sampling rate by considering multiple inputs required can be processed in parallel and produce multiple

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outputs at the same time, this increases the area but this technique can reduce the power consumption by lowering the supply voltage. The area complexity in hardware implementation of FIR filter is one of the major problem. However, an N-level parallel processing can increase the number of computations i.e., multipliers and adders by N times.

In some applications, FIR filter functions as high frequencies and low power circuit with high throughput. Moreover, two techniques are used in DSP applications, they are parallel and pipeline processing.

In parallel processing technique, multiple inputs are considered and produce multiple outputs at the same time but this increases the area. In pipeline process, the critical path is decreased by interleaving the number of latches along the data path, this increase the system latency and number of latches. However, both techniques can reduce the significant power consumption but the sampling speed does not increase.

The two parallel FIR filter using traditional direct arithmetic costs considerable MAC (multiply and accumulate) blocks of different filter order. The basic idea is to replace all multiplications and additions by a shifter-accumulator. Distributed Arithmetic relies on the fact that the filter coefficients are known, so multiplying c[n]x[n] becomes a multiplication with a constant. This is an importance difference and a prerequisite for a Distributed Arithmetic design.

This proposed paper provides the principle of LUT less DA and introduced in FIR filter design. Here the bit positions which having binary values are known as prior. Instead of direct multiplication the multiply operations are carried out by a series of shifters and adders.

For example if h(k)= 0.1010, then Y=X*h(k), this can be implemented as Y=X>>1+X>>3, where >> denotes a right shift operation. By using this technique the results produce the same output as direct multiplication.

The symmetric filter coefficients are generated by MATLAB using Filter Design and Analysis (FDA) tool, which can lead to significant saving in hardware area by reducing half of the multipliers in sub-filter section in two parallel FIR filter.

II. TWO PARALLEL FIR FILTER STRUCTURES

Consider an N-tap FIR filter which can be expressed in time-domain form as:

$$Y(n)=\sum c(i)x(n-i),\ k=0,1,2,\ldots\infty \quad \ldots\ldots\ldots (1)$$

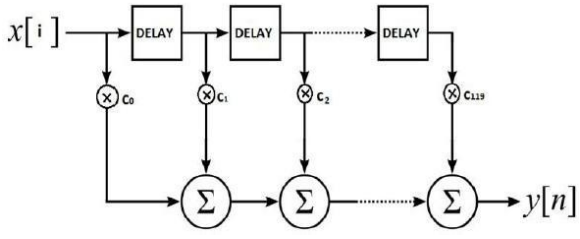

Fig.1 FIR filter

Where,
c(i) = constant or filter coefficient
x(i) = n^{th} point of input sequences is

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variable
y(n) = output system response

1) Traditional Two Parallel FIR Filter Structure

The traditional two parallel FIR filter structure is shown as,

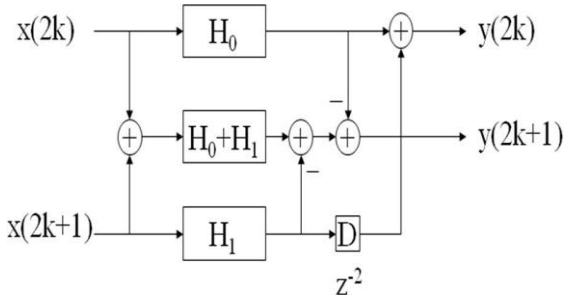


Fig.2 Traditional Two Parallel FIR Filter

The output response is given as,

$Y0 = X0\ H0 + z^{-2}X1H1$

$Y1 = (H0 + H1)(X0 + X1) – H0X0 – H1X1$ ..(2)

The hardware implementation of equation (2) requires three sub-filter blocks of length N/2 (where N is the number of taps) with one pre-processing and three post-processing adders, with totally 3N/2= 1.5N multiplication and 3(N/2-1)+4= 1.5N+4 additions.

The traditional two parallel FIR filter structure is implemented by using direct multiplication with a tap length of 24 and the simulation results are shown below.

2) Modified Two Parallel FIR Filter Structure

The traditional two parallel FIR filter structure is modified such that it earns more sub-filter blocks with symmetric coefficients so that the implementation hardware area is reduced and is shown as,

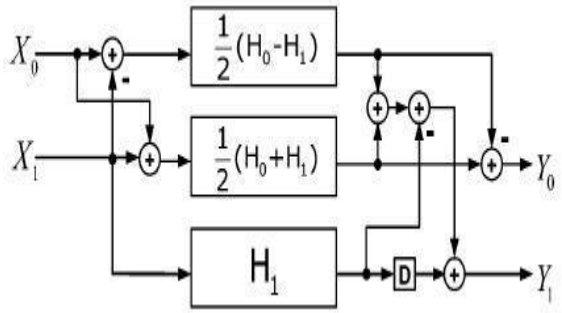


Fig.3 Modified Two Parallel FIR Filter

The output response is given as,

$Y0= \{1/2[(H0+H1)(X0+X1)+(H0-H1)(X0-X1)]- H1X1\}+Z^{-2}\ H1X1$

$Y1=\{1/2[(H_0+H_1)(X_0+X_1)-(H_0-H_1)(X_0-X_1)$ … (3)

The number of required multiplications in the single sub-filter block can be decreased by using modified structure. Therefore, the modified structure will reduce approximately one fourth over the traditional filter structure, which results in lowering of hardware cost.

The hardware implementation of equation (3) requires three sub-filter blocks of length N/2 with two pre-processing adders and four post-processing adders.

In modified structure the number of adders in pre-processing and post-processing stage has been increased but it contains two sub-filter blocks with symmetric coefficients which results in large number of reduced multipliers, but the traditional structure has only one sub-filter block with symmetry of

coefficients. The modified two parallel FIR filter structure is implemented by using direct multiplication with a tap length of 24 and the simulation results are shown below.

3) Proposed Two Parallel FIR Filter Structure

To use the symmetry of coefficients in FIR filters the proposed structure of two parallel FIR filter is implemented by using LUT less DA, such that it can earn many sub-filters blocks with symmetric coefficients which leads to reducing half of multiplications in sub-filter that can be reused for multiplications of whole taps. Hence for a L parallel, N tap FIR filter the total amount of saved multipliers will be half the total multipliers i.e., N/2L.

The proposed two parallel FIR filter structure using LUT less DA is obtained by considering modified two parallel FIR filter structure.

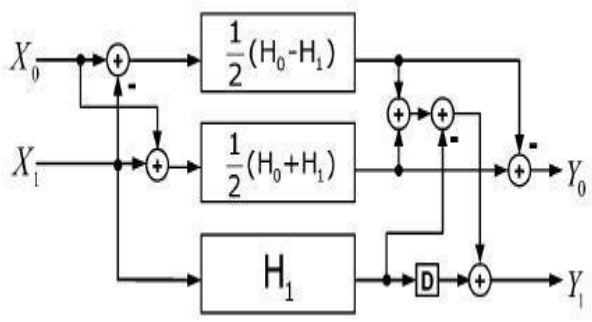


Fig.4 Proposed Two Parallel FIR Filter

using LUT less DA

The output response is given as,

$Y_0=\{1/2[(H_0+H_1)(X_0+X_1)+(H_0-H_1)(X_0-X_1)]-H_1X_1\}+Z^{-2}$ H_1X_1

$Y1=\{1/2[(H_0+H_1)(X_0+X_1)-(H_0-H_1)(X_0-X_1)]...(4)$

The proposed structure has three sub-filter blocks in which two sub-filter blocks contains symmetric coefficients. The DA with LUT less technique is applied to the proposed two parallel (L=2) FIR filter in fig.4 with a tap length of 24 and the simulation results are shown below.

III. 24 TAP FIR FILTER DESIGN

To design power and area efficient two parallel FIR filter, consider the filter coefficients which are generated from MATLAB using FDA tool by specifying the type of filter with desired frequencies and different filter order.

The design indexes of the FIR filter is given as a transposed direct-form low pass filter with sampling frequency Fs: 48KHz, pass-band frequency Fpass: 960Hz, stop band frequency Fstop: 1200Hz, filter order: 24, input data width: 8, output data width: 24.

The set of symmetric coefficients are represented as,

{h(0),h(1),h(2),h(3),h(4),h(5),h(6),h(7),h(8), h(9)

……..h(22),h(23)}.

Where

h(0)=h(23)

h(1)=h(22)

h(2)=h(21)

h(3)=h(20)

h(11)=h(12), applying to proposed two parallel FIR filter structure, the top two sub-filter blocks will be as

H0 ±H1 ={h(0)±h(1), h(2)±h(3), h(4)±h(5), h(6)±h(7),….., h(20)±h(21),

h(22)±h(23) }
Where

h(0) ± h(1) = ±(h(22) ± h(23))

h(2) ± h(3) = ±(h(20) ± h(21))

h(4) ± h(5) = ±(h(18) ± h(19))…(5)

TABLE: 1 Filter Coefficients (From MATLAB)

h(0)= h(23)= 0.156394
h(1)= h(22)= 0.07832
h(2)= h(21)= 0.043769
h(3)= h(20)= 0.090583
h(4)= h(19)= 0.041809
h(5)= h(18)= 0.043890
h(6)= h(17)= 0.364409
h(7)= h(16)= 0.004082
h(8)= h(15)= 0.077261
h(9)= h(14)= 0.410924
h(10)= h(13)= 0.49934
h(11)= h(12)= 0.05092

The filter coefficients are quantized by using Maximum Absolute Difference (MAD) algorithm. The subfilter block with half the amount of multipliers required can be realized is shown in figure,

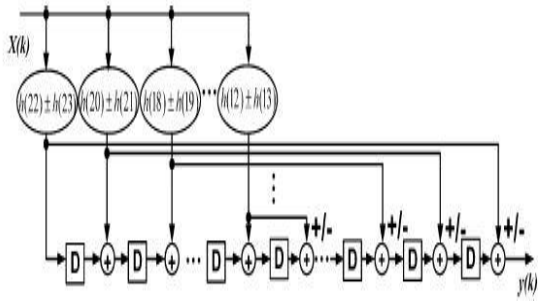
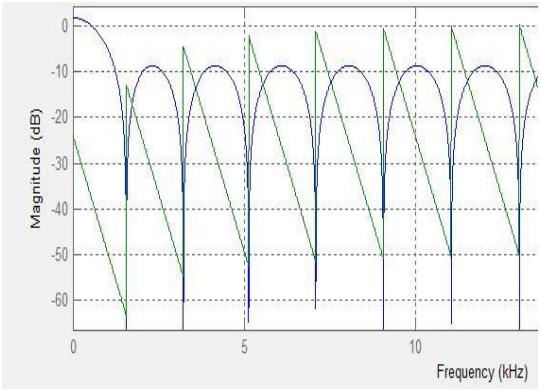


Fig.5 Subfilter Block Implementation with Symmetric Coefficients

Partition the coefficients according to the subfilter requirement such that two parallel FIR filter structure consider only N/2 coefficients in each subfilter. Therefore, for a 24-tap it takes 12 coefficients in each subfilter block. H0 takes even coefficients and H1 considers odd coefficients. Each outputs of multiplier respond to two taps.

The frequency and phase response of the low pass filter with filter order 24 is shown in figure.



IV. RESULTS

The simulation results are carried out in ModelSim altera 6.4a and area, power constraints are synthesized by using Cadence (RTL Complier) tool.

Traditional two parallel FIR filter using direct multiplication is shown as,

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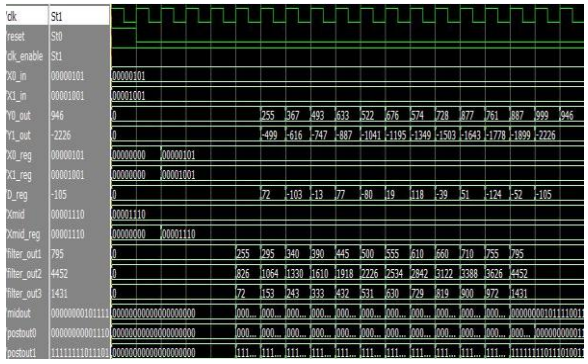

Fig.7 Simulation of Traditional Two Parallel FIR

Filter Using Direct Multiplication

Modified two parallel FIR filter using direct multiplication is shown as,

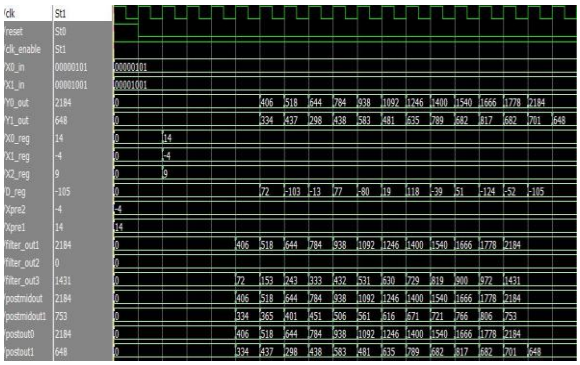

Fig.8 Simulation of Modified Two Parallel FIR Filter

Using Direct Multiplication

Two parallel FIR filter proposed using LUT less DA is shown as,

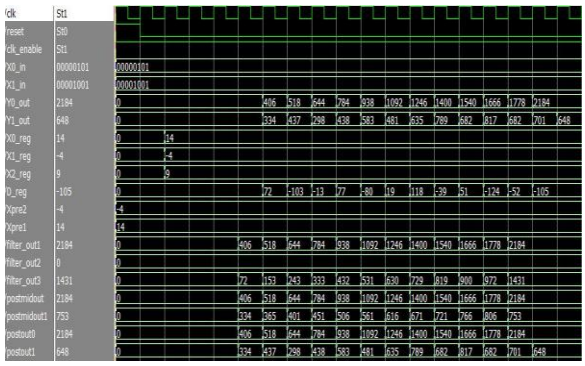

Fig.9 Simulation of Proposed Two Parallel FIR Filter Using LUT less DA

The simulation results shows that, for modified two parallel FIR filter structure using direct multiplication and proposed two parallel FIR filter using LUT less DA gives same output.

The synthesis results of area and power for traditional, modified and proposed structures of two parallel FIR filter is tabulated as,

TABLE:2 Comparison of Area and Power

TWO PARALLEL FIR FILTER	AREA (Cell Area)	POWER(µW)
TRADITIONAL STRUCTURE	636592	24.7
MODIFIED STRUCTURE	419560	12.9
PROPOSED STRUCTURE	241843	4.1

It is observed from the synthesis results, using LUT less DA for the proposed structure of two parallel gives significant

area and power savings.

V. CONCLUSION

This paper presents the design and implementation of two parallel FIR filter structure using LUT less DA. The simulation results of modified two parallel FIR filter using direct multiplication and proposed two parallel FIR filter using LUT less DA gives same output. Since multipliers consume more area and power, the proposed two parallel FIR filter structure can lead to more than 50 percent reduction in area and power by replacing the multipliers with significant amount of adders and shifters.

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