A Novel Access speed Data Retention Time Reliable Gain cell Low power operation

Mr. N. Md. BILAL[1], LAKSHMI DEVI NAKKA[2]

[1]Associate Professor Dept. of ECE, Svr Engineering College Nandyal Mail: - 404bilal@gmail.com

[2]PG-Scholar Dept. of ECE, Svr Engineering College Nandyal Mail: - nakkalakshmidevi@gmail.com

Abstract

Memories have occupied increasingly large portions of the die area of VLSI systems-on-chip (SoCs), in general, and of microprocessor. This is due to the large 6-transistor (6T) SRAM bitcell and its area-consuming peripheral circuitry that are the basis for the vast majority of these. In addition, the standby power of ultralow-power (ULP) systems, such as biomedical implants and wireless sensor networks, is often dominated by embedded memories, which continue to leak during the long retentive standby periods that characterize these systems. Logic compatible gain cell (GC)-embedded DRAM (eDRAM) arrays are considered an alternative to SRAM due to their small size, nonratioed operation, low static leakage, and two-port functionality. However, traditional GC-eDRAM implementations require boosted control signals in order to write full voltage levels to the cell to reduce the refresh rate and shorten access times. These boosted levels require an extra power supply or on-chip charge pumps, as well as nontrivial level shifting and toleration of high voltage levels. In this brief, we present a novel, logic compatible, 3T GC-eDRAM bitcell that operates with a single-supply voltage and provides superior write capability to the conventional GC structures.

Keywords: Access speed, Data Retention Time, Reliable, Embedded DRAM, Gain cell, Low power operation.

1. Introduction

In recent years, memories have occupied increasingly large portions of the die area of VLSI systems-on-chip (SoCs), in general, and of microprocessors, in particular, as shown in the latest ITRS edition [1]. This is due to the large 6-Transistor (6T) SRAM bitcell and its area-consuming peripheral circuitry that are the basis for the vast majority of these memories. In addition, the standby power of ultra-low power (ULP) systems, such as biomedical implants and wireless sensor networks, is often dominated by embedded memories which continue to leak during the long retentive standby periods that characterize these systems. 6T SRAM has been the traditional choice for the implementation of embedded memories due to its high-access speed and refresh-free static data retention. However, the 6T bitcell has several drawbacks in modern systems, including its large transistor count, its impeded functionality under voltage scaling, and the aforementioned static leakage currents from the supply voltage (VDD) to GND. One of the interesting alternative implementations that addresses these limitations, while continuing to provide full CMOS logic compatibility, is gaincell (GC) embedded DRAM (eDRAM), such as the circuit illustrated in Fig. 1(a) [2]–[5]. Most often consisting of two (2T) or three (3T) transistors, GC-eDRAMs provide a reduced silicon footprint, along with inherent 2-port functionality, nonratioed circuit operation, and very low static leakage currents from VDD to GND. However, as opposed to static memories, such as SRAM, the data retention of GC-eDRAM depends

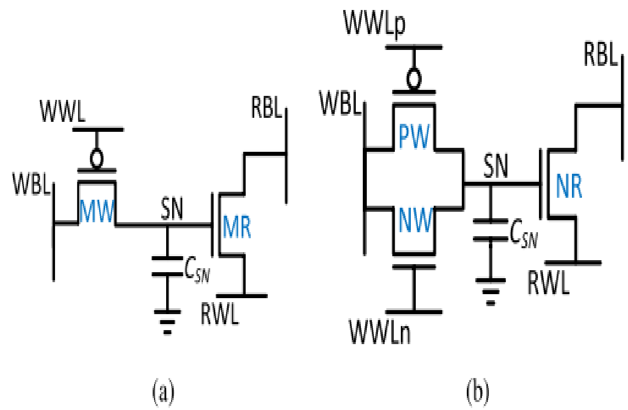

Fig 1. Schematic of conventional and proposed GCs. (a) 2T mixed GC. (b) Proposed 3T GC.

Reduced silicon footprint, along with inherent two-port functionality, nonratioed circuit operation, and very low static leakage currents from VDD to GND. However, as opposed to static memories, such as SRAM, the data retention of GC-eDRAM depends on dynamically stored charge, and thereby requires periodic, power-hungry refresh operations.

2. Related Work

2.1 EXISTING METHOD

A. 6T SRAM

Basic static RAM circuits can be viewed as vibrations on the designs used for latches and flip-flops more aggressive static RAMs make use of design tricks originally developed RAMs to speed up the system. The value is stored in the middle four transistors, of Fig.2 which form a pair on inverters connected in a loop. The other two transistors control access to the memory cell by the bit lines. When select = 0, the inverters reinforce each other to store the value. A read or write is performed when cell is selected. To read, bit and bit are precharged to before the select line is allowed to go high. One of the cell's inverters will have its output at 1, and the other at 0, which inverter is 1 depends on the value stored. The right hand inverter's pull down and the bit line will be drained to through that inverter's pull down and the bit line will remain high. If the opposite value is stored in the cell, the bit lines will be pulled own while bit remains high. To write, the bit and bit lines are set to the desired value, then select is set to 1.charge sharing forces the inverters to switch values, if necessary, to store the desired value. The bit lines have much higher capacitance than

p-ISSN: 2348-6848
e-ISSN: 2348-795X
Volume 03 Issue 12
August 2016

the inverters, so the charge on the bit lines is enough to overwhelm the inverter pair and cause it to flip state.

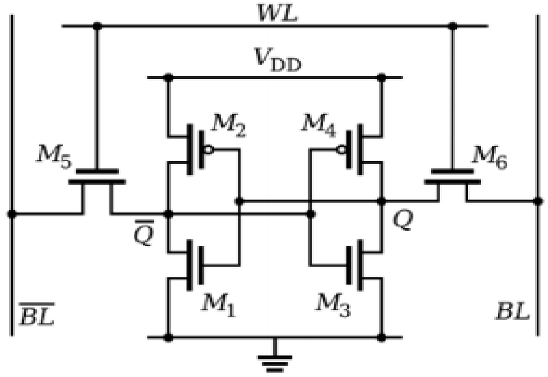

Fig 2: Fig.1 6T SRAM

B. 2T Mixed Gain Cell

2T mixed GC can be implemented with either an NMOS or a PMOS device as shown in Fig.3. Moreover, both MW (write transistor) and MR (read transistor) can be implemented with standard threshold voltage core or high threshold voltage I/O devices in the considered CMOS technology. Due to the voltage drop across MW, a boosted write word line (WWL)voltage is required during write access above for NMOS operation and below for PMOS operation. For a read operation a PMOS MR requires a pre-discharge of the parasitic RBL capacitance followed by raising the read word line (RWL). If the selected bitcell's storage mode (SN) holds a loop value,MR is conducting and charges RBL post a detectable sensing threshold. If SN holds value MR is cut-off such that RBL remains discharged below the sensing threshold. For the NMOS implementation of MR, the operation is exactly opposite i.e. RBL is precharged and RWL is lowered to initiate a read.

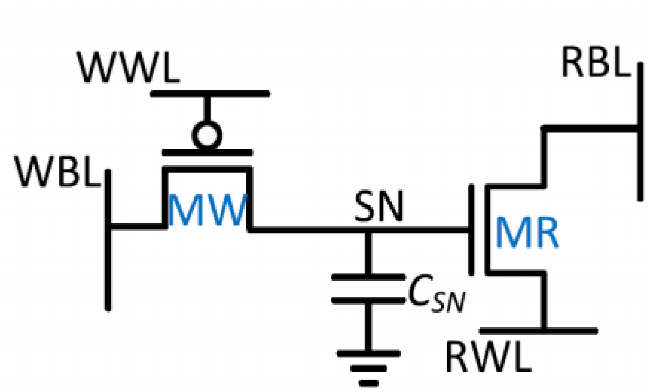

Fig 3. 2T Mixed Gain Cell.

3. Implementation

3.1 PROPOSED METHOD

In this brief, we present a new topology for a 3TGC, featuring a complementary transmission gate in the write port. While the proposed solution is quite straight forward it is novel and its impact in very high. We demonstrate the functionality of the proposed system used in ultra-low power applications such as biomedical sensor nodes and implants. The proposed 3T GC-eDRAM macro is shown to be fully functional with a supply voltage ranging from 600mv to 2.5v.

A. 3T Gain Cell eDRAM

3T GC consists of write port featuring a complementary transmission gate PMOS write (PW) and NMOS write (NW) a storage node (SN) composed of the three transistors, a read

p-ISSN: 2348-6848
e-ISSN: 2348-795X
Volume 03 Issue 12
August 2016

port based on NMOS read (NR) and the metal interconnect as in Fig 3. the GC is built that all the transistors operates with standard voltage and is fully compatible with standard digital CMOS technologies. The gates of PW and NW are connected to the world line of PMOS and NMOS WWLp and WWLn. A common write bit line is used to drive the data to the transmission gate during write operations. When the fullswing is given to the cells transmission gate enables the propagation of strong levels to the SN without any need for boosted world line. Read operation is performed by precharging the read bit line (RBL) to and subsequently driving the read word line (RWL) to GND. If the storage node is already high it discharges RBL capacitances or blocking the discharge path if SN is low. IN order to achieve a tradeoff between speed, area, power and reliability, a dynamic sense amplifier can be used to improve the read operation and its performance as described in [5],[6].

B. Operation

The circuit is described with = 900 mv. This voltage was chosen as a good medium voltage between and since the data retention time (DRT) is proved to be efficient in. GC-eDRAM design [8] at this voltage starting with charged WBL is driven low and the world lines WWLp is set to 0 and WWLn is set to. Then a strong 0 level is passed to the SN, during standby, the level on SN deteriorates due to leakage currents dominated by the sub threshold leakage of PW and NW in mature CMOS nodes. Hence in order to extend the retention time WBL is driven to during standby and read cycles thereby significantly reducing the sub threshold leakage through the transmission gate for both stored low and high values compared with the condition where WBL is either driven to either or GND. The write circuitry and read circuitry are described in section IV.A. During readout the 0 level blocks the discharge paththrough NR, maintaining the precharged voltage on RBL. During the next write operation WBL is driven high, resulting in a strong 1 stored on the SN. The subsequent read operation provides a strong gate overdrive to transistor NR, thereby discharging RBL toread a 1. It should be noted that during this operation (Read 1), bitcells storing 1 and sharing thesame column turn on when RBL discharges by more than the of NR, causing it to saturate before it can completely discharge. This phenomenon is common to many GC-eDRAM configurations, as discussed in[8].

C. Data Retention Time

The data retention time (DRT) of GC embedded DRAMS is the time interval for writing a data level in the bit cell to the last moment the data can still correctly read out the stored information. For 2T and 3T cells methodology

p-ISSN: 2348-6848
e-ISSN: 2348-795X
Volume 03 Issue 12
August 2016

which are affected by the initially degraded voltage level corresponding to the data values due to the threshold voltage (V_t) drop across the write transistor DRT is primarily limited by the initial charge stored on the internal bit cell capacitance and the leakage currents that degrade the stored voltage level over time. In order to describe this issue a boosted write world line (WWL) voltage is usually employed to pass a full swing level to the storage capacitance. Any how this requires the generation of boosted on-chip voltage, which entails substantial overhead [1]. The magnitude of the voltage boost is set not only to overcome the drop, but also to achieve short write access time which otherwise are typically longer than 6T SRAM implementation. The proposed bitcells provides strong initial data levels for enhanced DRT and robust operation as well as for fast write access time.

3.2 MEMORY MACRO PERIPHERALS

To improve the array performance in terms of access time and power consumption several peripheral techniques were integrated into the designed memory macro in the proposed technique single supply voltage is provided to the circuit which simplifies the implementation of a full memory macro. This is the significant advantage over the other GC eDRAMS that uses conventional bit cells. These bit cells require the use of level shifters to create the desired boosted or negative voltage supply depending on the types of MOS write. The peripheral circuit which is designed for this memory macro and their techniques are described as follows.

A. Readout Circuitry

Large number of ultra low power systems comprising of low voltage embedded memories consists of simple sense inverter. This sense inverter is used for the purpose of reduction in area, robust and low power readout operation however this inverter suffers from very slow data readout as it requires RBL to be discharged or charged for PMOS read device switching the threshold of the inverter. This operation is further impeded by the before mentioned. In order to overcome this limitation the readout path that was integrated into the proposed 3T GC-eDRAM macro cell has two sensing node 1). A faster dynamic sensing mode but it is potentially more error-phrone which acts in dynamic readout mode 2). A slightly slower static mode but more reliable. In both the sensing modes however threshold device PMOS transistors were used in order to allow a faster read access time due to the above mentioned problem the read out circuitry is provided the supply voltage through the read enable signal in order to save substantial static power because of the leaky low voltage

International Journal of Research
Available at https://edupediapublications.org/journals
p-ISSN: 2348-6848
e-ISSN: 2348-795X
Volume 03 Issue 12
August 2016

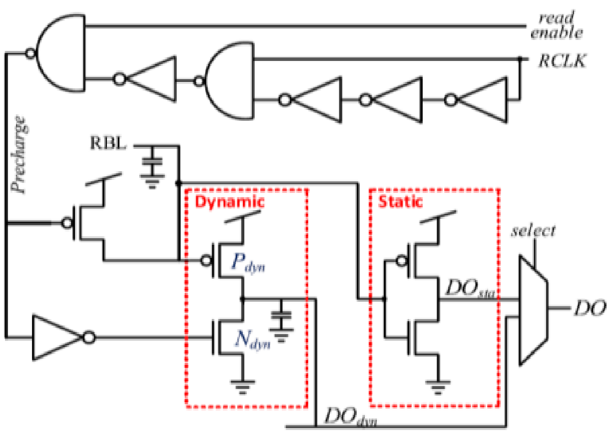

Fig 4.ReadOut Circuitry.

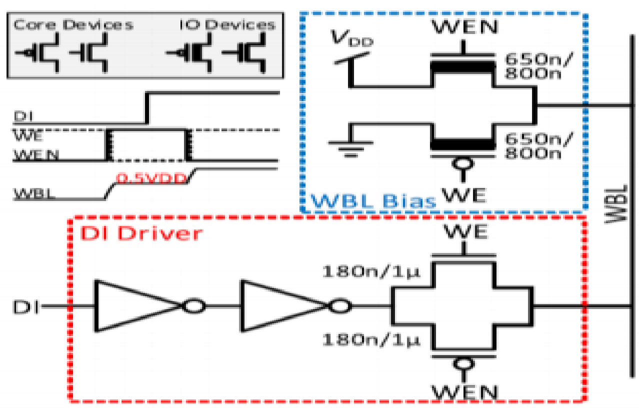

Fig 5. Write Circuitry.

threshold devices the schematic diagram with the two sensing nodes of static and dynamic are shown in Fig. 4.RBL saturation during readout that slows down the charging and discharging operation as the RBL voltage increases and decreases.

The raising edge of the read clock (RCLK) creates a precharge pulse that charges the parasitic capacitance of RBL and discharges the dynamic sense inverter output capacitance through the discharge transistor, . Subsequently RBL is conditionally discharge during read operation turning on to complement the output if high value is stored in the selected cell. Therefore an RBL swing of only one threshold voltage is required to complete a read operation.

B. Write Circuitry

The proposed single supply 3T bit cell provide a significant improvement in write time when compared to the read time, which means it has fast access time, when compared to the readout circuitry. It also has an initial SN level improvement over standard GC implementation the dual transistor write port built by means of transmission gate provides a leakage path to or from the storage node. The write circuitry to implement the median WBL bias during standby and read cycle is shown in Fig.5. The increased aggregated sub- current causes faster degradation of the stored charge, leading to reduced DRT, as compared with a reference 2T cell. In addition, several previous works have shown that the data dependent, asymmetric DRT (for data 0 and 1) of standard GCs can be manipulated to overall enhance DRTs by biasing the WBL at the best case voltage for the weaker data level during standby and read operations . For the proposed 3T configuration, the worst case DRTs of the 1 and 0 levels are similar, and significant deterioration of the stored levels occurs for both extreme values of WBL bias (VDD and GND).

4. Experimental Work

International Journal of Research
Available at https://edupediapublications.org/journals

p-ISSN: 2348-6848
e-ISSN: 2348-795X
Volume 03 Issue 12
August 2016

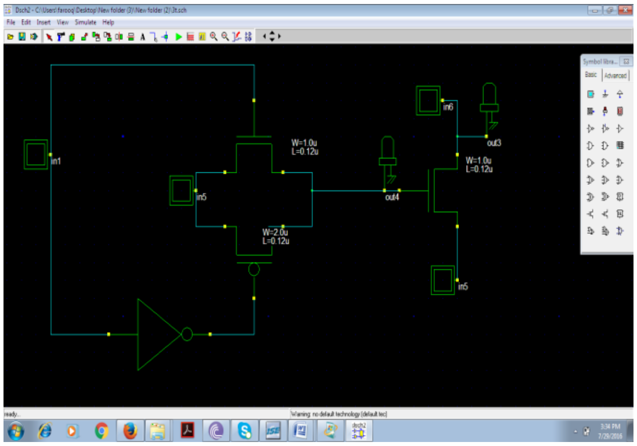

Fig :-6 Circuit of The Project

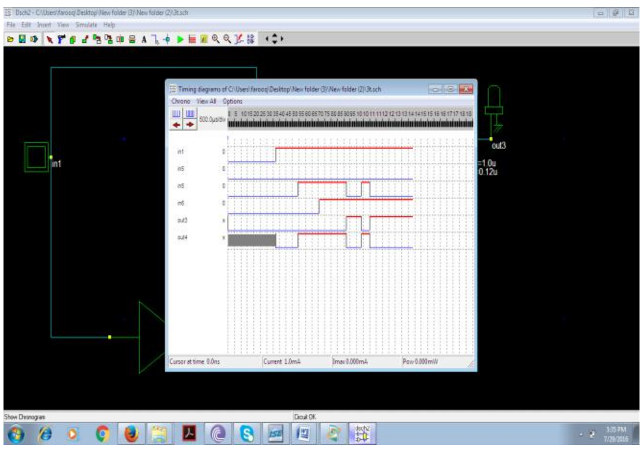

Fig :-7 Out Screes-1

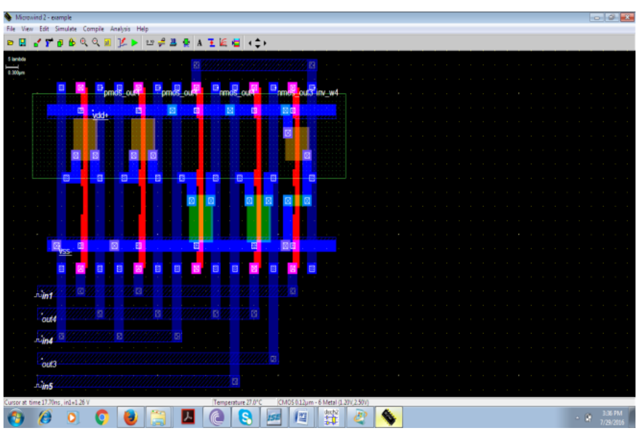

Fig :- Out Screen -2

5. Conclusion

This brief proposes a novel 3T GC eDRAM microcell targeted at ULP systems and providing high storage density. The proposed GC is operated from a single-supply voltage, eliminating the need for boosted voltages, commonly found in prior-art implementations. When compared with 6T SRAM technology and 2T mixed gain cell technology it has less consumption of power and becomes fully functional at the voltage range of 600mv to 2.5v showing a worst case Data Retention power of 4.6 nW at 900mv.The proposed cell exhibits faster write-access than conventional GC circuits, thereby increasing DRTs and reducing refresh power consumption. The average power consumption at write access time is less than that of read access time. Measurement results show full functionality at voltages ranging from 600 mv to 2.5 V with power as much as lower than a previously reported 6T SRAM in the same technology node. Testing is the major issue in eDRAM technology. So in future various testing method can be used to check the better performance of the circuit.

6. References

[1] Raychowdhuryet al., "PVT-and-aging adaptive word line boosting For 8T SRAM power reduction," in Proc. IEEE ISSCC, Feb. 2010, pp. 352353.

[2] A. Teman, P. Meinerzhagen, R. Giterman, A. Fish, and A. Burg, "Replica Technique for adaptive refresh timing of gain-cell-embedded DRAM,"IEEE Trans. Circuits Syst. II, Exp. Briefs, vol. 61, no. 4, pp. 259–263, Apr2014

[3] D. Somasekharet al., "2 GHz 2 Mb 2T gain cell memory macro with 128 GBytes/sec bandwidth in a 65 nm logic process technology,"IEEE J. Solid-State Circuits, vol. 44, no. 1, pp. 174–185, Jan. 2009.

[4] G. M. S. Reddy and P. C. Reddy, "Design and implementation of 8k-bits Low power SRAM in 180nm technology," in Proc. IMCECS, vol. 2. 2009,

[5] K. C. Chun, P. Jain, T.-H. Kim, and C. H. Kim, "A 667 MHz logic compatible embedded DRAM featuring an asymmetric 2T gain cell for high speed on-die caches," IEEE J. Solid-State Circuits, vol. 47, no. 2 pp. 547–559, Feb. 2012.

[6] K. C. Chun, P. Jain, J. H. Lee, and C. H. Kim, "A 3T gain cell embedded DRAM utilizing preferential boosting for high density and low power on die Caches," IEEE J. Solid-State Circuits, vol. 46, no. 6, pp. 1495–1505, Jun. 2011.

[7] K. C. Chun, W. Zhang, P. Jain, and C. H. Kim, "A 2T1C embedded DRAM macro with no boosted supplies featuring a 7T SRAM based Repair and a cell storage monitor," IEEE J. Solid-State Circuits, vol. 47,no. 10, pp. 2517–2526, Oct. 2012..

[8] P. Meinerzhagen, A. Teman, R. Giterman, A. Burg, and A. Fish, ―Exploration of sub-VT and near-VT 2T gain-cell memories for ultralow power applications under technology scaling,‖ J. Low Power Electron. Appl., vol. 3, no. 2, pp. 54–72, 2013.

[9] W. Zhang, K. C. Chun, and C. H. Kim, ―A write-back-free 2T1D Embedded DRAM with local voltage sensing and a dual-row-access low Power mode,‖ IEEE Trans. Circuits Syst. I, Reg. Papers, vol. 60, no. 8,pp. 2030–2038, Aug. 2013

[10] Y. Lee, M.-T. Chen, J. Park, D. Sylvester, and D. Blaauw, ―A 5.42nW/kB retention power logic-compatible embedded DRAM with 2T dual-Vt gain cell for low power sensing applications,‖ in Proc. IEEE ASSCC,Nov. 2010, pp