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A New Current Sharing Technique on a General Case of Paralleled Dc-Dc Boost Converters

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Abstract—In this project, a new current sharing technique on a general case of N paralleled DC–DC boost converters is presented. The proposed optimization is based on the knowledge of individual boost parameters. Every loss through the structure are modeled by equivalent resistors. Using an accurate online estimation of those resistors, the losses through each individual converter can be determined. Then, a new current sharing scheme is defined aiming to maximize the global efficiency of the overall structure. To verify the proposed method, simulations and experiments have been realized on a three-parallel boost converters structure.

Index Terms—Boost converters, current-sharing, parallel converters, parameter estimation.

I.INTRODUCTION

First, paralleling dc–dc converters allows a reduction of the size of components, especially inductive ones. It also reduces stress among individual converters by segmenting the total power, leading to a better global efficiency. Furthermore, this leads to an enhanced reliability, and allows possible reconfigurations when one or more of the paralleled modules present malfunctioning. In non isolated applications, the boost converter is one of the most used since it is well known and allows good efficiency. In this paper, an *N* parallel boost converters structure with one output capacitor is considered, as shown in Fig. 1. A good reliability of energy conversion is always needed. By diagnosing the fault in its early stages, the reliability of the power conversion system can be increased significantly [2]. To achieve this, it is very interesting to develop an efficient online parameter estimation. Many parameter estimation techniques have already been proposed for dc–dc boost converters. For example, in [3] and [4] a method to estimate inductance, capacitor, capacitor serial resistance, and load is presented. One of the main disadvantages of the proposed technique, as for those proposed in [5] and [6], is that it requires a sampling frequency much higher than switching frequency. For the present application, the sampling frequency is kept equal to the switching frequency. For this reason, Shahin *et al.* In most of the literature, the current repartition is only designed in order to allow the system to work. However, as it will be underline in this paper, the repartition can influence on the global structure efficiency. Classically, this is not taken into account. In this aim, the new sharing scheme proposed in this paper allows us to maximize the global efficiency of the overall structure.

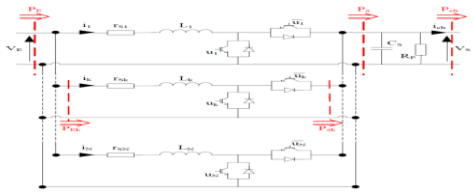


Fig. 1. N parallel boost converters structure with one output capacitor.

II. MODELLING OF SYSTEM AND ESTIMATION

A. Model Of The Structure

The system consists in *N* parallel boost converters with one output capacitor as shown in Fig. 1. The considered modeling equations (1a) and (1b) are a direct application of Shahin *et al.* work. In this paper, it is proposed to model losses through a boost converter by adding *N* serial and one parallel resistors in the conventional ideal model. For the considered application, each individual boost converter model has a serial resistance *rsk* , while a unique parallel resistor *Rp* includes all the rest of the

losses for the whole structure. This difference with the method proposed comes from the nature of the structure with only one output capacitor and one output current sensor. The next section details the method to obtain an accurate online estimation of the resistor values

$$\begin{cases} L_k \dfrac{\mathrm{d}i_k}{\mathrm{d}t} = V_{in} - r_{s_k} i_k - (1-d_k) V_o & \text{(1a)} \\ C_o \dfrac{\mathrm{d}V_o}{\mathrm{d}t} = \displaystyle\sum_{k=1}^{N} (1-d_k) i_k - i_{\mathrm{Load}} - \dfrac{V_o}{R_p} & \text{(1b)} \end{cases}$$

where *dk* represents the duty cycle corresponding to the PWM output signal *uk* . Even if the adopted loss modeling is only represented through resistors, it is useful to underline that not only ohmic losses are taken into account. In fact, every loss through the converter is taken into account with those of equivalent resistors, such as core hysteresis and eddy current losses, conduction ohmic losses, and switching losses of semiconductors. Particularly, the parallel resistor Rp does not only represent the capacitor *Co* losses through its ESR. Indeed, it is well known the even under zero power, boost converters still present losses, which will be taken into account through parameter Rp while serial resistor is not able to model this behavior. Finally, parameters Rsk and Rp represent the overall losses through the structure. This will be verified in the experimental part by checking that calculated losses correspond to Measurement. For a more detail description of this loss modeling technique, the reader is invited to read reference, where analytical study is presented, as well has load dependence behavior of such a modeling in the case of a single-boost converter. It has to be noticed that the estimation of losses through the converters can also been used for others purpose. As an example, it can be used for verifying the ageing of the individual converters by checking on the variations of the estimated equivalent resistors. This aspect cannot be developed in this paper since it is not its goal, but reader is again invited to read for more details on the estimation.

B. Parameters Online Estimation

Before designing control laws and current-sharing technique, the system parameters need to be estimated. This has to be realized by considering online sampled signals, namely, *V*in, *ik, Vo* and *i*Load . It is possible to estimate the equivalent loss resistors following (2) and (4). Considering that the input power follows its reference *P*in = *P* in ref ∀*t*, serial resistors will be estimated through (2). This condition will be ensured with the current regulation presented in Section III

$$\frac{\mathrm{d}\hat{r}_{s_k}}{\mathrm{d}t} = \lambda_{s_k} \cdot \left(\hat{P}_{\mathrm{out}_k} - P_{\mathrm{out}_k}\right) \cdot \left(\frac{V_{\mathrm{in}}}{P_{\mathrm{in}_k}}\right)^2. \qquad (2)$$

Where power Poutk and estimated power follow(3), and *λsk* convergence coefficients corresponding to serial resistor *rsk*

$$\begin{cases} P_{\mathrm{out}_k} = (1-d_k) V_o i_k \\ \hat{P}_{\mathrm{out}_k} = P_{\mathrm{in}_k} - \hat{r}_{s_k} \left(\dfrac{P_{\mathrm{in}_k}}{V_{\mathrm{in}}}\right)^2. \end{cases} \qquad (3)$$

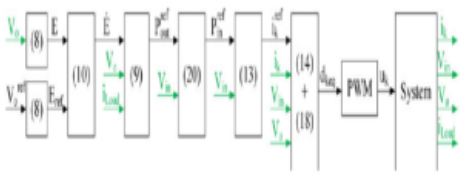
Then, considering the output voltage perfectly regulated (*Vo* = *V* refo ∀*t*), the parallel resistor will be estimated through (4). This condition will be ensured through the energy regulation presented in the following section

$$\frac{\mathrm{d}\hat{R}_p}{\mathrm{d}t} = \lambda_p \cdot \left(\hat{i}_d - i_d\right) \cdot \frac{\hat{R}_p^2}{V_o}. \qquad (4)$$

Where current *id* = _*k* (1 - *dk*) *ik* , estimated current^*id* = *i*Load + *Vo*^*Rp*, and *λp* convergence coefficient for parallel resistor *Rp* .

C. Stability Of The Estimation

Exponential stability can be proved easily with the classical Lyapunov approach . The stability and dynamics of the proposed estimations are determined by coefficients *λsk* and *λp* . In order to demonstrate their stability, the Lyapunov candidate



functions following (5) are defined as

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$$\begin{cases} V(\hat{r}_{s_k}) = \frac{1}{2}\left(\hat{P}_{\text{out}_k} - P_{\text{out}_k}\right)^2 \\ V\left(\hat{R}_p\right) = \frac{1}{2}\left(\hat{i}_d - i_d\right)^2. \end{cases} \quad (5)$$

For a positive input power, their derivative can be expressed through (6)

$$\begin{cases} \dot{V}(\hat{r}_{s_k}) = \left(\hat{P}_{\text{out}_k} - P_{\text{out}_k}\right) \frac{\mathrm{d}\left(\hat{P}_{\text{out}_k} - P_{\text{out}_k}\right)}{\mathrm{d}\hat{r}_{s_k}} \frac{\mathrm{d}\hat{r}_{s_k}}{\mathrm{dt}} \\ \dot{V}\left(\hat{R}_p\right) = \left(\hat{i}_d - i_d\right) \frac{\mathrm{d}\left(\hat{i}_d - i_d\right)}{\mathrm{d}\hat{R}_p} \frac{\mathrm{d}\hat{R}_p}{\mathrm{dt}} \end{cases} \quad (6)$$

The derivatives of Lyapunov functions (6) can be simplified in view of (2) and (4), leading to (7)

$$\begin{cases} \dot{V}(\hat{r}_{s_k}) = -\lambda_{s_k}\left(\hat{P}_{\text{out}_k} - P_{\text{out}_k}\right)^2 \le -2\lambda_{s_k} V(\hat{r}_{s_k}) \\ \qquad\qquad \forall \lambda_{s_k}, \lambda_p > 0 \\ \dot{V}\left(\hat{R}_p\right) = -\lambda_p\left(\hat{i}_d - i_d\right)^2 \le -2\lambda_p V\left(\hat{R}_p\right). \end{cases} \quad (7)$$

Then, by choosing those two parameters positive, it is demonstrated that the estimation errors exponentially converge to 0.

III. CONTROL DESIGN

To ensure the control of the structure, it has been decided to design a two-loop control scheme. A first controller enables voltage regulation through energy control. It is based on flatness control method. A second-loop controller, based on sliding method, ensure the current regulation for each individual converter. The proposed control strategy ensures asymptotic stability, robustness against parameter variations, and high dynamics regulation. A block schematic of the entire control is given in Fig. 2.

A. Energy Control Loop Based On Flatness

Flatness was firstly defined by Fliess *et al.* using the formalism of differential algebra. It has been decided to indirectly control the output voltage *Vo* by regulating the energy *E* (8) stored in the capacitor *Co* . As detailed in and, it is possible to demonstrate that *E* is a flat output for the considered system in view of (1a) and (1b)

$$E = \frac{1}{2} C_o V_o^2. \quad (8)$$

To obtain a relationship between the input current references *i*ref*k* and the flat output system *E*, the derivative $\dot{E}$ is considered as

$$\dot{E} = P_{\text{out}} - P_{\text{Load}} - \frac{V_o^2}{R_p}. \quad (9)$$

To ensure reference tracking, a second-order control law as (10) is proposed to cancel the static error

$$\left(\ddot{E}_{\text{ref}} - \dot{E}\right) + 2\xi_E \omega_{n_E}\left(\dot{E}_{\text{ref}} - \dot{E}\right) + \omega_{n_E}^2 \int \left(E_{\text{ref}} - E\right) \mathrm{dt} = 0. \quad (10)$$

The power *P*out is given as follows:

$$P_{\text{out}} = P_{\text{in}} - \sum_{k=1}^{N} r_{s_k}\left(\alpha_k \frac{P_{\text{in}}}{V_{\text{in}}}\right)^2. \quad (11)$$

The parameters α_k are power repartition coefficients. In the next section, a new current-sharing scheme aiming to maximize the overall efficiency will be detailed as a function of the parameters α_k . However, in order to transfer the needed power through the structure, repartition coefficients must follow:

$$\sum_{k=1}^{N} \alpha_k = 1 \quad \Rightarrow \quad \alpha_N = 1 - \sum_{k=1}^{N-1} \alpha_k. \quad (12)$$

Finally, current references are deduced from (13). Parameter *P*ref in of this equation will be defined in Section IV

$$i_k^{\text{ref}} = \alpha_k \frac{P_{\text{in}}^{\text{ref}}}{V_{\text{in}}}. \quad (13)$$

B. Current Loops Design—A Sliding Approach

To ensure current regulation, it has been decided to design a sliding-based controller as used in. Sliding based control allows robust regulation and has been detailed in. It has already been applied on the case of paralleled boosts in [28] where robustness againstinductor variations is underlined and guaranteed. For each individual boost converter, the sliding surface *Sk* is defined as follows:

$$S_k = \left(i_k - i_k^{\text{ref}}\right) + K_{i_k} \int \left(i_k - i_k^{\text{ref}}\right) \mathrm{dt}. \quad (14)$$

The current *ik* will follow its reference *i*ref*k* if the derivative of the surface *Sk* verify

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$$\dot{S}_k = -\lambda_{i_k} S_k. \qquad (15)$$

Equations (14) and (15) can be expressed as

$$\dot{\epsilon_k} + (K_{i_k} + \lambda_{i_k})\,\epsilon_k + K_{i_k}\lambda_{i_k} \int \epsilon_k \, dt = 0 \qquad (16)$$

where *Kik* and *λik* are the current regulation parameters and Comparing (16) with a second-order law, it is

TABLE I
REGULATION PARAMETERS

	Parameter	Value
Energy Control Loop	ξ_E	0.7
	ω_{n_E}	100 *rad/s*
Current Regulation	K_{i_k}	2000 *rad/s*
	λ_{i_k}	2000 *rad/s*
	ω_{i_k}	2000 *rad/s*

possible to express current regulation pulsation *ωI* as

$$\omega_{I_k}^2 = K_{i_k}\lambda_{i_k}. \qquad (17)$$

By combining (1) and (15), it is possible to determine the equivalent duty cycle *dk*e q allowing a good reference tracking

$$d_{k_{eq}} = 1 + \frac{1}{V_o}\left[r_{s_k} i_k - V_{in} + L_k\left(-\lambda_{i_k} S_k + \frac{di_k^{ref}}{dt} - K_{i_k}\left(i_k - i_k^{ref}\right)\right)\right]. \qquad (18)$$

C.RegulationParameters

For simulations and experimental validation, the switching frequency is set to *fs* = 20 kHz. Table I shows parameters of the controllers. Parameters *ωik* are chosen in order to verify (19) which is necessary to ensure the validity of the used mean model. In a two-loop control scheme, dynamics of the regulation must be separated, then *ωnE* is chosen in order to satisfy

$$\begin{cases} \omega_s = 2\pi f_s \gg \omega_{i_k} & (19a) \\ \omega_{i_k} \gg \omega_{n_E}. & (19b) \end{cases}$$

IV. SIMULATION RESULTS

Simulation on three-parallel boost converters have been realized to verify the effectiveness of the proposed method. First, the current repartition is set to αk = 13 . At time *t* = 0.5 s, the proposed power repartition is enabled. Parameters taken for simulation are the same as those listed in Table II for experimental verification. Serial and parallel resistors of the simulated model are chosen constant for an easier computation. To validate our purpose, the simulated paralleled boost converters on which the proposed control is applied present different efficiencies for each individual converter. This is simulated by imposing *rs*1 = 0.39 Ω, *rs*2 = 0.39Ω, and *rs*3 = 1.40Ω traducing more losses through the third individual converter. This difference between serial resistors is only one modeling of a poorer behavior of the third converter. On a real boost converter, many reasons can lead to such results, as many different losses are taken into account through this resistor (see Section II-A and reference for more details). First, it is ensured that the estimated resistors converge to their simulated values. Then, from (22), it is possible to calculate optimal repartition coefficients as

$$\begin{cases} \alpha_1^{opt} = 0.439 \\ \alpha_2^{opt} = 0.439 \\ \alpha_3^{opt} = 0.122. \end{cases}$$

This results on different current references for each converter. Fig. 5 shows current on the previously described control scheme. Fig. shows the efficiency of the structure. In this figure, the efficiency of the proposed current-sharing scheme can be observed. Indeed, when total power is equally divide through elements (*t* < 0.5 s), efficiency is about 2.4% less than the efficiency with the proposed method. Note that the difference with respect to experimental result comes from the hypothesis that estimated resistors are constant. In practice, those resistors change with respect to the power as well described. This is also the reason why their is no long transitory in simulation, as explained in the experimental part. In view of these results, another advantage of the proposed current sharing can be underlined. As shown in Fig. 5, the proposed repartition leads to a lower current in the less efficient converter. Then,

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this converter will suffer lower stress than better converters. Finally, it can be assumed that the proposed current-sharing scheme leads to make uniform ageing of the paralleled modules. Only ageing tests can corroborate this assertion but this aspect will not be treated in this paper. This property should have an effect on the structure health improving its long-term reliability and facilitating its maintenance. For example, a three-parallel boost converter structure can be easily realized using integrated circuits planned for inverters. In this case, the ageing uniformity resulting from the proposed current sharing scheme, will ensure a replacement of the

used module when all the semiconductors are deficient. On the other hand, for classical methods, the replacement can be needed for only one of the converters presenting malfunctioning

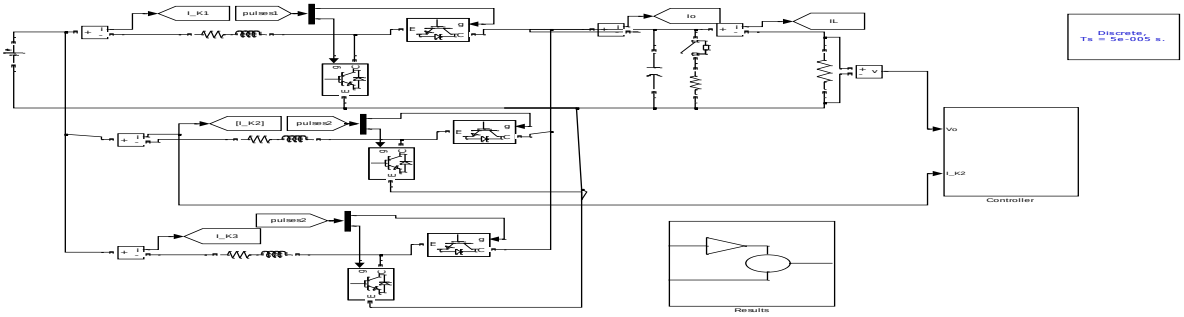

Fig 2 : Simulation model for proposed system

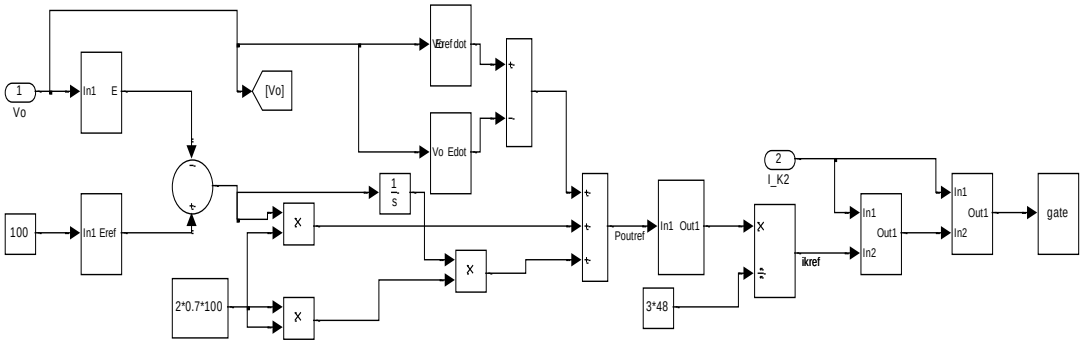

Fig 3: Controller subsystem

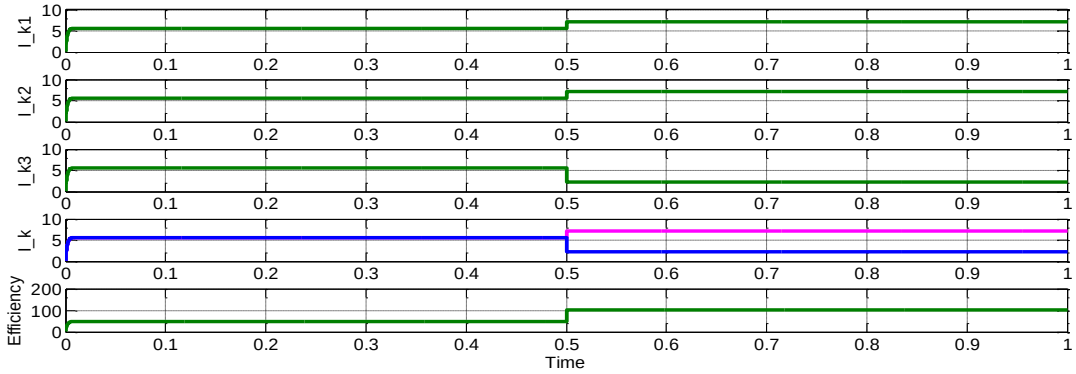

Fig. 4. Simulated average input currents *ik* .

V.CONCLUSION

A new current-sharing technique on parallel dc–dc boost converters has been presented in this paper. Through online estimation, individual converter losses are deduced and power repartition coefficients are redefined in order to maximize the efficiency of the overall structure. Output voltage and individual input currents are regulated through a two-loop control design based on flatness theory and sliding mode controllers. Compared with the most used current-sharing technique consisting in equal repartition, the proposed method shows its interest when one or more converter in parallel present malfunctioning. In these conditions, the presented method allows a gain in efficiency up to 4.5% in the tested cases, depending on the load power. Another benefit of the proposed repartition is the fact that it leads to uniform ageing between the paralleled elements. This should have an effect on the structure health improving its long-term reliability and facilitating its maintenance. Long-term experimentations are required to attest this last assumption and will be part of future works. The presented current sharing has been discussed, verified, and tested both by simulation and experiment. The validation has been realized on the case of a three-parallel boost converter structure, but the concept can easily be scaled to any number of phases. Indeed, theoretical study has been led on the general case of *N* converters in parallel. Practically, each phase will need its own current regulation, its own serial resistor estimation, and the repartition coefficients calculation will require only a few more time as the number of converter increase.

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