

Design of Reconfigurable Structure for Efficient and Scalable Orthogonal Approximation of DCT in FPGA Era

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ABSTRACT:

This paper presents a generalized recursive formula to obtain orthogonal approximation of DCT where roughly DCT of length might be produced from some DCTs of length at the cost of additions for input preprocessing. Many of the existing computations for approximation within the DCT target just the DCT of small transform measures and most of them are non-orthogonal. Approximation of discrete cosine transform (DCT) is helpful for reducing its computational complexity without major effect on its coding performance. We perform recursive sparse matrix decomposition and use the symmetries of DCT basis vectors for deriving the suggested approximation formula. Suggested formula is extremely scalable for hardware furthermore to software implementation of DCT of greater measures, plus it will make technique existing approximation of 8-point DCT to obtain approximate DCT connected getting an

electrical two length. We show the suggested approximation of DCT provides comparable or better image and video compression performance compared to existing approximation techniques. It's proven that suggested formula involves lower arithmetic complexity in comparison while using the other existing approximation computations. We've presented an entirely scalable reconfigurable parallel architecture for the computation of approximate DCT while using suggested formula. One distinctively interesting feature within the suggested design is it might be configured for the computation in the 32-point DCT or parallel computation of two 16-point DCTs or four 8-point DCTs obtaining a marginal control overhead. The suggested architecture can be found to provide several positive aspects in relation to hardware complexity, regularity and modularity. Experimental results acquired from FPGA implementation show the benefit of the suggested method.

Keywords: *Algorithm-architecture code sign, DCT approximation, discrete cosine*

transform (DCT), high efficiency video coding (HEVC).

I. INTRODUCTION

Lately, significant work continues to be completed to derive approximate of 8-point DCT for lowering the computational complexity. The necessity of approximation is much more essential for greater-size DCT because the computational complexity from the DCT develops nonlinearly. However, modern video coding standards for example high quality video coding (HEVC) uses DCT of bigger block dimensions to have greater compression ratio. The multiplications which consume the majority of the power and computation-time, and also to obtain significant estimation of DCT too. The discrete cosine transform (DCT) is commonly utilized in image and video compression [1]. Because the DCT is computationally intensive, several calculations happen to be suggested within the literature to compute it efficiently. Haweel has suggested the signed DCT (SDCT) for 8 8 blocks in which the basis vector elements are changed by their sign. They've provided a great estimation from the DCT by changing the foundation vector elements

by, 1/2, 1. Different color leaves, Bayer and Contra have suggested two transforms produced from and 1 as aspects of transform kernel, and also have proven their techniques perform much better than the technique, designed for low- and-compression ratio situations. But, the extension from the design strategy utilized in H264 AVC for bigger transform dimensions, for example 16-point and 32-point isn't feasible. Besides, several images processing programs for example monitoring and synchronized compression and file encryption require greater DCT dimensions. Within this context, Cintra features a brand new type of integer transforms relevant to many block-measures. Lately, two new transforms happen to be suggested for 8-point DCT approximation. The very first technique is for length, 16 and 32 and is dependent on the right extension of integer DCT [2]. Also, an organized way of creating a binary form of high-size DCT (BDCT) using the sequence-purchased Walsh-Hadamard transform (SO-WHT) is suggested. This

transform is really a permuted form of the WHT which approximates the DCT perfectly and keeps all the benefits of the WHT. A plan of approximation of DCT must have the next features: i) it ought to have low computational complexity. ii) It ought to have low error energy to be able to provide compression performance near to the exact DCT, and ideally ought to be orthogonal. iii) It ought to work with greater measures of DCT to aid modern video coding standards, along with other programs like monitoring, surveillance, and synchronized compression and file encryption. However the existing DCT calculations don't provide the very best of all of the above three needs. A few of the existing techniques are deficient when it comes to scalability, generalization for greater dimensions, and orthogonally. We intend to maintain orthogonally within the approximate DCT for 2 reasons. First of all, when the transform is orthogonal, we are able to always find its inverse, and also the kernel matrix from the inverse transform is acquired just by transposing the kernel matrix from the forward transform. This selection of inverse transform could be employed to compute the forward and

inverse DCT by similar computing structures. Furthermore, just in case of orthogonal transforms, similar fast calculations are relevant to both forward and inverse transforms [3]. Within this paper, we advise a formula to derive approximate type of DCTs which satisfy all of the three features. We have the suggested approximate type of DCT by recursive decomposition of sparse DCT matrix. It's observed that suggested algorithm involves less arithmetic complexity compared to existing DCT approximation calculations. The suggested approximate type of DCT of various measures is orthogonal, and lead to lower error-energy in comparison towards the existing calculations for DCT approximation. The decomposition process enables generalization from the suggested transform for greater-size DCTs. Curiously, suggested formula is definitely scalable for hardware in addition to software implementation of DCT of greater measures, and it could make utilization of the greatest of the existing approximations of 8-point DCT. In line with the suggested formula, we've suggested a completely scalable, reconfigurable, and parallel architecture for approximate DCT computation. One

distinctively interesting feature of suggested design would be that the structure for that computation of 32-point DCT might be configured for parallel computation of two 16-point DCTs or four 8-point DCTs.

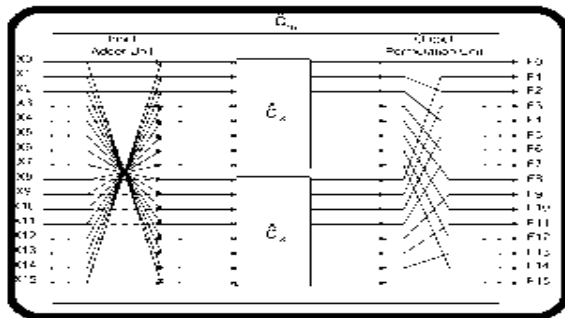


Fig.1. Proposed DCT structure

II. PROPOSED MODEL

For approximation of we are able to pick the 8-point DCT, since that is definitely the best trade-off between the amount of needed arithmetic operators and excellence of the reconstructed image. Therefore, when we replace by, we shall have two primary advantages. First of all, we shall have good compression performance because of the efficiency of and next the implementation is going to be much easier, scalable and reconfigural. For approximation of we've investigated two other low-complexity options, as well as in the next we discuss here three possible options of approximation of. We haven't done thorough search of

possible solutions. To locate these approximated sub matrices we go ahead and take tiniest size DCTmatrix to terminate the approximation procedure to eight, since 4-point DCT and a pair of-pointDCT could be implemented by adders only. Consequently, a great approximation of, where's an important power two, for, results in a proper approximations. So there might be other possible low-complexity implementation. We discuss the suggested scalable architecture for that computation of approximate DCT of and 32. We has derived the theoretical estimate of their hardware complexity and discusses the reconfiguration plan. Observe that structures of 16-point DCT might be extended to get the DCT of greater dimensions. To evaluate the computational complexity of suggested -point approximate DCT, we have to determine the computational price of matrices The amount of arithmetic procedures involved with suggested DCT approximation of various measures and individuals from the existing competing approximations. It may be discovered that the suggested method necessitates the cheapest quantity of additions, and doesn't require any shift procedures [4]. Observe

that shift operation doesn't involve any combinational components, and needs only rewiring during hardware implementation. However it has indirect contribution towards the hardware complexity since shift-add procedures result in rise in bit-width which results in greater hardware complexity of arithmetic models which stick to the shift-add operation. Also, we observe that all considered approximation techniques involve considerably less computational complexity over those of the precise DCT calculations. Pipelined and non-pipelined types of different techniques are developed, synthesized and validated utilizing an integrated logic analyzer. Observe that both pipelined and non-pipelined designs involve exactly the same quantity of LUTs since pipeline registers don't require additional LUTs. For 8-point DCT, we've used the approximation suggested, which forms the fundamental computing block from the suggested method [5]. Also, we underline that designs have a similar critical path and accordingly have a similar MOFs. Most significantly, the suggested designs are multiple-use for various transform measures. Therefore, confirmed DCT architecture ought to be potentially reused for that DCT

of various measures rather than using separate structures for various measures. We advise here such reconfigurable DCT structures that could be reused for that computation of DCT of various measures. The reconfigurable architecture for that implementation of approximated 16-point DCT It includes three computing models, namely two 8-point approximated DCT models along with a 16-point input adder unit that creates. It performs the calculation of the 32-point DCT or two 16-point DCTs in parallel or four 8-point DCTs in parallel. The architecture consists of 32-point input adder unit, two 16-point input adder models, and 4 8-point DCT models. The configurability is accomplished by three control blocks made up of 64 2:1 MUXes together with 30 3:1 MUXes. The very first control block decides if the DCT dimensions are of 32 or lower. To judge the performance from the suggested formula for video coding we've integrated the suggested approximated DCT into HEVC reference software HM12.1.

FPGA DESIGN FLOW:

In this part of tutorial we are going to have a short intro on FPGA design flow. A

simplified version of design flow is given in the flowing diagram

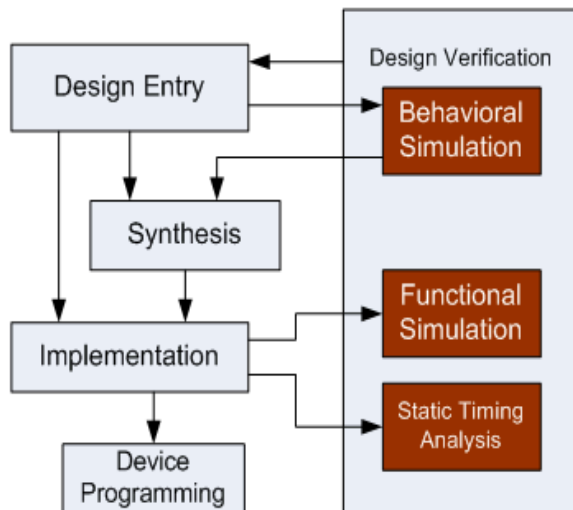


Fig: fpga Design Flow

III. CONCLUSION

The suggested approximated DCT has lots of advantages, such by regularity, structural simplicity, lower-computational complexity, and scalability. We've also suggested a completely scalable reconfigurable architecture for approximate DCT computation in which the computation of 32-point DCT might be configured for parallel computation of two 16-point DCTs or four 8-point DCTs. Within this paper, we've suggested a recursive formula to acquire orthogonal approximation of DCT where approximate DCT of length might be produced from a set of DCTs of length at the expense of additions for input preprocessing.

Comparison with lately suggested competing techniques shows the potency of the suggested approximation when it comes to error energy, hardware sources consumption, and compressed picture quality.

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BIOGRAPHY



Rakesh Gupta (2014 -2016) is pursuing Master of Technology in Embedded System Design in St. Martin's Engineering College Affiliated to Jawaharlal Nehru Technological University Hyderabad (JNTUH). He completed his Bachelor of Technology in Electronics and communications from St. Martin's Engineering College, Hyderabad in 2012. He worked as Embedded Engineer in field of Home Automation and also conducted various Realtime workshops for engineering students on various latest technologies in various Engineering colleges across India.



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