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Improved Power Factor In Bridgeless Converter by Fuzzy Controlled Based SMPS Applications

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Abstract – power factor corrected (PFC) Switched Mode Power Supply (SMPS) based on bridgeless Buck-Boost converter topology with fuzzy logic control is proposed and is compared with the conventional SMPS. The multiple outputs of the SMPS are +12V,-12V, +5V,-5V for PC applications. To obtain nearly unity power factor and reduction in total harmonic distortion (THD) of input current, the SMPS with buck-boost converter based topology is designed to operate in discontinuous conduction mode (DCM). DCM operation gives added advantages of improved power factor and reduced switching losses and reduces the complexity of circuit operation. The presence of only two switches in the current conduction path during each switching cycle and the absence of diode bridge rectifier results in reduced conduction losses and an improved power factor, as compared to the conventional SMPS Single-phase ac supply is fed to a pair of back-to-back-connected buck–boost converters to eliminate the diode bridge rectifier, which results in reduction of conduction losses and power quality improvement at the front end. The operation of the bridgeless buck–boost converter in discontinuous conduction mode ensures inherent PFC operation and reduces complexity in control. To observe the performance of this converter, a model based on the Cuk topology has been designed and developed by using MATLAB/ SIMULINK software and implemented with Proportional-Integral (PI) and Fuzzy logic controller. The simulations are demonstrated in order to validate the effectiveness of the controllers in power factor improvement.

Index Terms—Bridgeless buck–boost converter, discontinuous conduction mode (DCM), multiple output switched-mode power supply (SMPS), power factor (PF) correction (PFC), Fuzzy Logic Controller.

I. INTRODUCTION

The growth of consumer electronics has meant that the average home has a lot of mains driven electronic devices such as low energy lighting, battery chargers,televisions, and computers their peripherals etc. Invariably these electronic devices have mains rectification circuits, which is the dominant cause of mains harmonic distortion [1-4]. Most applications comprising of ac-dc power converters need the output dc voltage to be well regulated with good steady-state as well as transient performance [5].

The circuit which was typically favored until recently (diode rectifier-capacitor filter) for the utility interface minimizes the cost, but it severely deteriorates the quality of the supply thereby affecting the performance of other loads connected to it also causing other well-known problems. The current waveform is very peaky, non-sinusoidal, and highly distorted; the PF is around 0.48 [6-8]. At full load, the total harmonic distortion (THD) of input ac mains current is 83.5%. The performance of the power supply is violating the limits set by various international standards such as the International Electro technical Commission (IEC) [9].

Due to these issues, improved-power-quality SMPSs are extensively being researched, which are expected to draw a sinusoidal input current at a high PF. Improvement in power quality also results in better reliability and enhanced efficiency [10]. To achieve a perceivable improvement in power quality, PF correction (PFC) circuits are employed in these SMPSs at the utility interface point. Active power factor correction refers to the method of increasing PF by using active electronic circuits with feedback that control the shape of the drawn current. High-frequency switching techniques have been used to shape the input current waveform successfully [11].

Multiple output DC-DC converters are desirable for a variety of applications to reduce the number of power supplies, complexity, space and cost than a large number of single output converters. Now a days, a DC-DC converter consisting of two stages is becoming popular as the use of first stage eliminates the second harmonic voltage effect that is reflected at the output because of single phase AC mains input [12]. The first stage converter can be a non-isolated DC-DC converter and the second stage should be an isolated DC-DC converter having multiple outputs. To reduce the complexity, cost and space, only a single output (the most sensitive one) is sensed and regulated by feedback control. Generally, in the front end, a diode bridge is used to convert AC mains voltage to unregulated DC voltage which results in poor power factor (PF). To compensate for this, in the present work, a DC-DC converter is used with power factor correction (PFC) circuit to meet the IEEE and IEC standards [13-14].

II. CONFIGURATION OF BRIDGELESS-CONVERTER-BASED MULTIPLE-OUTPUT SMPS

The system configuration of the proposed multiple-output SMPS is shown in Fig.1. Single-phase ac supply is fed to two buck–boost converters through an inductor–capacitor (Lin–Cin) filter to eliminate the high-frequency ripples. The upper buck–boost converter that conducts during the positive half cycle of the ac supply consists of one high-frequency switch Sp, inductor Lp, and two diodes Dp1 and Dp2. Similarly, the lower buck–boost converter that operates during the negative half cycle consists of one high-frequency switch Sn, inductor Ln, and two diodes Dn1 and Dn2. Both inductors Lp and Ln of buck–boost converters are designed in DCM to obtain inherent PFC at the input ac mains. The input capacitor of the half bridge VSI acts as the filter at the output of the buck–boost converter. The voltage and current stresses on the switches of the buck–boost converters are evaluated to estimate the switch rating and heat sink design. The output dc voltage of the buck–boost converter is regulated by using closed-loop control. The regulated dc output voltage of the buck–boost converter is fed to the half-bridge VSI for obtaining multiple dc voltages. The half-bridge VSI consists of two input capacitors C11 andC12, two high-frequency switches S1 and S2, and one multiple output high-frequency transformer (HFT). The HFT is having one primary winding and four secondary windings which are connected in center-tapped configuration to reduce the losses.

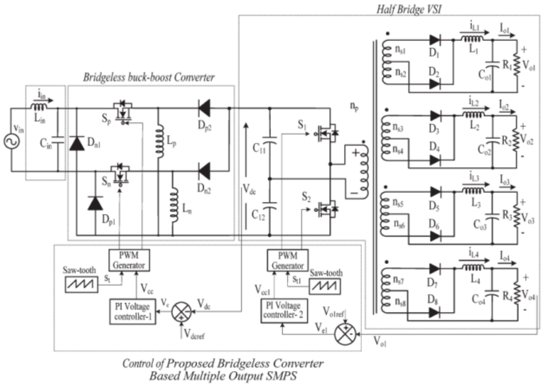


Fig.1. Proposed bridgeless-converter-based multiple-output SMPS.

At the secondary side of the HFT, filter inductors L1, L2, L3,and L4 and capacitors Co1, Co2, Co3, and Co4 are connected to each winding to reduce the current and voltage ripples, respectively. The output voltages are regulated by using closed loop control of one of the output voltages. The highest rated dc voltage is sensed for this purpose. The other three outputs are controlled through duty ratio control of the half-bridge VSI because a common core is used for all other secondary windings of the HFT with proper winding arrangements. The effect of varying input voltages and loads is studied to reveal the improved performance of the proposed bridgeless-converter-based multiple-output SMPS. The hardware of the SMPS is implemented in a laboratory prototype to verify the simulated results.

III. OPERATING PRINCIPLE OF BRIDGELESS-CONVERTER-BASED MULTIPLE-OUTPUT SMPS

The proposed bridgeless-converter-based multiple-output SMPS consists of a single-phase ac supply feeding two back-to-back-connected buck–boost converters with a half-bridge VSI and multiple-output HFT at the load end. The buck–boost converters are controlled suitably to obtain a high PF and low input current THD. The half-bridge VSI at the output takes care of high-frequency isolation with multiple dc output voltages being regulated. The operation of both converters in one switching cycle is described in the following subsections.

A. Operation of Buck–Boost Converter

The switches in the upper and lower buck–boost converters are switched on and off alternately in the positive and negative half cycles of the ac voltage, respectively. The operation of the upper buck–boost converter in DCM during the positive half cycle of the ac input voltage is shown in Fig. 3. The lower one operates in the same way but during the negative half cycle. Three states are observed in DCM operation in each switching cycle. In the first state, when the upper switch Spis on, inductor Lp starts storing energy from the input, and the inductor current increases to the maximum value, as shown in Fig. 2(a). Diode Dp1 completes the current flow path in the input side. In the second state, Sp is turned off, and the energy in inductor Lp is transferred to the output, thus reducing its current from maximum value to zero, as shown in Fig. 2(b). In the last state of one switching cycle, neither the switch and nor the diode conducts, and the inductor current remains zero, ensuring DCM operation [Fig. 2(c)]. Fig. 2(d) shows the waveforms for one complete pulse width modulation (PWM) switching cycle. In the next switching cycle, the same sequence of operation repeats itself. Similarly for negative half cycle of the input voltage, the lower buck–boost converter operates, and the same sequence of operation continues.

B. Operation of Half-Bridge VSI

The controlled output dc voltage of the dual buck–boost converter is fed to the half-bridge VSI for high-frequency isolation, for voltage scaling, and for obtaining multiple dc output voltages. The operation of the half-bridge VSI in one switching cycle is described in four states. The second and

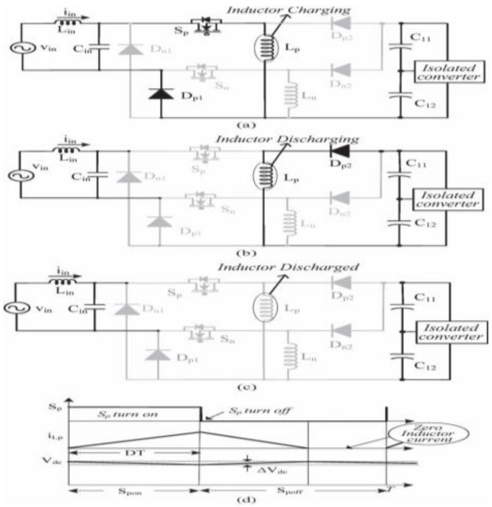


Fig.2. Operating modes for under (a) upper switch Sp is on, (b) upper switch Spis off, (c) both switch and diode are off, and (d) waveforms in one switching cycle.

fourth states are similar and occur twice in each switching cycle, as shown in Fig. 3(b). In the first state, the upper switch S1 is turned on; the input current circulates through the primary winding of the HFT to the lower input capacitor C12. Diodes D1, D3, D5, and D7 start conducting, and the inductors associated with the windings start storing energy, as shown in Fig. 3(a). Therefore, inductor currents iL1, iL2, iL3, and iL4 increase, and output filter capacitors Co1, Co2, Co3, and Co4 discharge through the loads. In the second state [Fig. 3(b)], both switches are turned off, and all secondary diodes D1–D8 freewheel the stored energy until the voltage across the HFT becomes zero. Therefore, inductor currents iL1, iL2, iL3, and iL4 start decreasing. In the third state of the switching cycle,

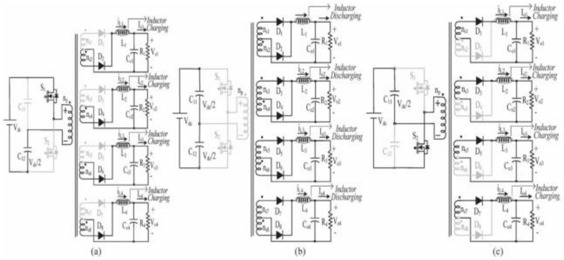


Fig.3. (a) When the first switch S1 is on, (b) when both switches are off, (c) and when the second switch S2 is on.

The second switch S2 is turned on, and the input current flows through upper capacitor C11 and the primary winding, as shown in Fig. 3(c). Associated diodes D2, D4, D6, and D8 in the secondary windings conduct, and inductors L1, L2, L3, and L4 start storing energy. When the energy stored in the inductors reaches maximum values, the switch is turned off. In the last state, all secondary diodes start conducting, which is similar to the second state. The same operating states repeat in each switching cycle.

IV. CONTROL OF PROPOSED BRIDGELESS-CONVERTER-BASED MULTIPLE-OUTPUT SMPS

The control of the SMPS is carried out using two independent controllers. The front-end bridgeless buck–boost converter utilizes the voltage follower approach, while the half-bridge VSI utilizes the average current control.

A. Control of Front-End Converter

The control of the PFC bridgeless converter generates the PWM pulses for both switches (Sp and Sn) according to the polarity of input ac mains voltage. In this technique, voltage error Ve, i.e., the difference between the reference voltage Vdcref and the sensed dc output voltage Vo1, is fed to a proportional–integral (PI) voltage controller, as shown in Fig. 1. The voltage error signal (Ve) is expressed as

$$V_e(n) = V_{\mathrm{dcref}}(n) - V_{\mathrm{dc}}(n)$$

Where n represents the nth sampling instant.

This error voltage signal (Ve) is fed to the voltage PI controller 1 to generate a controlled output voltage (Vcc). It is expressed as

$$V_{cc}(n) = V_{cc}(n-1) + k_p\{V_e(n) - V_e(n-1)\} + k_i V_e(n)$$

Where kp and ki are the proportional and integral gains of the voltage PI controller 1. Finally, the output of the voltage controller 1 is compared with a high-frequency saw tooth signal (St) to generate the PWM pulses

$$\text{For } v_{\mathrm{in}} > 0; \quad \begin{Bmatrix} \text{if } s_t < V_{\mathrm{cc}}, & \text{then } S_p = \text{on} \\ \text{if } s_t \geq V_{\mathrm{cc}}, & \text{then } S_p = \text{off} \end{Bmatrix}$$

$$\text{For } v_{\mathrm{in}} < 0; \quad \begin{Bmatrix} \text{if } s_t < V_{\mathrm{cc}}, & \text{then } S_n = \text{on} \\ \text{if } s_t \geq V_{\mathrm{cc}}, & \text{then } S_n = \text{off} \end{Bmatrix}$$

Where Sp and Sn represent the switching signals of PFC bridgeless buck–boost converter.

B. Control of Half-Bridge VSI

For controlling the output voltage of the half-bridge VSI, an average current control scheme is used. The highest ratedwinding output voltage Vo1 is sensed and compared with a constant reference value Vo1ref. The voltage error signal (Ve1) is fed to PI controller 2, and its output is compared with the saw tooth signal to generate PWM switching signals to maintain the output voltage constant. Thus, the control is able to take care of the impact of any individual output on the overall variationin the duty ratio and also the contribution of the present loadcondition of any of the outputs to the variations in Vo1, Vo2, Vo3, and Vo4. If the load on any of the other windings is varied, the duty cycle undergoes a change according to the impact felt on the highest rated output, and hence, voltage regulation is taken care of. However, the response of the other windings is slightly slower as compared to the winding whose output is sensed. Switches S1 and S2 are switched on and off alternately in each half cycle of one PWM period with sufficient dead time to avoid shoot-through.

V.FUZZY LOGIC CONTROL

L. A. Zadeh presented the first paper on fuzzy set theory in 1965. Since then, a new language was developed to describe the fuzzy properties of reality, which are very difficult and sometime even impossible to be described using conventional methods. Fuzzy set theory has been widely used in the control area with some application to power system [5]. A simple fuzzy logic control is built up by a group of rules based on the human knowledge of system behavior. Matlab/Simulink simulation model is built to study the dynamic behavior of converter. Furthermore, design of fuzzy logic controller can provide desirable both small signal and large signal dynamic performance at same time, which is not possible with linear control technique. Thus, fuzzy logic controller has been potential ability to improve the robustness of compensator.

The basic scheme of a fuzzy logic controller is shown in Fig .4. and consists of four principal components such as: a fuzzy fication interface, which converts input data into suitable linguistic values; a knowledge base, which consists of a data base with the necessary linguistic definitions and the control rule set; a decision-making logic which, simulating a human decision process, infer the fuzzy control action from the knowledge of the control rules and linguistic variable definitions; a de-fuzzification interface which yields non fuzzy control action from an inferred fuzzy control action [10].

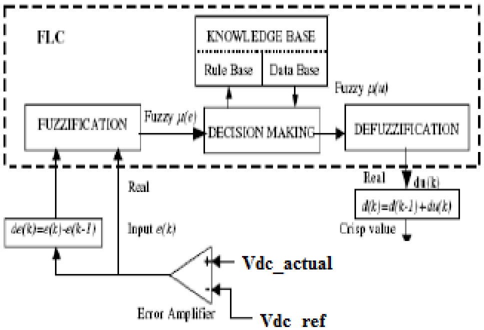


Fig.4.Block diagram of the Fuzzy Logic Controller (FLC) for Proposed Converter.

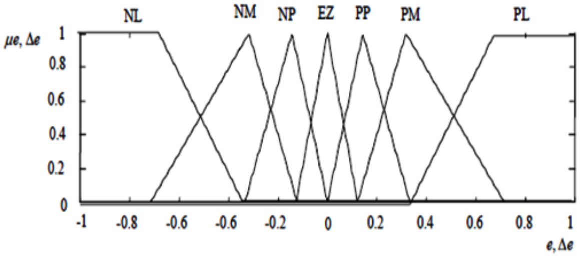


Fig.5. Membership functions for Input, Change in input, Output.

Rule Base:the elements of this rule base table are determined based on the theory that in the transient state, large errors need coarse control, which requires coarse in-put/output variables; in the steady state, small errors need fine control, which requires fine input/output variables. Based on this the elements of the rule table are obtained as shown in Table, with 'Vdc' and 'Vdc-ref' as inputs

e Δe	NL	NM	NS	EZ	PS	PM	PL
NL	NL	NL	NL	NL	NM	NS	EZ
NM	NL	NL	NL	NM	NS	EZ	PS
NS	NL	NL	NM	NS	EZ	PS	PM
EZ	NL	NM	NS	EZ	PS	PM	PL
PS	NM	NS	EZ	PS	PM	PL	PL
PM	NS	EZ	PS	PM	PL	PL	PL
PL	NL	NM	NS	EZ	PS	PM	PL

VI.MATLAB/SIMULATION RESULTS

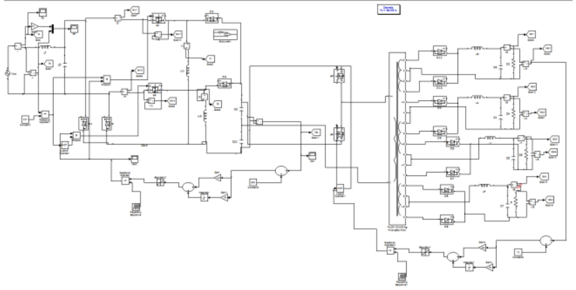


Fig 6 Matlab/simulation of bridgeless-converter-based multiple-output SMPS

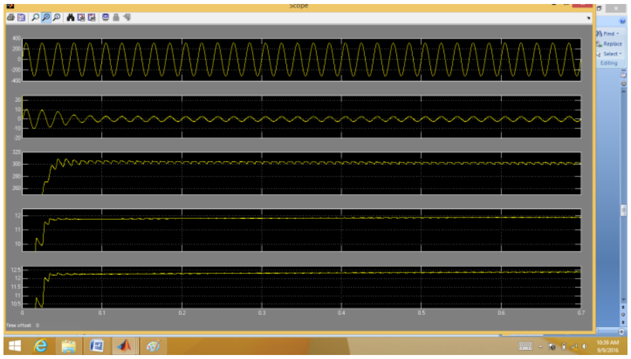


Fig 7 simulation wave form of Input voltage, current, buck–boost converter output voltage, half bridge VSI output voltages, and currents.

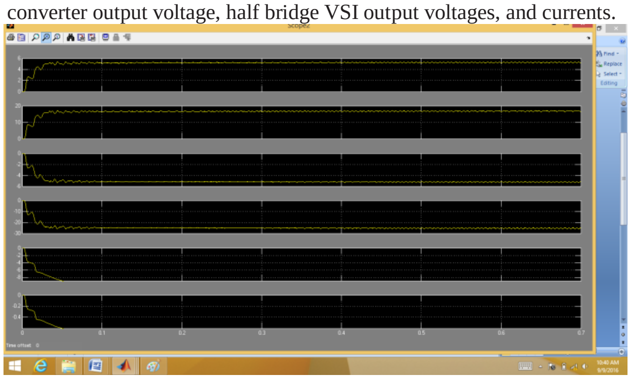


Fig 8 simulation wave form of half-bridge VSI output voltages, and currents at load variation in 12 and 5V outputs.

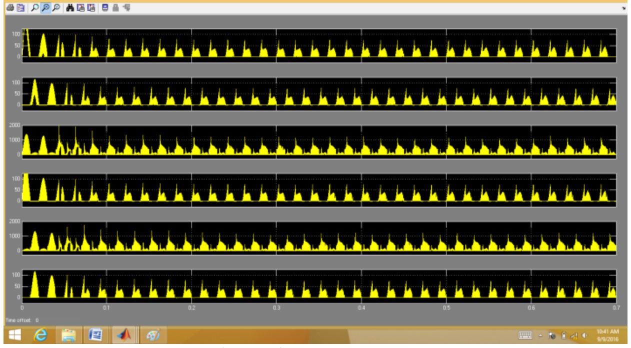


Fig 9 simulation waveform of inductor current, switch voltage and current of Buck-Boost converter.

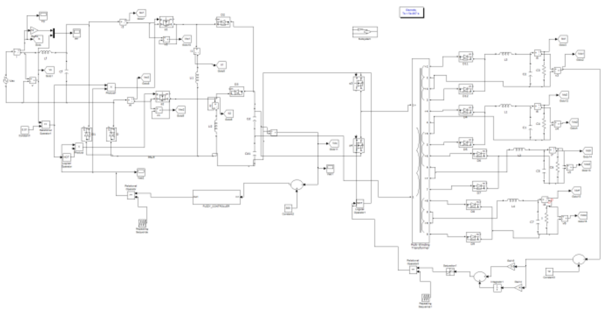


Fig 10 Matlab/simulation proposed method of bridgeless-converter-based multiple-output SMPS using Fuzzy logic.

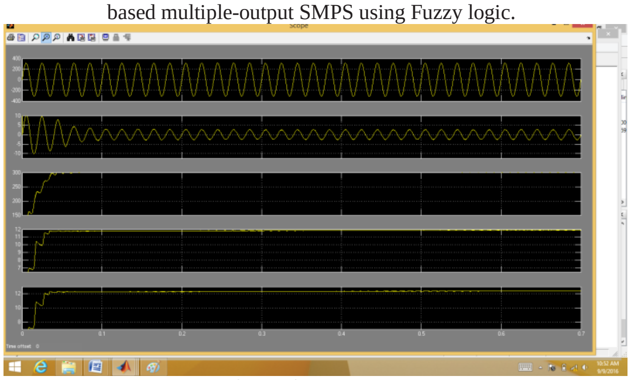


Fig 11 simulation wave form of Input voltage, current, buck–boost converter output voltage, half bridge VSI output voltages, and currents.

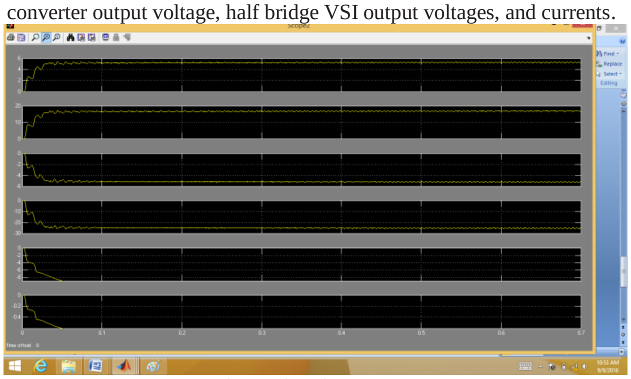


Fig 12 simulation wave form of half-bridge VSI output voltages, and currents at load variation in 12 and 5V outputs.

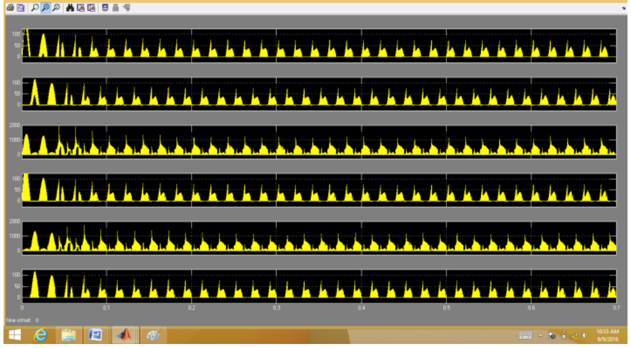
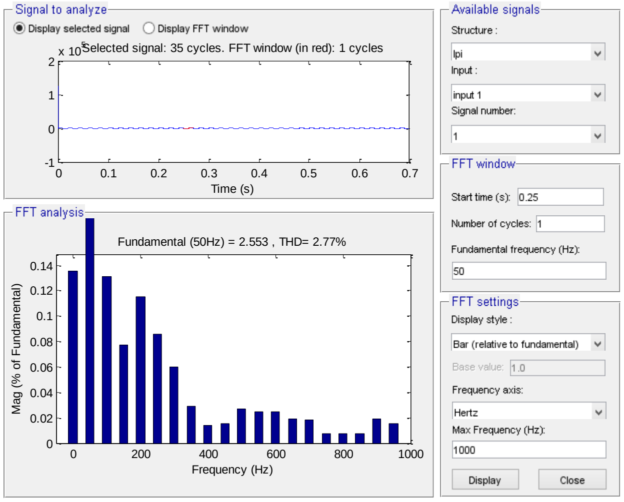


Fig 13 simulation waveform of inductor current, switch voltage and current of Buck-Boost converter.



● Display selected signal ○ Display FFT window

Selected signal: 35 cycles. FFT window (in red): 1 cycles

Fundamental (50Hz) = 2.553 , THD= 2.77%

Structure : lpi

Input : input 1

Signal number: 1

Start time (s): 0.25

Number of cycles: 1

Fundamental frequency (Hz): 50

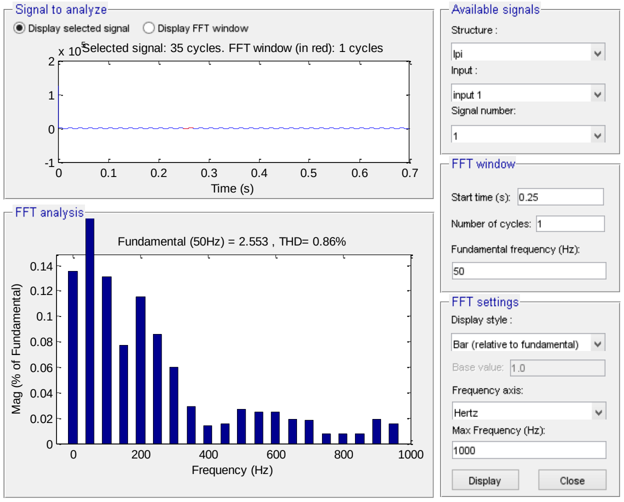
Display style : Bar (relative to fundamental)

Base value: 1.0

Frequency axis: Hertz

Max Frequency (Hz): 1000

Fig 14 Chart for THD value for bridgeless-converter-based multiple-output SMPS



● Display selected signal ○ Display FFT window

Selected signal: 35 cycles. FFT window (in red): 1 cycles

Fundamental (50Hz) = 2.553 , THD= 0.86%

Structure : lpi

Input : input 1

Signal number: 1

Start time (s): 0.25

Number of cycles: 1

Fundamental frequency (Hz): 50

Display style : Bar (relative to fundamental)

Base value: 1.0

Frequency axis: Hertz

Max Frequency (Hz): 1000

Fig 14 Chart for THD value for bridgeless-converter-based multiple-output SMPS using Fuzzy logic.

VII.CONCLUSIONS

A bridgeless-converter-based multiple-output SMPS has been designed, modeled, simulated, to demonstrate its capability to improve the power quality at the utility interface. The output dc voltage of the first-stage buck–boost converter has been maintained constant, independent of the changes in the input voltage and the load, and it is operated in DCM to achieve inherent PFC at the single-phase ac mains. In this paper, the Bridgeless buck-boost Topology for power factor correction has been simulated with PI and Fuzzy controller and results were presented. This converter topology uses reduced number of power switches compared to conventional buck-boost PFC converter and operates under DCM operation to produce less current ripple, thereby improving the power factor. When comparing the PI controller with fuzzy controller, Fuzzy controller improves power factor nearer to unity. The measured power factor using fuzzy controller shows 2% improvement in comparison to the PI controller. The MATLAB/SIMULINK software model has been used to validate the proposed work for power factor improvement.

REFERENCES

[1].Shikha Singh, Student Member, IEEE, Bhim Singh, Fellow, IEEE, G. Bhuvaneswari, Senior Member, IEEE, VashistBist, Student Member, IEEE, Ambrish Chandra, Fellow, IEEE, and Kamal Al-Haddad, Fellow, IEEE"Improved-Power-Quality Bridgeless-Converter-Based Multiple-Output SMPS"IEEE Transactions On Industry Applications, Vol. 51, No. 1, January/February 2015.

[2] W. Hart, Power Electronics. New York, NY, USA: McGraw-Hill, 2011.

[3] N. Mohan, T. M. Undeland, and W. P. Robbins, Power Electronics: Converters, Applications and Design. Hoboken, NJ, USA: Wiley, 2003.

[4] P. J. Moore and I. E. Portugues, "The influence of personal computer processing modes on line current harmonics," IEEE Trans. Power Del., vol. 18, no. 4, pp. 1363–1368, Oct. 2003.

[5] Limits for Harmonic Current Emissions (Equipment Input Current ≤ 16 A per Phase), Int. Standard IEC 61000-3-2, 2000.

[6] B. Singh et al., "A review of single-phase improved power quality AC–DC converters," IEEE Trans. Ind. Electron., vol. 50, no. 5, pp. 962–981, Oct. 2003.

[7] Singh, S. Singh, A. Chandra, and K. Al-Haddad, "Comprehensive study of single-phase AC–DC power factor corrected converters with highfrequency isolation," IEEE Trans. Ind. Informat., vol. 7, no. 4, pp. 540– 556, Nov. 2011.

[8] A. Canesin and I. Barbi, "A unity power factor multiple isolated outputs switching mode power supply using a single switch," in Proc. IEEE APEC, Mar. 1991, pp. 430–436.

[9] K. Matsui et al., "A comparison of various buck–boost converters and their application to PFC," in Proc. 28th IEEE IECON, 2002, vol. 1, pp. 30–36.

[10] E. H. Ismail, "Bridgeless SEPIC rectifier with unity power factor and reduced conduction losses," IEEE Trans. Ind. Electron., vol. 56, no. 4, pp. 1147–1157, Apr. 2009.

[11] A. A. Fardoun, E. H. Ismail, A. J. Sabzali, and M. A. Al-Saffar, "New efficient bridgeless Cuk rectifiers for PFC applications," IEEE Trans. Power Electron., vol. 27, no. 7, pp. 3292–3301, Jul. 2012.

[12] M. Mahdavi and H. Farzaneh-Fard, "Bridgeless Cuk power factor correction rectifier with reduced conduction losses," IET Power Electron., vol. 5, no. 9, pp. 1733–1740, Sep. 2012.

[13] Y. Jang and M. M. Jovanovic, "Bridgeless high-power-factor buck converter," IEEE Trans. Power Electron., vol. 26, no. 2, pp. 602–611, Feb. 2011.

[14] L. Huber, Y. Jang, and M. M. Jovanovic, "Performance evaluation of bridgeless PFC boost rectifiers," IEEE Trans. Power Electron., vol. 23, no. 3, pp. 1381–1390, May 2008.