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DESIGN AN AGING-AWARE RELIABLE H- MULTIPLIER

VEMULA PRIYANKA, M.Tech.,VLSI, E.C.E Dept.,CMR INSTITUTE OF TECHNOLOGY,

Mr.L.SUNEEL, Assistant Professor, E.C.E Dept.,CMR INSTITUTE OF TECHNOLOGY,

Mrs.C.SANTHI,Assistant Professor, E.C.E Dept, CMR INSTITUTE OF TECHNOLOGY.

ABSTRACT: This paper presents the design anH-Logic[H.L] multiplierfor 32*32bit number multiplication. Modern computer system is a dedicated with very high speed unique multiplier. Therefore, this paper presents the design anH-Logic multiplier. The proposed system generates M,N and X blocks. By extending bit of the operands and generating an additional product the H-Logic multiplier is obtained. Multiplication operation is performed by the H-Logicis efficient with the less area anditgives the reduces delay i.e., speed is increased.

Keywords: H.L, partial products, H- level logic unit.

INTRODUCTION

Multiplication is a basic fundamental operation in most signal processing algorithms. Multipliers have large area, long latency and consume operating considerable power. Therefore low-power multiplier design has been an important part in low-power VLSI system design. We have extensive work on low-power multipliers at technology, physical, circuit and logic levels. A system's performance is generally depends on the basically performance of the multiplier because the multiplier is generally the slowest element in any system.

LITERATURE SURVEY

Multiplication operation has been paid most attention by researchers, because addition is simply bitwiseXOR operation between two field elements, and the morecomplex operations, inversion, can be carried out with afew multiplications.

In [21], an LSD-first multiplier with lower area-time complexityhas been proposed using a new method for theaccumulation in which XOR gates and D flip-flops (FFs)have been replaced by T FFs and feedback loops have beeneliminated. In [30], a multiple-bit serial-parallel multiplier hasbeen proposed. One operand is decomposed recursively and the other operand is prereduced hierarchically. The multiplierhas higher area complexity compared with some of the existingmultipliers; however, it has lower critical path delay, whichresults in lower area-time complexity.

A low-complexity digit-serial SPB multiplier using the proposed(b, 2)-way Karatsuba decomposition has been proposed. The (4, 2)-way and (6, 2)-way Karatsuba-based digitserialmultipliers have been implemented and compared withthe existing SPB multiplier. The Karatsuba-based digit-serial

SPB multiplier shows lower area complexity, less area-delayproduct, and less

energy consumption compared with theexisting SPB multiplier.

PROPOSED TECHNIQUE

In this paper, a H- technique is adopted in designof a digit-serial PB multiplier. To the best ofour knowledge, a factoring method has not been reportedin the literature being used in the design of a finite fieldmultiplier at an architectural level. A logic gate substitutiontechnique is also used in our design to reduce the internalpower consumption of the proposed H- multiplier. The synthesis results show that our new design has boththe lowest area consumption and the less memory used consumption among several similar existing works.

A column-bypassing multiplier is an improvement on thenormal array multiplier (AM). The multiplier array consists of $(n-1)$rows of carry save adder (CSA), in which each and every row contains$(n-1)$ full adder (FA) cells. Each FA in the CSA array hastwo outputs: 1) the sum bit goes down and 2) the carry bitgoes to the lower left FA. The last row is a ripple adder forcarry propagation.

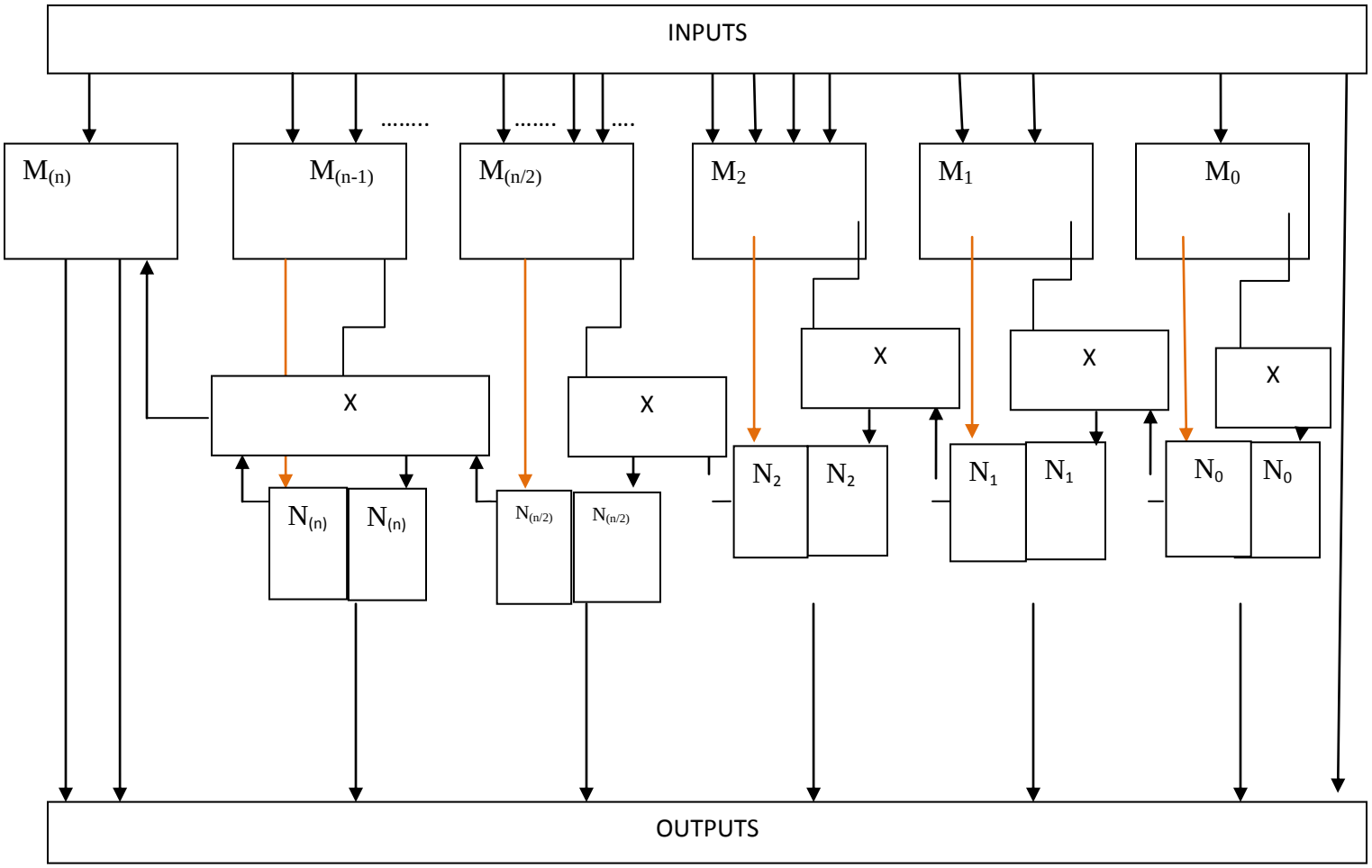

Fig. 1 4 x 4 HIGH PERFORMANCE H-LOGIC MULTIPLIER

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PROPOSED SYSTEM:

The gates in the H-Logic[H.L] multiplier are always active regard of input logics. In,H-Logic[H.L] multiplier design is proposed in which the operations are disabled if the corresponding bit in the multiplicand is 0. Fig. 1 shows a N×NH-Logic[H.L] multiplier, it can be seen that the M0,M1,…Mn done their operations and the outputs are passed to interconnected

To evaluate the complexities of H-MUL arithmetic hardware,circuit complexity is usually presented by the numberof FFs, two-input ANDgates, two-input XORgates, and MUXs. In estimation of critical path delay is used to refer to as the delaycaused by a two-input AND gate, a two-input or gate,a two-input XOR gate, a 2-to-1 multiplexer, a D FF, and aT FF, respectively.

Block and N-Block simultaneously. Depends on the preference of operation the H- level logic gives the N-block output to interconnected block and vice versa.

Therefore, the output of the adders in both diagonals is 0, and the outputsum bit is simply equal to the third bit.The above fig. 1 shows the 4*4 high performance H-Logic multiplierreduced the timing waste occurring in traditionalcircuits that use the critical path cycle of an execution cycleperiod. The basic concept is to execute a shorter path using H- logic. Since mostpaths execute in a cycle period that is very smaller thanthe critical path delay. The same architecture is extended up to 32*32 bits.

H-Logicwidely been adopted in multipliers since it can reduce the number of partial product rows to be added, thus reducing the size and enhancing the speed of the reduction tree. The least significant bit position of each partial product is rowencoding, leading to an irregular partial product array and a complex reduction tree. Therefore, the H-Logicmultipliers with partial product array produce a very highspeed.

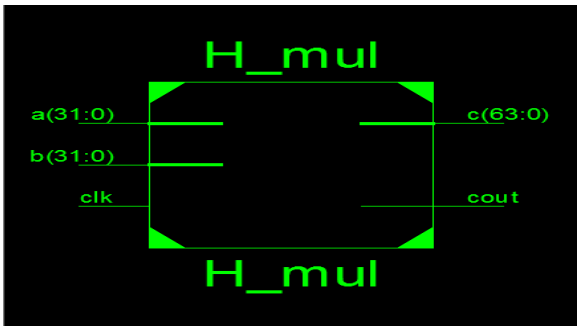


Fig. 2 R.T.L Schematic

The above fig. 2 shows the R.T.L schematic of high performance H-Logic multiplier and fig. 3 shows the technical schematic one of theLUT block of high performance H-Logic multiplier.

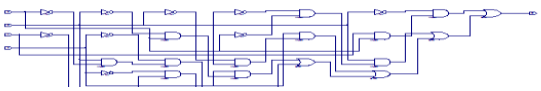
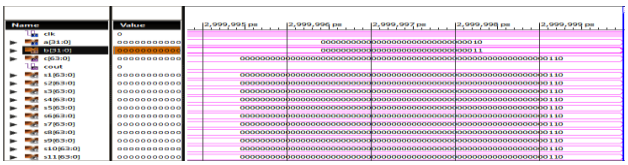


Fig. 3 LUT in technical Schematic

The below figure 4 shows the output waveform of 32*32 bit H-Logic multiplier.



The below table 1 shows the comparison of existed system and proposed system with area and delay

Fig. 4 OUTPUT Waveforms

System/parameter	Area[kb]	Delay[ns]
Existed System	382256	410
Proposed system	366700	102.80

Table.1 comparison table

The above comparison table shows that area of the proposed system is less compare with the existed system and delay is also efficient.

CONCLUSION

The H - technique has been adopted for a new architecturelevel design that minimizes the switching activities and consequently, reduces the power consumption of a digit-serialmultiplier. The logic gate substitution techniquehas also been utilized to further reduce the power consumptionof the digit-serial H-multiplier. Moreover, the area complexityof the finite field multiplier has been reduced.

REFERENCES

[1] R. Vattikonda, W. Wang, and Y. Cao, "Modeling and miimization ofpMOS NBTI effect for robust naometer design," in *Proc. ACM/IEEEDAC*, Jun. 2004, pp. 1047–1052.

[2] H. Abrishami, S. Hatami, B. Amelifard, and M. Pedram, "NBTI-awareflip-flop characterization and design," in *Proc. 44th ACM GLSVLSI*,2008, pp. 29–34

[3] S. V. Kumar, C. H. Kim, and S. S. Sapatnekar, "NBTI-aware synthesisof digital circuits," in *Proc. ACM/IEEE DAC*, Jun. 2007, pp. 370–375.

[4] A. Calimera, E. Macii, and M. Poncino, "Design techniqures for NBTItolerantpower-gating architecture," *IEEE Trans. Circuits Syst., Exp.Briefs*, vol. 59, no. 4, pp. 249–253, Apr. 2012.

[5] K.-C. Wu and D. Marculescu, "Joint logic restructuring and pin reorderingagainst NBTI-induced performance degradation," in *Proc. DATE*,2009, pp. 75–80.

[6] Y. Lee and T. Kim, "A fine-grained technique of NBTI-aware voltagescaling and body biasing for standard cell based designs," in *Proc. ASPDAC*,2011, pp. 603–608.

[7] M. Basoglu, M. Orshansky, and M. Erez, "NBTI-aware DVFS: A newapproach to saving energy and increasing processor lifetime," in *Proc.ACM/IEEE ISLPED*, Aug. 2010, pp. 253–258.

[8] K.-C. Wu and D. Marculescu, "Aging-aware timing analysis and optimizationconsidering path sensitization," in *Proc. DATE*, 2011, pp. 1–6.

[9] K. Du, P. Varman, and K. Mohanram, "High performance reliablevariable latency carry select addition," in *Proc. DATE*, 2012, pp. 1257–1262.

[10] A. K. Verma, P. Brisk, and P. Ienne, "Variable latency speculativeaddition: A new paradigm for arithmetic circuit design," in *Proc. DATE*,2008, pp. 1250–1255.