

Implementation of A High-Frequency Link Five and Eleven level Cascaded Converter with PWM Controller

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Abstract—Power Electronic converters, especially DC/AC Sinusoidal Pulse Width Modulation inverters have been extending their range of use in industry because of their numerous advantage. Recent advances in solid-state semiconductors have led to the development of medium-voltage power converters which could obviate the need for the step-up transformers of renewable power generation systems. The modular multilevel cascaded converters have been deemed as strong contenders for the development of medium-voltage converters, but the converters require multiple isolated and balanced dc supplies. This paper proposes the high-frequency link multilevel cascaded medium-voltage converter. The common high-frequency link generates multiple isolated and balanced dc supplies for the converter, which inherently minimizes the voltage imbalance and common mode issues. A multilevel phase shifted carrier based sinusoidal PWM switching scheme is utilized to reduce the complexity in control design. Therefore an identical H-bridge module is used to improve manufacturability and modularity. When comparing the five and eleven level inverter the voltage levels are increasing the THD value is decreases. The experimental results are analyzed and discussed. It is expected that the proposed new technology will have great potential for future renewable generation systems and smart grid applications.

Index Terms—Direct grid integration, high-frequency link, medium-voltage converters, modular multilevel cascaded (MMC) converters.

I. INTRODUCTION

Power Electronics is the art of converting electrical energy from one form to another in an efficient, clean, compact, and robust manner for convenient utilization. It has found an important place in modern technology being core of power and energy control. It is the technology associated with efficient conversion, control and conditioning of electric power from its available input into the desired output form. Power electronics and converters utilizing them made a head start when the first device the Silicon Controlled Rectifier was proposed by Bell Labs and commercially produced by General Electric in the earlier fifties. The simplest dc voltage source for a VSI may be a battery bank, which may consist of several cells in series-parallel combination. Solar photovoltaic cells can be

another dc voltage source. A voltage source is called stiff, if the source voltage magnitude does not depend on load connected to it. All voltage source inverters assume stiff voltage supply at the input. The first topology introduced was the series H-bridge design. This was followed by the diode-clamped converter which utilized a bank of series capacitors. A later invention detailed the flying capacitor design in which the capacitors were floating rather than series-connected. Another multilevel design involves parallel connection of inverter phases through inter-phase reactors. Several combinational designs have also emerged some involving cascading the fundamental topologies.

A Three phase five and eleven level Cascaded H-Bridge Inverter Using Low frequency transformer with Single DC Source is presented which overcomes the disadvantage of conventional MMC by employing low frequency transformers with single DC source. Using this proposed model number of DC sources are reduced thus decreasing the complexity and cost of the design. Also a low frequency transformer provides galvanic isolation and is used to obtain the required output voltage level with reduced harmonic components. Relay angles of the converter is obtained based on linearization method and this approach is useful in elimination of lower order harmonics.

II. Proposed Medium-Voltage Converter-Based Direct Grid Integration Systems

A. Basic Block Diagram of the Proposed Systems

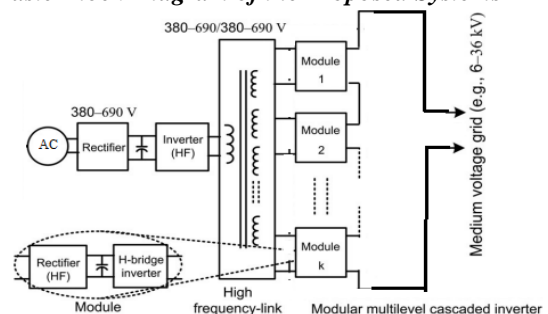


Fig. 1. Proposed single-phase five level inverter connected to grid.

For high-power applications, a number of medium/high frequency full-bridge inverters can be used in parallel. The parallel operation of multiple medium/high-frequency inverters enables the proposed technology to use mature low-rated power and low-cost semiconductor devices. To ensure a fixed grid voltage, a constant output voltage of the inverter is maintained.

The inverter output is supplied to the primary windings of a common multi winding medium/high-frequency link. Each secondary winding is connected with the H-bridge inverter through a bridge rectifier. The number of primary windings depends on the number of sources and the number of secondary windings depends on the number of levels of the MMC converter. The grid electrical isolation and voltage imbalance problems are solved inherently through the common medium/high-frequency link. A field-programmable gate array (FPGA)-based control circuit is used to control the magnitude and phase angle, and to ensure the power quality and stability of the system. In this paper, the phase-shifted carrier and third harmonic injected sinusoidal reference-based pulse width modulation (PWM) scheme is used. Desired output voltage level can be generated by cascading more modules on each phase. A high-level converter results in the elimination of the step-up transformer and lower total harmonic distortion (THD) with lower switching frequency. It also leads to the elimination of the output filters and a reduction in running cost. A high-level number attainability also allows for a lower level dc-link voltage requirement for each H-bridge inverter that serves to eliminate the boosters.

B. Design and Analysis of an 11-kV MMC Converter

If m_l is the number of levels of the converter, the number of cascaded modules on each phase can be calculated from

$$M_n = \frac{(m_l - 1)}{2} \tag{1}$$

If $V_{ll(rms)}$ is the grid line to line voltage, the minimum dc-link voltage of each H-bridge inverter cell can be calculated from

$$V_{dc(min)} = \sqrt{2} \frac{V_{ll(rms)}}{(m_l - 1)} \tag{2}$$

To determine the nominal dc-link voltage of each H-bridge inverter cell, a voltage reserve of 4% is assumed, i.e.,

$$V_{dc(nom)} = 1.04V_{dc(min)} \tag{3}$$

If $I_{p(rms)}$ is the inverter phase current, the apparent output power can be calculated from

$$S_c = \sqrt{3}V_{ll(rms)}I_{p(rms)} \tag{4}$$

The highest voltage rating of the commercially available IGBT is 6.5 kV and this is suitable for 2.54 kV or lower voltage converter systems with the traditional two-level converter topology.

The high-number of levels means that medium-voltage attainability is possible so that the renewable generation system can be connected to the medium-voltage ac network directly. It is also possible to improve the output power quality. The component number and control complexity increase linearly with the increase in the number of levels. Therefore, the optimal selection of the number of converter levels is important in order to achieve the best performance/cost ratio for the system. Table.1 summarizes the converter specifications used for the design and simulation of an 11-kV system.

TABLE I

Converter specifications in the simulation

Line voltage (kV)	11
Line current (A)	250
Apparent power (MVA)	4.76
Carrier frequency (kHz)	1–2
Output frequency (Hz)	50
Number of levels	7–21
Number of phases	3
Carrier shifting	Phase shifted

TABLE II

Selection of IGBTs for MMC converters

Level number	V_{com} (V)	Rated device voltage (kV)	$V_{com@100FIT}$ (V)	DVUF (%)
7	2696	6.5	3600	75
9	2022	4.5	2250	90
11	1618	3.3	1800	90
13	1348	3.3	1800	75
15	1156	2.5	1200	96
17	1011	2.5	1200	84
19	898	1.7	900	99
21	809	1.7	900	90

Each module dc-link voltage of a seven-level topology-based 11-kV converter is 2696 V which may be supported by the 6.5-kV IGBT. Thus, at least seven-level topology is required to design an 11-kV converter. The output power quality of a 21-level converter is good enough to feed into the 11-kV ac grid directly. The cheap 1.7-kV IGBT can be used to design the 21-level inverter. Therefore, 7-level to 21-level MMC converter topologies are considered for 11-kV systems. The device voltage utilization factor (DVUF), ratio of commutation voltage of respective commutation cells V_{com} and device commutation voltage for a device reliability of 100 failures in time (FIT) due to cosmic radiation ($V_{com@100FIT}$), is summarized in Table II. Higher DVUF is essential for cost-effective design, since semiconductor cost is the significant figure in medium-voltage converter applications. From Table II, it can be seen that only a few converters have high DVUF. In order

to ensure a cost effective design, the converters with level numbers of 9, 11, 15, 19 and 21 for an 11-kV system have been considered for further analysis. The number of arithmetic and logic operations (ALOs) for the switching section and cost of semiconductors are calculated and summarized in Table III. The number of ALOs is used to compare the complexity of the converters. The THD is calculated through the MATLAB/Simulink environment. Fig.8 shows the output voltage waveforms of the converters with level numbers of 5 and 11 their frequency spectrums are shown in Fig.9.

C. Modulation Scheme for MMC Converters

Different types of major reference signals used in the traditional converters can also be employed in the multilevel converter system (e.g., sinusoidal, third harmonic injected sinusoidal, 60° modulated sinusoidal and trapezoidal). Each has unique advantages and disadvantages. It is possible to reduce the switching losses by reducing the number of switching occurrences in each period. Flattening the top of the reference signal waveforms (e.g., third harmonic injected sinusoidal, 60° modulated sinusoidal and trapezoidal) not only allows the possibility of switching loss reduction but also increases the range of linear modulation. In this paper, four modulation schemes (e.g., the phase-shifted carriers with sinusoidal references (SPWM), the phase-shifted carriers with third harmonic injected sinusoidal references (THPWM), the phase-shifted carriers with 60° modulated sinusoidal references (SDPWM), and the phase shifted carriers with trapezoidal type references (TRPWM)) are applied on 7-level to 19-level MMC converter systems to analyze the performance. Of these four modulation schemes, the THPWM scheme gives the best harmonic performance. The SDPWM and TRPWM schemes have higher lower order harmonic contents than that of the SPWM and THPWM schemes. In addition, the SPWM has shown a higher reduction rate for the high level number.

III. DESIGN OF MEDIUM/HIGH FREQUENCY LINK

At the beginning, according to the power converter rating, the transformer-link specifications, such as rated power, frequency, excitation current, and voltage, are calculated. The core material is selected according to the availability, system requirements, and cost. From the specifications of the transformer-link and data sheets of core materials, the transformer-link initial parameters are calculated. These parameters are used as initial values of the optimization process. The volume and weight of the transformer need to be optimized by selecting proper parameters. The winding dimensions depend on the diameter and number of the conductors, and winding structure. Single layer winding provides low ac/dc resistance ratios, but it increases the winding and core dimension significantly. For simplicity of the winding process, a toroidal structure core is considered. Different factors are also considered

during the selection of core dimensions, such as the winding dimensions, toroid hole reserve for natural cooling, maximum temperature limits, maximum power loss, availability of core material stripe dimensions, leakage inductance, and the possibility to induce an equal voltage in multiple secondary windings. Therefore, the design process involves multi physics problems with some critical decision-making tasks.

TABLE IV

Coefficients of specific core loss of metglas alloy 2605 sa1

Excitation voltage type	Coefficients		
	k'	m'	n'
Sinusoidal (from datasheet)	6.50	1.51	1.74
Square (from curve-fitting)	6.2567	1.5800	1.6195

A. Core Material Selection

With the advent of new power semiconductor devices, different soft magnetic materials are conceived with a high magnetic saturation and low power loss to reduce the weight and volume of conventional power transformers. The grain-oriented silicon sheet steels, which are commonly used as the core material for power-frequency transformers, are not suitable for medium/high-frequency applications because of the heavy eddy current loss. The soft ferrites have been widely used in medium- and high-frequency inductors and transformers due to their low price and general availability. Because of the low saturation flux density (only 0.3–0.5 T), which results in the transformer's large size, they are not suitable for large power applications.

On the other hand, the amorphous alloy and nano crystalline materials have excellent magnetic characteristics for medium/high-frequency applications, such as high permeability, high saturation flux density, and relatively low core losses. The nano crystalline alloy Vitroperm 55Z has a lower specific core loss than that of Vitroperm 500F. Of the other amorphous alloys, 2605SA1 and 2605S3A, the alloy 2714A has the lowest specific core loss but its saturation flux density is only 0.57 T. Although nano crystalline alloy has a lower specific core loss than the amorphous alloys, its saturation flux density (about 1 T) is much lower than that of the amorphous alloys 2605S3A and 2605SA1, which are 1.41 and 1.56 T, respectively. The Metglas alloys 2605SA1 and 2605S3A are iron-based material with specific core losses of about 20 and 7 W/kg, respectively, at 10 kHz sinusoidal excitation of 0.3 T, and these are manufactured by Hitachi Metals, Japan. Taking into account the flux density, specific core loss, cost, and availability, the Metglas alloys 2605S3A and 2605SA1 stripe of 20μm thickness and 25 mm width have been chosen as the core material.

The coefficients (k^1 , m^1 , and n^1) of Steinmetz (6) from the datasheet for the Metglas alloy 2605SA1 are

experimental results under sinusoidal voltage excitation, where f is the frequency in kilohertz and B the magnitude of flux density in tesla. For this design, new coefficients are calculated by measurements under square wave voltage excitation.

$$P_{\text{core}} = k' f^{m'} B^{n'} \quad (5)$$

B. Calculation of Number of Turns

The medium/high-frequency link works with a square wave voltage; thus, according to Faraday's law, a triangular flux is required to generate the square wave voltage as shown in Fig.2, where T is the period of excitation voltage, V_{max} the maximum excitation voltage, and ϕ_{max} the maximum flux.

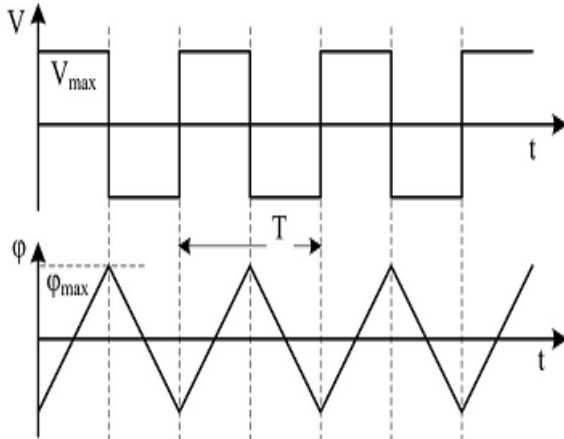


Fig.2. Voltage and flux in a square wave medium/high-frequency link. The triangular flux can be modeled mathematically as

$$\varphi(t) = \begin{cases} \frac{\varphi_{\text{max}}}{T/4} \left(t - \frac{T}{4} \right) & \dots\dots\dots 0 \leq t \leq \frac{T}{2} \\ -\frac{\varphi_{\text{max}}}{T/4} \left(t - \frac{3T}{4} \right) & \dots\dots\dots \frac{T}{2} \leq t \leq T \end{cases} \quad (6)$$

If N is the number of turns, the expression of the voltage can be deduced by Faraday's law and (6) as

$$v(t) = \begin{cases} N \frac{\varphi_{\text{max}}}{T/4} & \dots\dots\dots 0 \leq t \leq \frac{T}{2} \\ -N \frac{\varphi_{\text{max}}}{T/4} & \dots\dots\dots \frac{T}{2} \leq t \leq T \end{cases} = \begin{cases} V_{\text{max}} & \dots\dots\dots 0 \leq t \leq \frac{T}{2} \\ -V_{\text{max}} & \dots\dots\dots \frac{T}{2} \leq t \leq T \end{cases} \quad (7)$$

Where

$$V_{\text{max}} = N \frac{\varphi_{\text{max}}}{T/4} \quad (8)$$

Expression (7) is the mathematical model of the excitation voltage waveform, as shown in Fig.2. The rms value of excitation voltage can be calculated as

TABLE V

Specifications of 1.73KVA high-frequency links

Core material (Metglas alloys)	2605S3A and 2605SA1
Core type	Toroidal
Core size (cm ²)	5
Power rating (kVA)	1.73
Voltage rating (V)	210/374
Rated frequency (kHz)	10
Number of turns	14/25
Number of primary	1
Number of secondary	6
Number of strand of Litz wire	13/3
Single strand diameter (mm)	0.4 (both sides)

$$V_{\text{rms}} = \sqrt{\frac{1}{T} \left\{ V_{\text{max}}^2 \left(\frac{T}{2} \right) + (-V_{\text{max}})^2 \frac{T}{2} \right\}}$$

$$V_{\text{rms}} = \sqrt{\frac{2}{T} \left\{ V_{\text{max}}^2 \left(\frac{T}{2} \right) \right\}} = V_{\text{max}} \quad (9)$$

If f is the frequency of the excitation voltage, B_{max} is the maximum flux density, and A is the cross-sectional area of the core, then from (8) and (9) the expression of the number of turns can be deduced as

$$V_{\text{rms}} = V_{\text{max}} = N \frac{\varphi_{\text{max}}}{T/4} = 4fN\varphi_{\text{max}} = 4fNAB_{\text{max}}$$

$$N = \frac{V_{\text{rms}}}{4fAB_{\text{max}}} \quad (10)$$

Table V summarizes the specifications of 1.73 kVA high frequency links.

C. Winding Wire Selection

The skin and proximity effects increase the ac resistances in high-frequency windings. In a conductor, the ac/dc resistance ratios, K_r depends strongly on both the number of layers m and the conductor diameter d . The ac resistance of the m^{th} layer for solid round wires can be represented as follows:

$$K_r = \frac{R_{\text{ac}}}{R_{\text{dc}}} = \frac{\xi}{2} [M(\xi) + (2m - 1)^2 D(\xi)] \quad (11)$$

Where

$$\xi = \frac{0.886d}{\delta} \quad (12)$$

$$M(\xi) = \frac{\sinh(\xi) + \sin(\xi)}{\cosh(\xi) - \cos(\xi)} \quad (13)$$

$$D(\xi) = \frac{\sinh(\xi) - \sin(\xi)}{\cosh(\xi) + \cos(\xi)} \quad (14)$$

and

$$\delta = \frac{0.071}{\sqrt{f}} \quad (15)$$

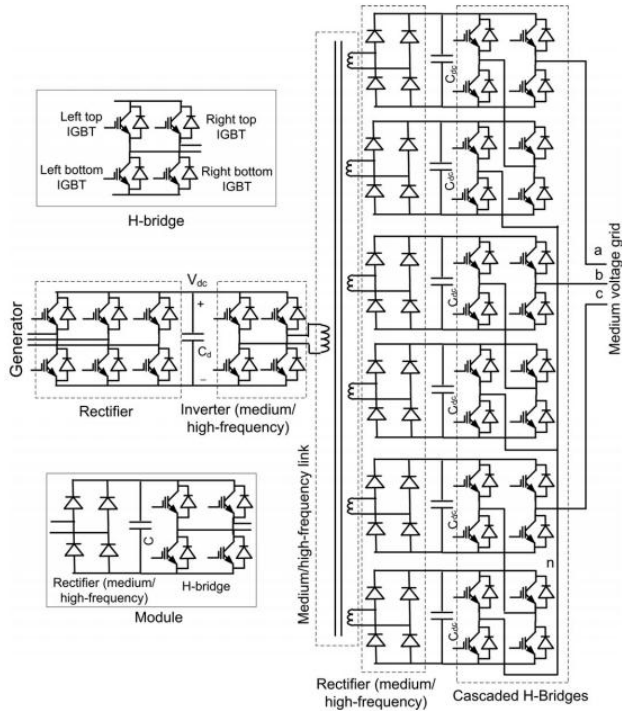


Fig. 3. Detailed power conversion circuit with three-phase five-level converter: for simplicity, single high-frequency inverter is considered. A VHDL code-based program is used to create the LUT, which contains the sine reference.

IV. MATLAB/SIMULATION RESULTS

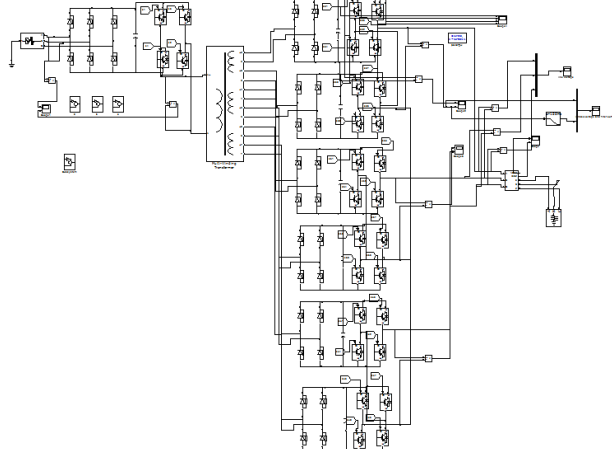


Fig. 4. Matlab/Simulation model of five level Cascaded H-bridge inverter.

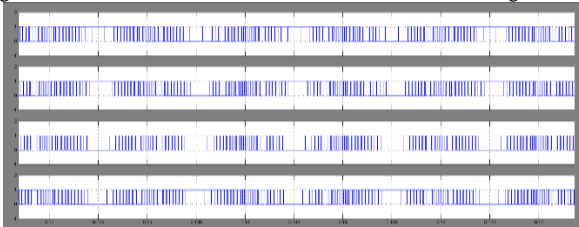


Fig. 5. Gate pulses (15 V) of four IGBTs in the top module in phase.

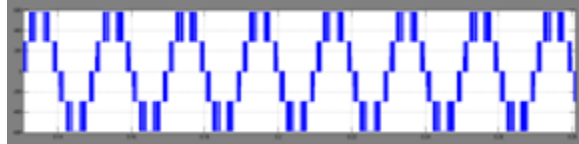


Fig. 6. Five level inverter voltage.

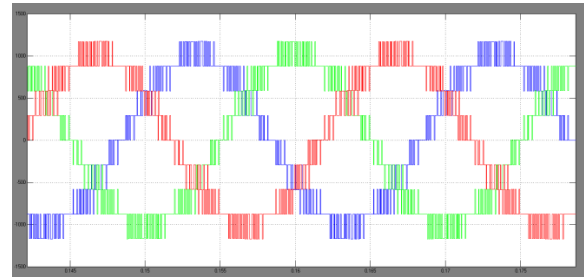


Fig. 7. Three phase voltage.

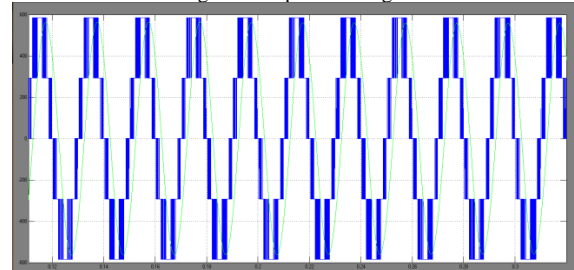


Fig. 8. With Filter and without Filter voltage.

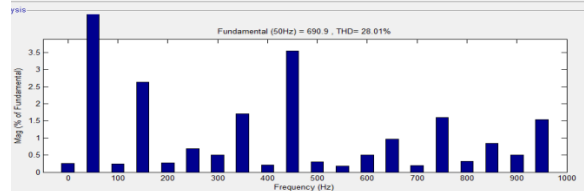
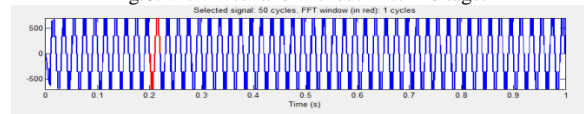


Fig. 9. FFT analysis for five level inverter voltage without filter.

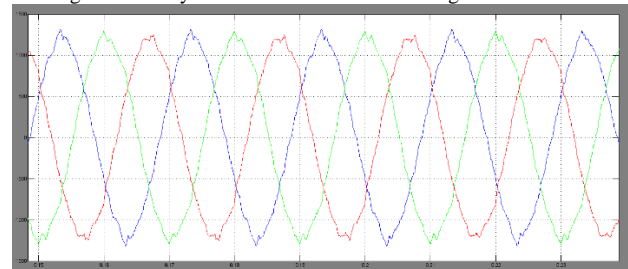


Fig. 10. Simulated line voltages (after filter circuit) of 1-kV multilevel cascaded converter.

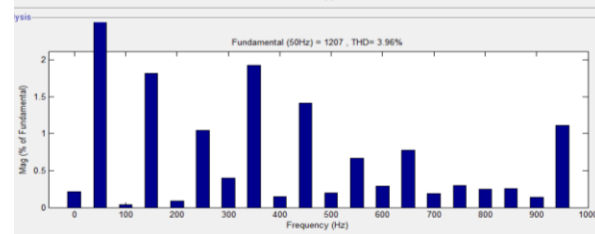
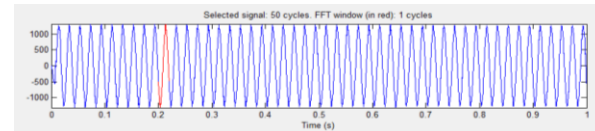


Fig. 11. FFT analysis of five level inverter voltage with filter.

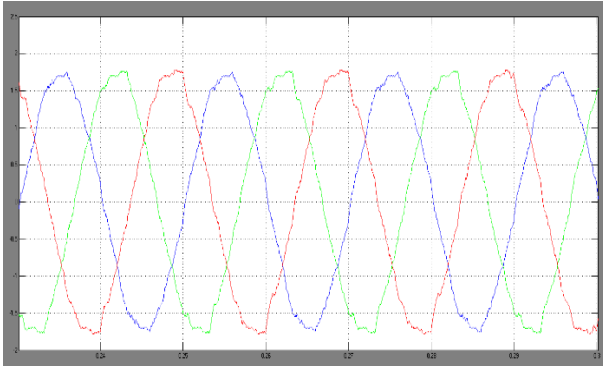


Fig.12. Simulated line currents of the 1-kV multilevel cascaded converter.

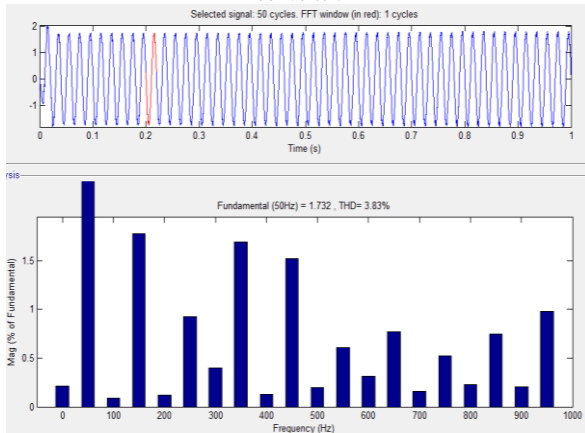


Fig.13.FFT analysis of five level inverter current with filter.

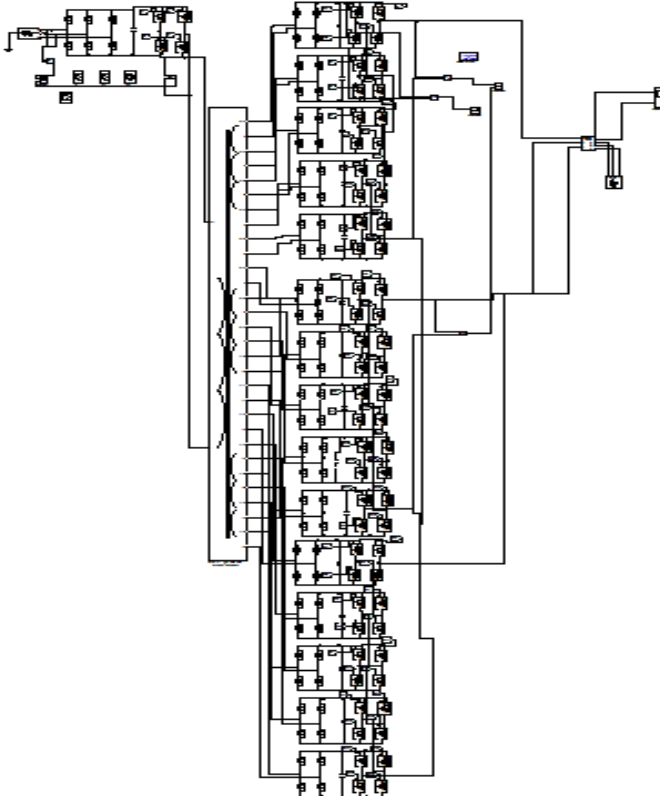


Fig.14.Matlab/Simulation model of eleven level inverter.

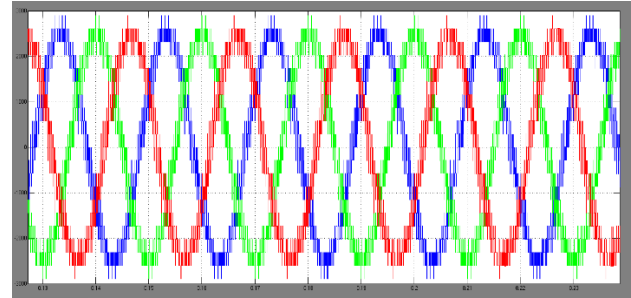


Fig.15.three phase voltage for eleven level inverter.

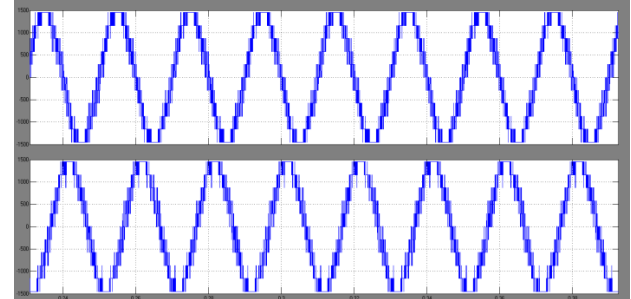


Fig.16.Single phase eleven level inverter voltage for phase a and b.

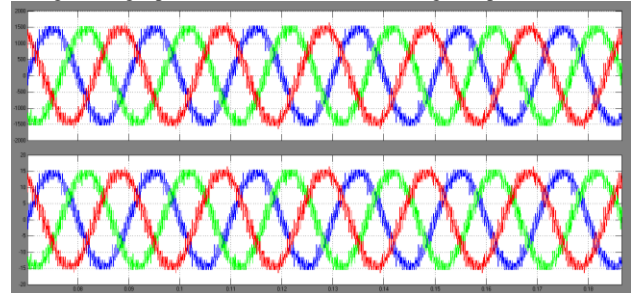


Fig.17.Three phase voltage and current for inverter.

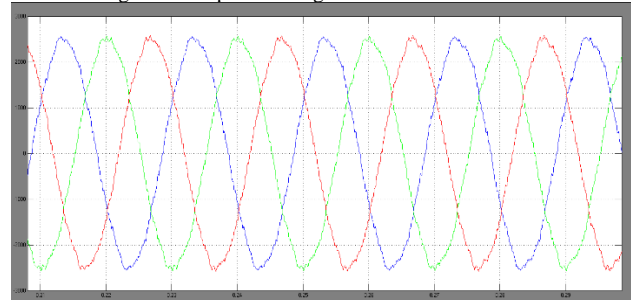


Fig.18.three phase voltage with filter.

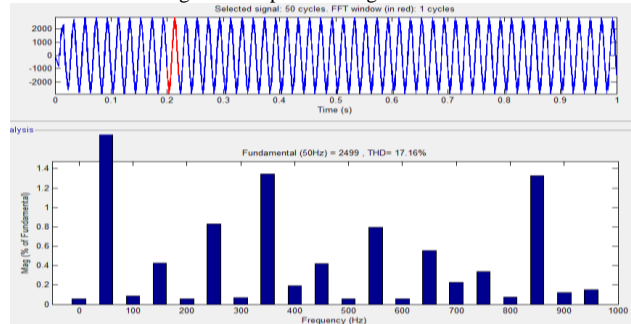


Fig.19.FFT analysis of without filter.

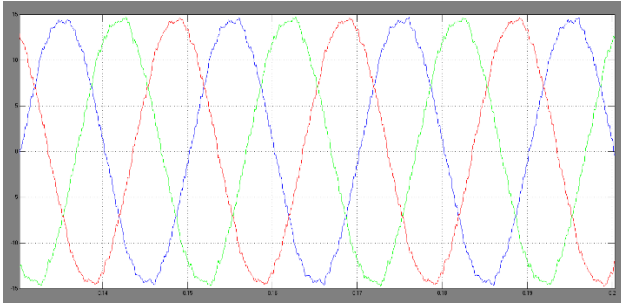


Fig.20.three phase current with filter.

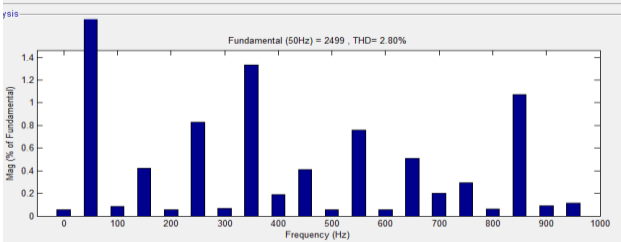
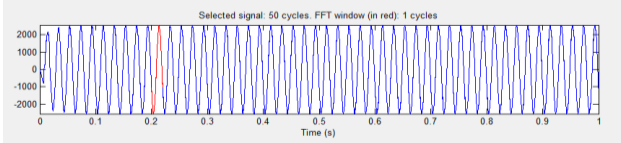


Fig.21.FFT analysis of the voltage with filter.

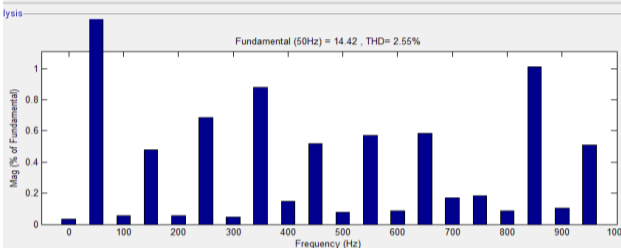
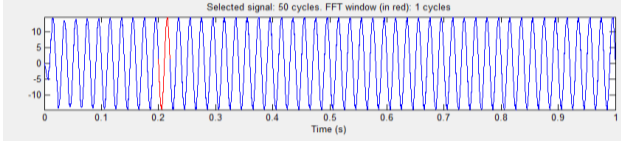


Fig.22.FFT analysis of the current with filter.

V. CONCLUSION

The multiple secondary windings high-frequency link can be a good solution to provide multiple isolated and balanced dc supplies for the MMC converter and to ensure electrical isolation between grid and renewable generations systems. In this paper, the proposed medium-voltage system has been validated by a scaled down three-phase 1-kV system with a five-level and eleven level MMC converter topology. A simulation model for the cascaded multilevel inverter is developed in MATLAB/SIMULINK platform. The inverter output is a five level phase voltage. The paper presents the main circuit model in simulation results in detail. The FFT analysis results verified the proposed cascaded multilevel inverter with a PWM control method.

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