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Analysis of current controlled current conveyor using 120 nm Technology

Neetu narwariya[#1], Deepak sharma[*2]

[#]*Electronics & Communication, R.G.P.V Bhopal*
L.K.C.T. Indore M.P. India
Neetu.narwariya90@gmail.com
[2]deepakd.sharma@gmail.com

***Abstract*—Current mode circuits like current conveyors are getting significant attention in current analog ICs design due to their higher band-width, greater linearity, larger dynamic range, simpler circuitry, lower power consumption and less chip area. The second generation current controlled conveyor (CCCII) has the advantage of electronic adjustability over the CCII i.e. in CCCII; adjustment of the X-terminal intrinsic resistance via a bias current is possible. The presented approach is based on the CMOS implementation of second generation positive (CCCII+), negative (CCCII-) and dual Output Current Controlled Conveyor (DOCCCII). All the circuits have been designed and simulated using 120nm CMOS technology model parameters on TANNAR using 1.5V supply voltage. TSPICE simulations have been carried out to verify the linearity between output and input ports, range of operation frequency, etc. The outcomes show good agreement between expected and experimental results.**

***Keywords*—CMOS, PMOSFET, NMOSFET, CCCII+,CCCII-,DOCCCII.**

Introduction

Current conveyor is a versatile current mode circuit, gaining acceptance as both a theoretical and practical building block. The current conveyor, with one high impedance input, one low impedance input and one high impedance output is a suitable element for both voltage-mode and current-mode circuits. The classical op-amps suffer from limited gain-bandwidth product problems and from low slew rate at its output. So, they remain unsatisfactory at higher frequencies. Moreover supply voltage has become the great concern in present electronic circuit design scenario especially for portable and battery powered equipment and the breakdown voltage of short channel MOS transistors. Since a low-voltage operating circuit becomes necessary, current mode techniques are better suited for such purposes in comparison with voltage-mode ones. Consequently, current mode circuits are receiving significant attention due to their larger dynamic range, higher band-width, greater linearity, simpler circuitry, lower power consumption, and reduced chip area as compared to their voltage mode counterparts like Operational Amplifiers. In recent years, due to the integration suitability with CMOS technology, current mode devices are finding even more consideration in circuit designs [1, 2].

DESCRIPTION OF CURRENT CONTROLLED CONVEYORS

Fig. 1 and Fig. 2 show the symbol and equivalent circuit of the second generation Current Controlled Conveyor (CCCII). A CCCII-based circuit, whether positive, negative or dual output [3], provides electronic tunability and wide tenable range of its resistance at X-terminal [6]. The CCCII requires no external resistors; hence it is very suitable in the design of integrated filters and oscillators. Also, as the CCCII is current controlled current source, the CCCII based circuit is very suitable for high

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frequency operation. These features are very attractive to circuit designers [4].

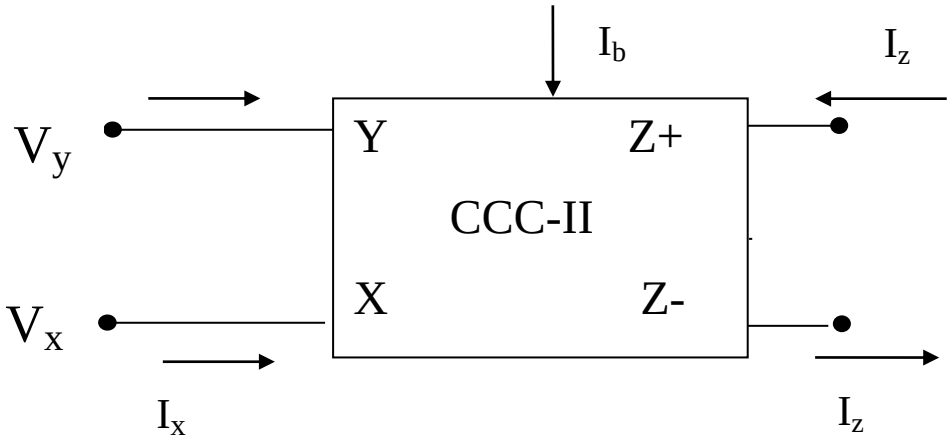

Fig.1: Symbol for CCCII

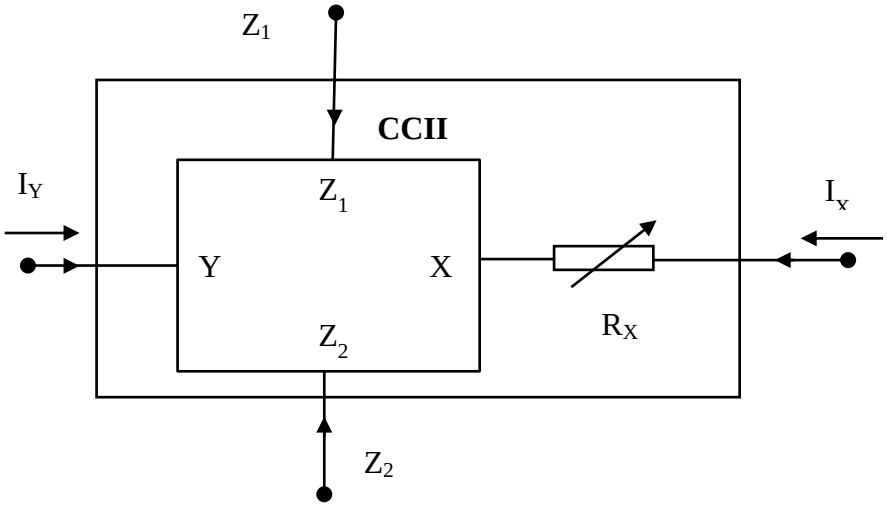

Fig.2 Eqivalent Circuit Diagram of CCCII

The relationship between the voltage and current variables at input and output ports X, Y and Z of the CCCII can be expressed by the following matrix,

Where the sign ± refers to plus-type or minus-type CCCII, respectively, and RX denotes the intrinsic resistance at X terminal. RX is adjustable by a supplied bias current I_b which can be expressed through a class AB trans-linear loop, which is used as input section.

$$I_Y = 0$$

$$V_X = V_Y + I_X R_X$$

$$I_{Z+} = I_X$$

$$I_{Z-} = -I_X$$

$$R_X = 1/g_m$$

CMOS IMPLEMENTATION OF CCCII

Fig. 3, 4, and 5 respectively show the schematics of conventional CMOS implementation of positive, negative and dual output current controlled conveyor (CCCII+, CCCII-, DOCCCII). We know that MOS-transistors in particular are more suitable for processing currents rather than voltages, because both in common-source and common-gate amplifier configurations the output signal is a current, while common drain amplifier configuration are almost useless at low supply voltages because of the bulk-effect present in typical CMOS processes. Moreover, MOS current-mirrors are more accurate and less sensitive to process variation than bipolar current mirrors because with the latter the base currents limit the accuracy. So, MOS-transistor circuits should be simplified by using current signals in preference to voltage signals. When the signal is conveyed as a current, the voltages in MOS transistor circuits are proportional to the square root of the signal, if saturation region operation is assumed for the devices [5,7]. Therefore, a compression of voltage signal swing and a reduction of supply voltage is possible. Also, with very high values for the drain currents of the MOS, their maximum usable frequency will be reached sooner.

The circuit in Fig. 3 consists of one mixed trans-linear loop (transistors M1 to M4) as input cell. Two current mirrors (transistors M5, M6 and M7, M9) allow the mixed loop to be dc biased by the current Ib, the input cell present a high input impedance input port (Y) and a low impedance output port(X).

This cell act as a voltage follower. The output Z that copies the current flowing through port X is realized in the conventional manner using two complementary mirror [4]. As shown in Fig. 4, current mirrors built up of M11,M12 & M15,M17 and M14,M16 & M10,M13 are cross coupling to generate negative current at Z. While in Fig. 5 generates both types of the output.

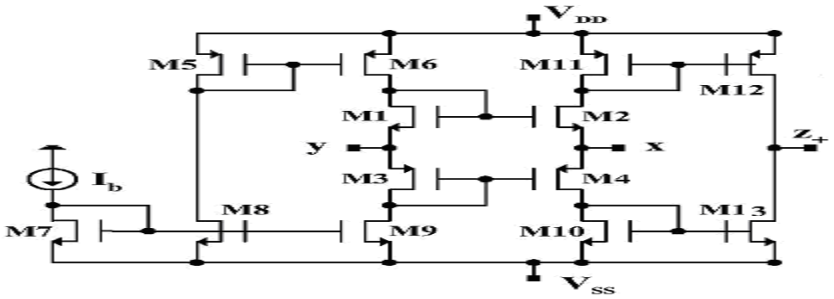

Fig.3 CMOS based circuit of CCCII+

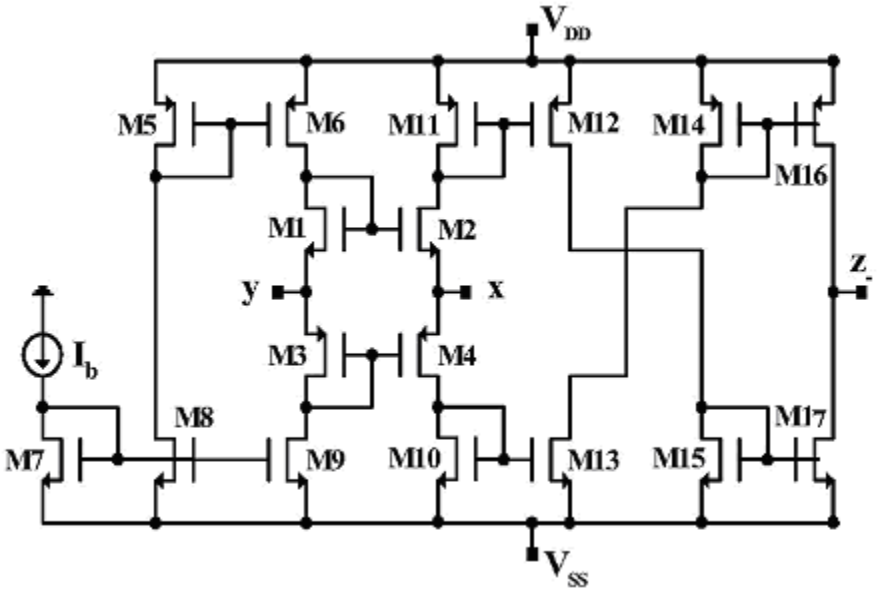

Fig.4 CMOS based circuit of CCCIIFig

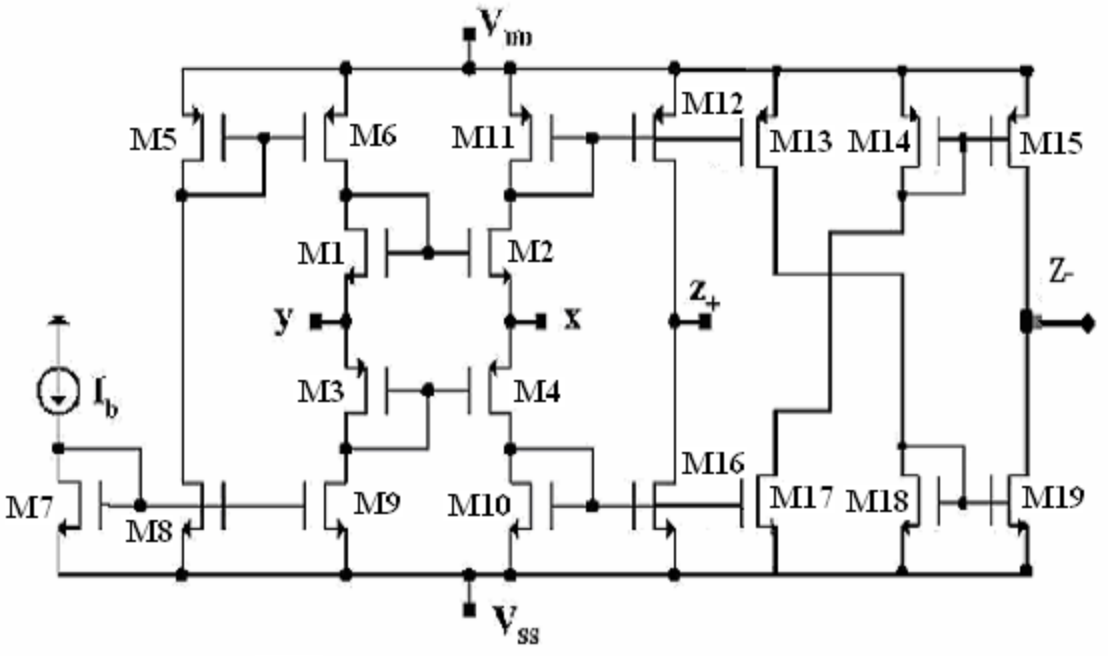

Fig.5 CMOS based circuit of DOCCCII

ANALYSIS OF CCCII

Fig. 6, 7, and 8 show the transient and AC analysis of CCCII+, CCCII- and DOCCCII respectively. AC analysis shows the range of frequency of operation and it indicates that current relationship is accurate up to 1GHz for all three CCCII circuits.

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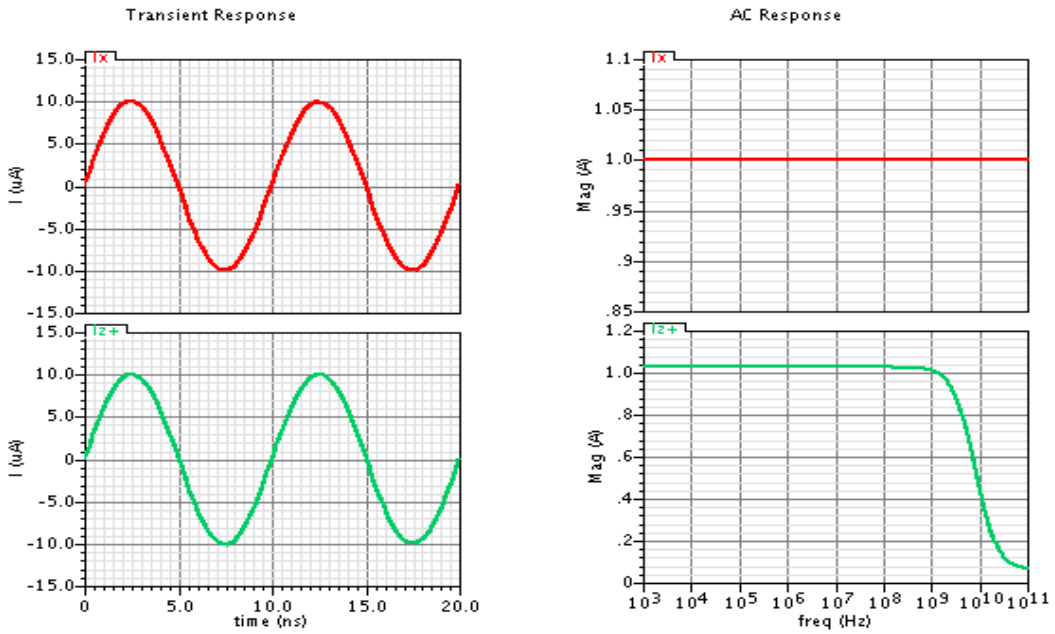

Fig.6 Transient and AC analysis of CCCII+

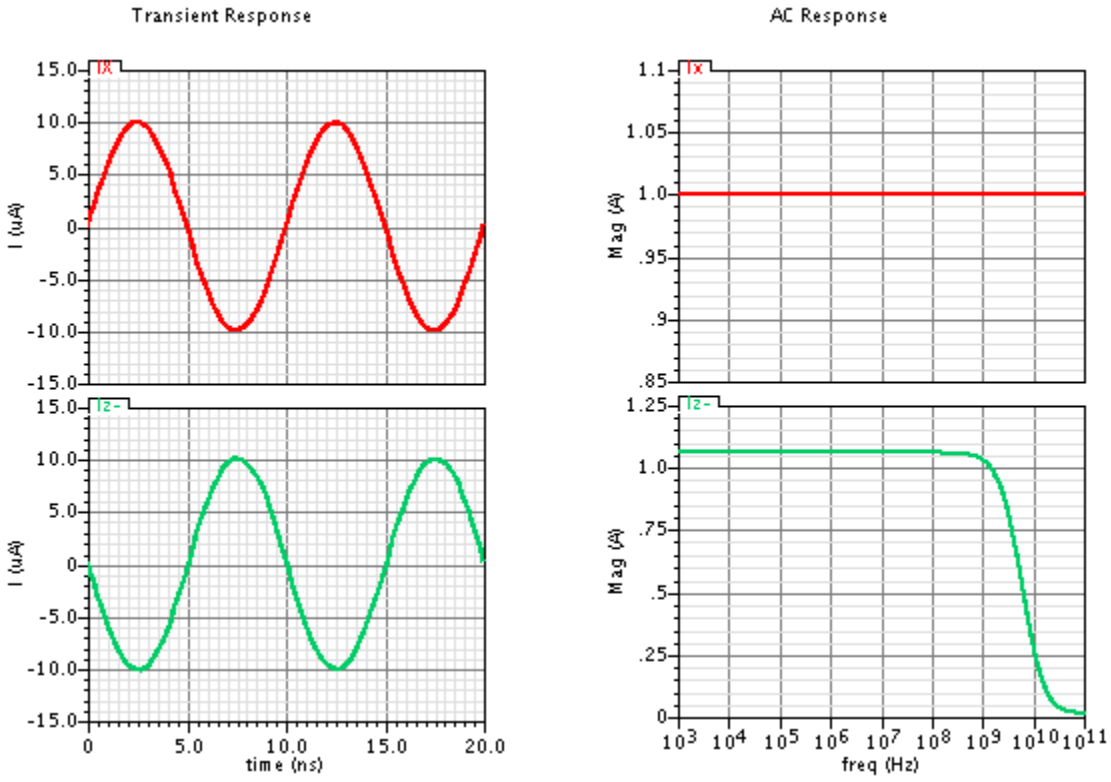

Fig.7: Transient and AC analysis of CCCII

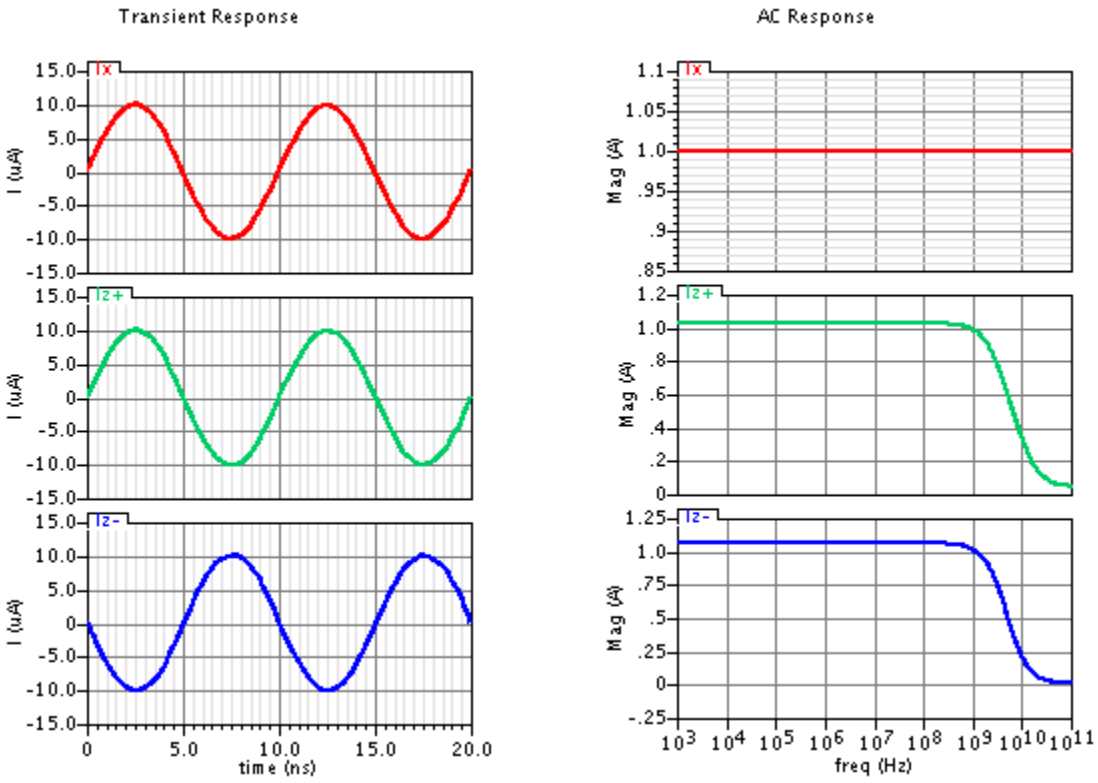

Fig.8: Transient and AC analysis of DOCCCII

Transient analysis has been carried out with 100 MHz frequency sinusoidal input undistorted output. At frequencies higher than 100 MHz we may find phase shift in the output, so its actual range of frequency is around 100MHz.

DC analysis has also been done to find the linearity between input and output ports. So in this way all three CCCII+, CCCII-, DOCCCII verified the current relationship equation i.e. Iz=+Ix, Iz=-Ix and Iz=±Ix respectively.

CONCLUSION

We presented a CMOS implementation of CCCII+, CCCII-, DOCCCII circuit in 120nm CMOS technology. The design, based on a ±1.5V DC supply and developed using TANNAR tool, achieves good linearity, low power dissipation and high bandwidth in the device.

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