Implementation of Differential Voltagecuurent Conveyor Using Dvcc

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Abstract— The proposed second generation DVCC has been designed in 0.12μm CMOS technology with 1.5V supply voltage. Tanner tool simulator is used for circuit simulation. In low voltage sub-micrometer analog circuit accuracy and precision can be limited by the finite gain as well as by input offset voltage. Proposed circuit features have high gain, high bandwidth and low power dissipation that can be achieved simultaneously without requiring well matched register.

Keywords—CMOS, PMOSFET, NMOSFET, OPAMP, CMRR, SLEW RATE,GAIN, TANNER TOOL,CC.

INTRODUCTION

The current conveyor may be a basic building block that may be enforced in analog circuit style. This was introduced by sedra and Smith in 1968 however its real blessings and innovative impact wasn't clear at that point [2]. In recent years, current mode circuit have emerged as a very important category of circuits with properties of

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accuracy, high frequency vary and flexibility in an exceedingly wide of range of applications. Current conveyor represents the rising category of high performance analog circuit style supported current mode approach. it's straightforward design, wider information measure and capability to control at low voltage
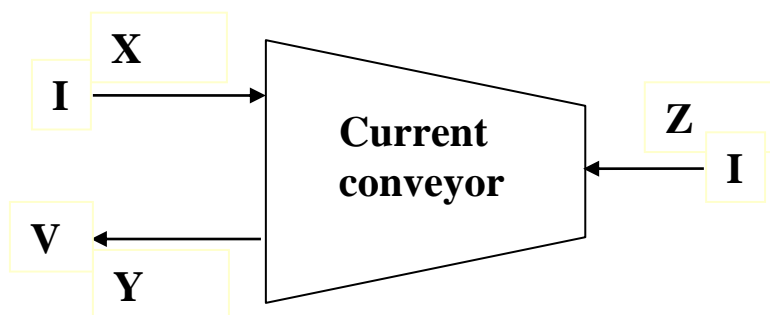

Figure 1: Representation of current conveyor

The current conveyor black box was a three terminal device (X and Y is input terminals, Z is output terminal) with following properties [5]:

1. The potential at its input terminal X is equal to the voltage applied at the other input terminal Y.
2. An input current that is forced into node X result in an equal amount of current flowing into node Y.
3. The input current flowing conveyed to output terminal (X terminal to Z terminal), which has the

characteristics of a high output impedance current source.

The term conveyor refers to the third property above the third property refer convey; current is sent from the input terminal to the output terminal, whereas decoupling the circuits connected to the current terminal. When a voltage supply is applied to port Y, then a similar potential can seem on the port X and if a current is forced through port X, Associate equal current can flow through port Y

(depending upon the characteristics of the CC). The same current is also conveyed to output port Z, which is at a high impedance level.

Second Generation Current Conveyor (CCII)

The second generation current conveyor (CCII) is one in all the foremost versatile current mode building blocks [3]. For several application s, a high ohmic resistance input port is preferred so as to avoid loading impact. So, second generation current conveyor was developed to fulfill this demand. It's one high and one low ohmic resistance input port instead of the 2 low ohmic resistance input port of CCI [2].Since it's introduced in 197, it's been utilized in big selection of application and a number of other circuits are accomplished victimization this block. The CCII may be thought of because the basic analog circuit style block as a result of all the active devices may be made from an appropriate association of 1 or 2 CCIIs. It's a {3} terminal device and also the block illustration of this conveyor is shown in figure 2.
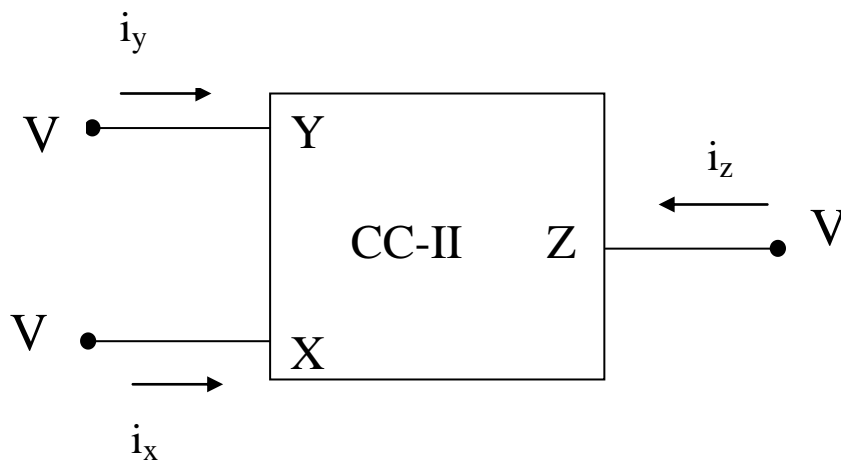

Figure 2: Block Representation of CCII

This current conveyor differs from the primary generation current conveyor in a very sense that the port Y may be a high resistivity port i.e. there's no current following into port Y. The port Y of the second generation current conveyor is employed as a voltage input and port Z is employed as a current output port. Whereas, the port X may be used as a voltage output or as a current input port. Therefore, this current conveyor may be accustomed method each voltage and current signal.

The relation between the terminal voltages and current of CCII can be given by the following matrix relation.

There are two types of second generation current conveyor

A. Positive current conveyor (CCII+) in which the currents direction of i_x and i_z are same as in a current mirror.

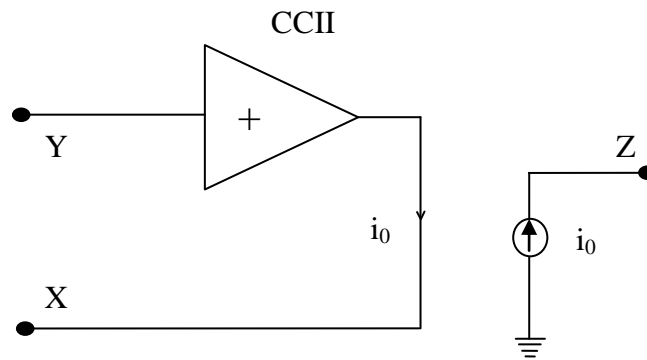B. Negative current conveyor (CCII-) in which currents direction i_x and i_z are the different as in current mirror.

$$\begin{bmatrix} I_Y \\ V_X \\ I_Z \end{bmatrix} = \begin{bmatrix} 0 & 0 & 0 \\ 1 & 0 & 0 \\ 0 & \pm 1 & 0 \end{bmatrix} \begin{bmatrix} V_Y \\ I_X \\ V_Z \end{bmatrix}$$

These two conveyors are shown in figure
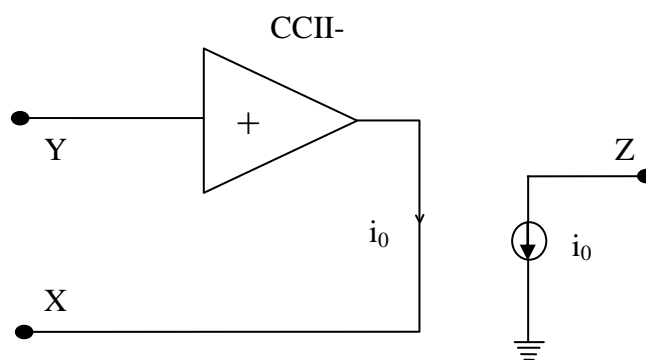
CCII

Figure3 (a) Positive CCII+

CCII-

Figure3 (b) Negative CCII-

PROPOSED DIFFERENTIAL VOLTAGE CURRENT CONVEYOR

The Differential voltage conveying action of the circuit is based on the differential pairs M_3, M_4 and M_5, M_6. The current mirror formed by the transistor M_1 and M_2 forces the sum of the drain currents of the drain currents of M_3 and M_5 the sum of the drain currents of M_4 and M_6, hence using standard notation, the port relations of an idea DVCC can be characterized by:-

$$V_{G1} - V_{G2} = V_{G4} - V_{G3}$$

$$V_x = V_{Y1} - V_{Y2}$$

Transistor M2 and M12 provide the necessary feedback action to make the voltage V, independent of the current drawn from the terminal X. the current through terminal X is conveyed to the Z1 terminal by the current mirrors consisting of transistors M_7, M_8 and M10, M11. The operation of this circuit is not affected by the body effect. All the PMOS transistors have sources which are connected to the positive supply rail, while all Nmos transistors, except M_3, M_4, M_5 and M_6, have sources connected to the negative supply rail.
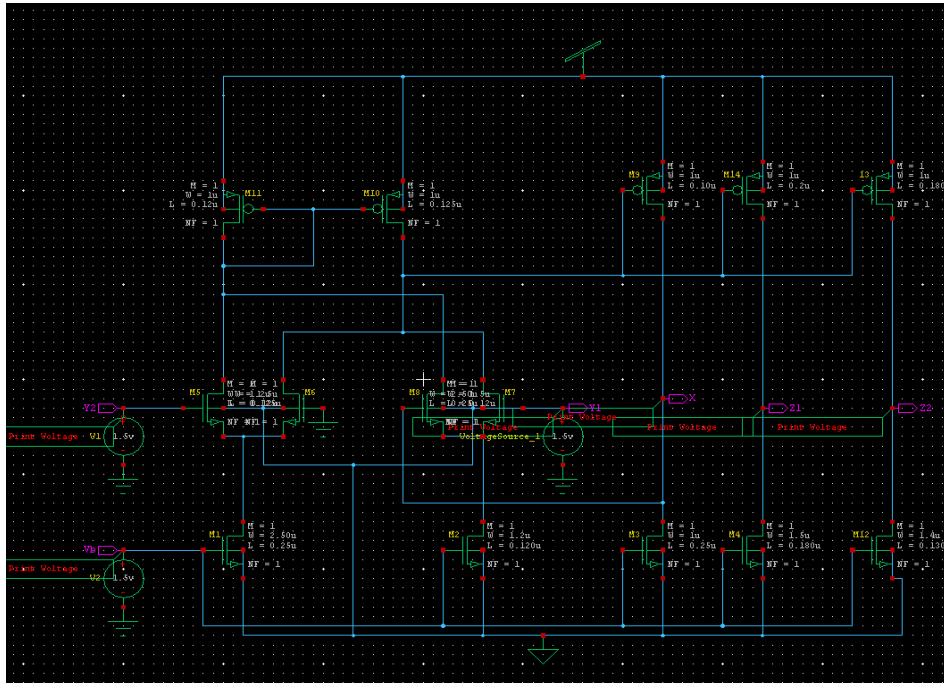
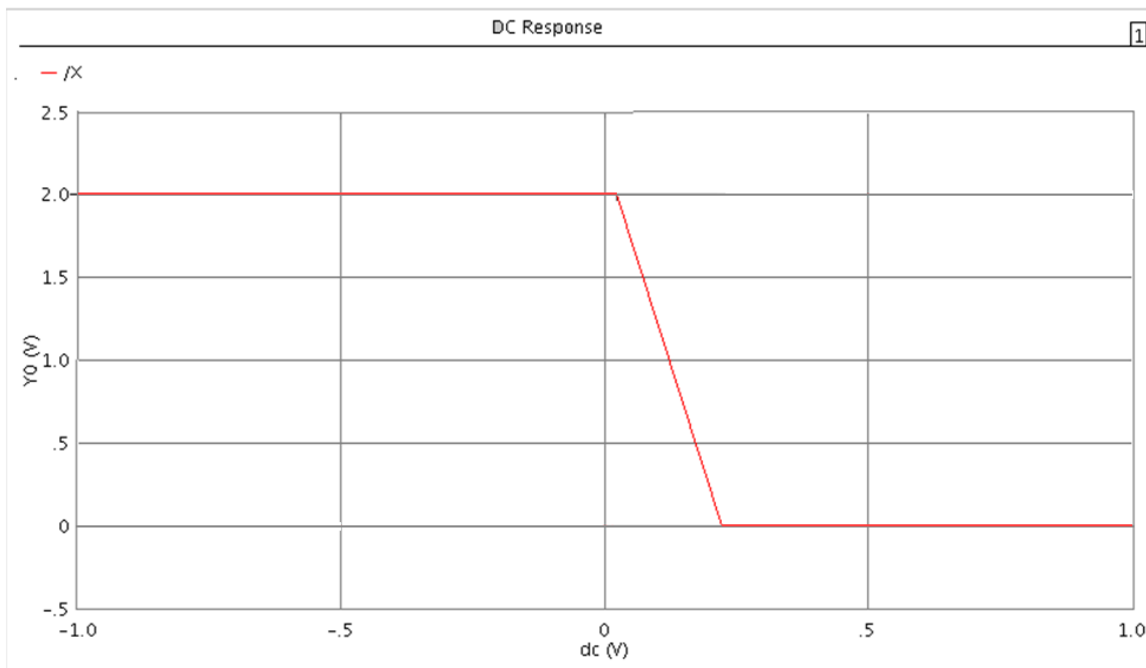**Figure 4 proposed dvcc**

RESULTS

DC Response:-

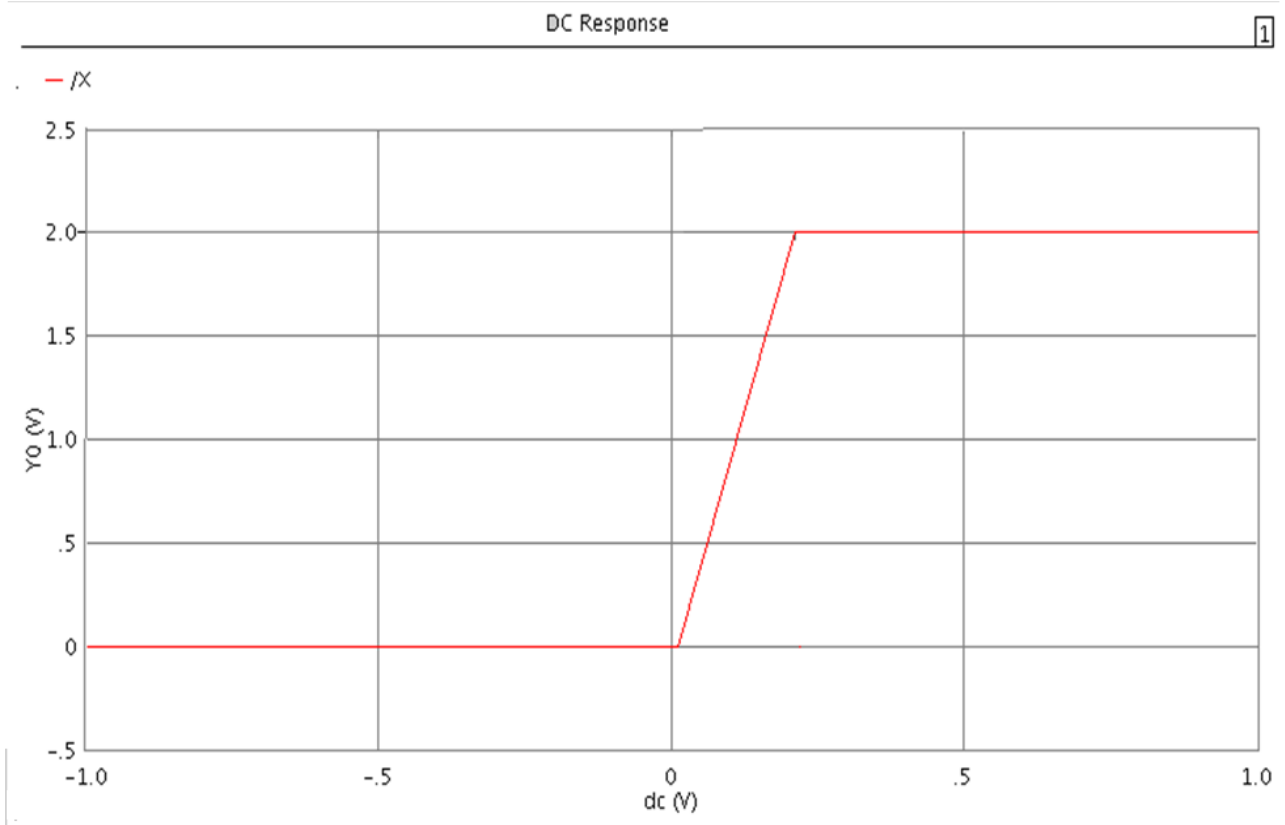**Figure5:-DC Response for Positive Terminal**

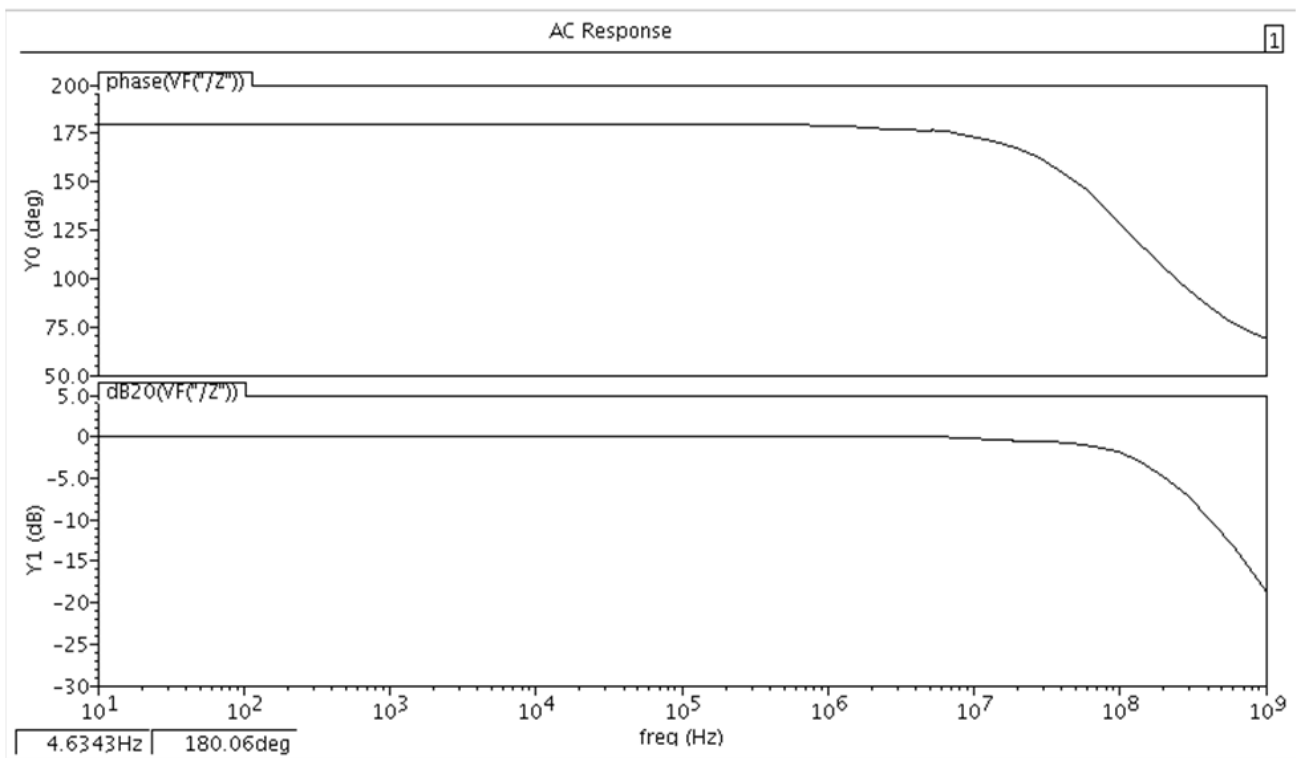**Figure 6: DC Response for Negative Terminal**

AC Response:-

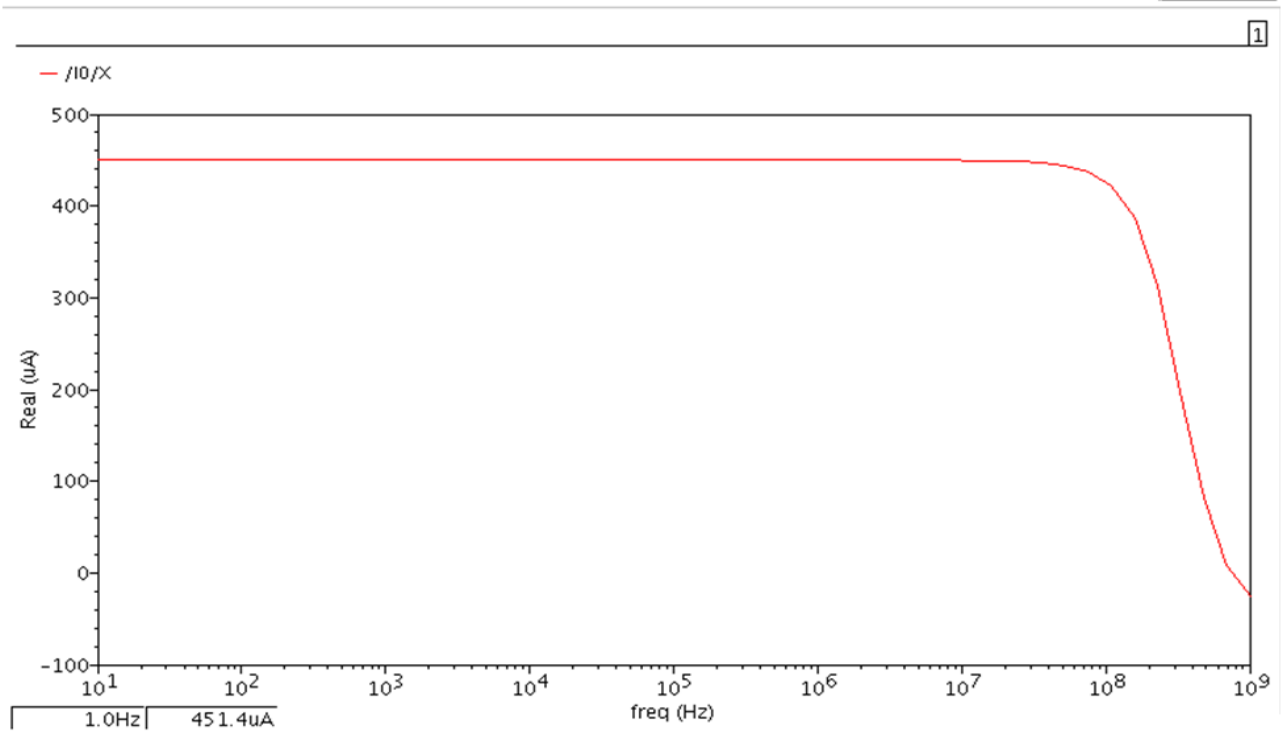**Figure 7:Magnitude and Phase Response**

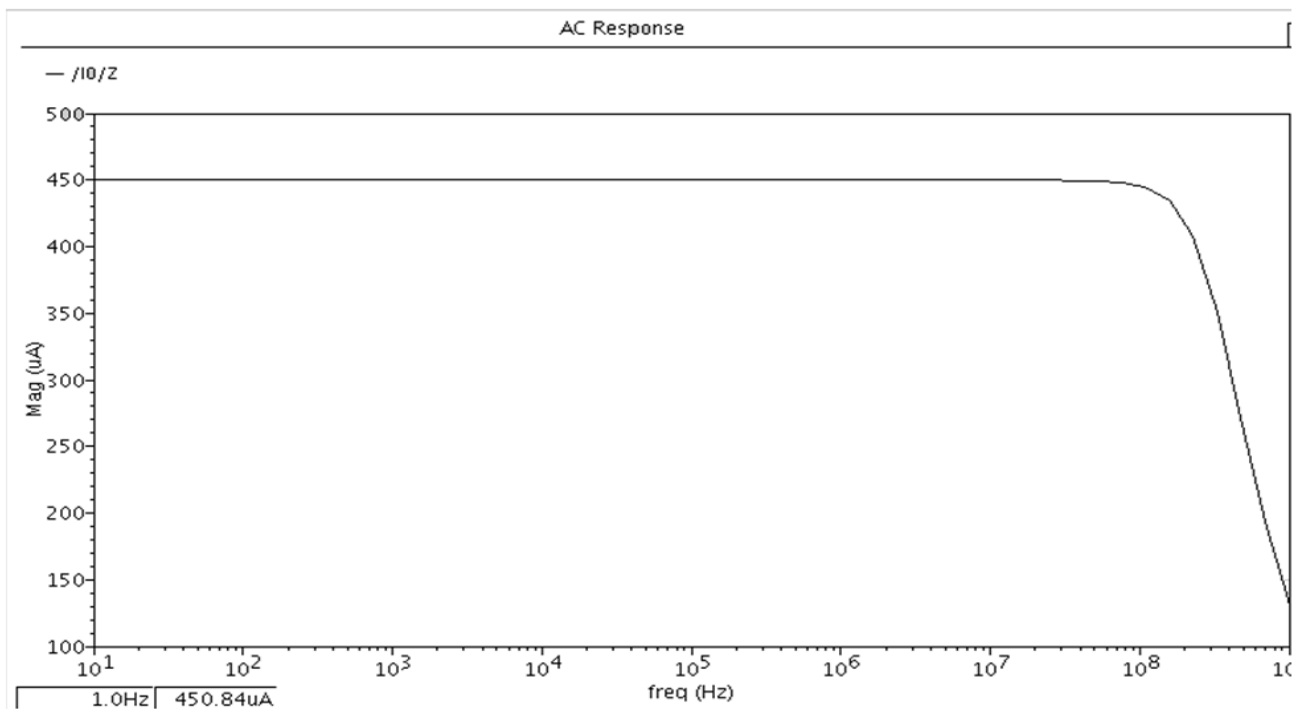**Figure 8: Current at terminal X**

Figure 9: Current at terminal Z

CONCLUSION

Among various Morden active building blocks, DVCC is emerging as quite flexible and versatile for analog circuit design and has been used for a variety of functions. To realize the current mode

(CM) analog filter, DVCC is an important and economical solution. The circuit structure of DVCC is simple and easy to implement in integrated circuits. The circuit has been fonud to be small sensitive and with possibility to easy control the filter parameters (the pole and zero frequencies and the quality factors) by electrically changing the trans-conductance. The proposed universal filter is capable to use especially at higher frequency ranges. That's why DVCC have been finding prominent attention in the area of analog signal processing. All varity of the filter can be obtained by altering the position of input and output terminals. All simulation carried out by TANNAR Tool in 0.12 μ m CMOS technology. The result is justified and match with standard results.

REFERENCES

[1] Sedra A, Smith K. A second-generation current conveyor and its applications. IEEE Transactions on Circuit Theory 1970; 17:132–4.

[2] SEDRA, A.S, ROBERTS, *G* w., and GOHH, F: 'the current conveyor: History, progress and new results', *IEE Proc. G, Circuits Devices Syst.,* 1990, **137,** *(2),* pp. 78-87.

[3] Mahmoud SA. Fully differential CMOS CCII based on differential difference trans-conductor. Analog Integrated Circuits and Signal Processing 2007; 50:195–203.

[4] Ismail AM, Soliman AM. Novel CMOS liberalized balanced output trans-conductance amplifier based on differential pairs. Frequenz 1999;53:170–4

[5] Mahmoud SA. Fully differential CMOS CCII based on differential difference trans-conductor. Analog Integrated Circuits and Signal Processing 2006; 49:267–79.

[6] YOU, F., **EMBABI,** S.H.K., and SANCHEZ-SINENCIO, E.: 'Low-voltage class AB buffers with quiescent current control', *IEEE J. Solid- State Circuits,* 1998, **33** *(6),* **pp.** 915-919.

[7] FABRE, A, SAAID, O., WIEST. F. and BOUCHERON, C.: 'High frequency application based on a new current controlled conveyor', *IEEE Trans. Circuits Syst.-I,* 1996, **CAS-43,** *(2),* pp. 82-91.

[8] K.C. Smith and A.S. Sidhra, "The current conveyor-a new circuit building block," Proc.IEEE,vol 56 pp. 1368 -1369 Aug. 1968

[9] J.H.Huijsing and J.De Korte, "Monolithic nullor-a universal active network element" IEEE Journal of Solid State Circuit, Vol. SC-12, pp. 59-64, Feb. 1977.

[10] A.S.Sedra and K.C..Smith, "A second generation current conveyor and its application," IEEE Trans Circuit Theory,vol. CT-17,pp. 132-134,1970.

[11] M.A.Lbrahim, and H.Kuntman, "A new voltage-mode KHN-BIQUAD using differential difference current conveyor" Inter. Conf. On Electrical and Electronics Engineering, Bursa Turkey, Dec. 3-7, 2003.

[12] W.Chiu, S. I. Liu, H. W. Tsao, and J. J. Chen, "CMOS differential difference current conveyor and their application" IEE Proc. Circuit Device Syst, Vol. 143(2), pp.91-96, 1996.