International Journal of Research
Available at https://edupediapublications.org/journals
p-ISSN: 2348-6848
e-ISSN: 2348-795X
Volume 03 Issue 13
September 2016

Parasitic Boost Circuit For Transformer Less Active Voltage Quality Regulator With Closed Loop Controller

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Abstract— Power Quality (PQ) problems have obtained increasing attentions as they can affect lots of sensitive end-users. Studies indicate that voltage sags, transients and momentary interruptions constitute 92% of all the PQ problems occurring in the distribution power system. Typical sag can be a drop between 10% and 90% of the rated rms voltage and has the duration time of 0.5 cycles to 1 min. According to the data presented, majority of the sags recorded are of depth no less than 50%, but deeper sags with long duration time obviously cannot be ignored as they are more intolerable than shallow and short-duration sags to the sensitive electrical consumers. The most studied voltage regulator topologies can be generally categorized into two groups the inverter-based regulator and direct AC–AC converters. Series-connected Devices (SD) are voltage-source inverter-based regulators and an SD compensate for voltage sags by injecting a missing voltage in series with the grid. A new design is proposed in order to compensate the voltage levels. High operation efficiency is obtained by this method of controlling due to application of the DC link voltage adaptive control method. Additionally, the proposed active voltage quality regulator is a cost effective solution for long duration sags that are lower than 50% of the nominal voltage as it is transformer less compared with the traditional dynamic voltage restorer.

Index Terms—Dynamic voltage restorer (DVR), dynamic sag correction, long duration deep sag, parasitic boost circuit, series connect compensator.

I.INTRODUCTION

Sensitive end-users including industrial and commercial electrical consumers are facing serious problems because of the Power Quality problems.92% of all the PQ problems occurring in the distribution power system are due to voltage sags, transients, and momentary interruptions. Even 0.25 s voltage sag is long enough to interrupt a manufacture process resulting in enormous financial losses, which shows seriousness of voltage sags. Many power devices have been proposed to mitigate voltage sags for sensitive loads [1]. The used topologies are: the AC inverter-based regulator and direct AC-AC converters. Series-connected Devices (SD) are voltage-source inverter-based regulators and they compensate voltage sags by injecting the missing voltage in series with the grid. The key features related to the evaluation of certain SD topologies are cost, complexity and compensation ability. Dynamic Voltage Restorer (DVR) is a commonly used SD [2, 3]. Four typical DVR system topologies are investigated and experimentally compared. The evaluation shows that DVR with no storage and load connected shunt converter ranks the highest as it can compensate long duration deep sags at a relatively low complexity and cost. DySC is changed according to the structural differences between the DVR with load connected shunt converter and the one with supply-connected shunt converter [4, 5]. As a result, the shunt converter together with the series converter forms a boost charging circuit and the DC-link voltage will be charged to exceed the peak value of supply voltage. Thus obtained novel topology is called the transformer-less active voltage quality regulator with the parasitic boost circuit (PB-AVQR), and it is capable of mitigating long-duration deep voltage sags without increasing the cost, volume and

complexity compared with the traditional DySC topology. The DC-link voltage adaptive control method proposed and is also applied in the PB-AVQR to improve its efficiency [6].

A type of transformer less SD topology known as dynamic sag corrector (DySC) is proposed, and it is a low cost, small size, light weight, and highly effective system for sag mitigation as the series transformer is no longer needed. When the grid voltage differs from its desired waveform, a missing voltage will be injected and filtered by the DySC through its half-bridge converter (V1, V2) and output filter (Lf, Cf) to maintain the load voltage at its rated value [7, 8]. During this period of time, the energy needed for the compensation is provided by the residual supply via a passive shunt converter (D1, D2,L1) and stored in the dc-link capacitors (C1,C2). So, the dc-link voltage should always be lower than the peak value of the supply voltage, and it means that the DySC can only compensate for voltage sags no deeper than 50% since the largest injection voltage of the DySC is solely determined by its dc-link voltage [9].

This obtained novel topology is called the transformer less active voltage quality regulator with the parasitic boost circuit (PB-AVQR), and it is capable of mitigating long duration deep voltage sags without increasing the cost, volume, and complexity compared with the traditional DySC topology [10]. The dc-link voltage adaptive control method proposed is also applied in the PB AVQR to improve its operation efficiency. This paper starts with introducing the operating mode and working principles of the proposed configuration. Then, the parasitic boost circuit model is provided followed by the theoretical analysis to calculate its dc-link voltage [11].

II TOPOLOGY AND PRINCIPLE

As shown in Fig. 1, the PB-AVQR topology is mainly consists of five parts, including a static bypass switch (VT1, VT2), a half-bridge inverter (V1, V2), a shunt converter (VT3, VT4), a storage module(C1,C2), and a low-pass filter (Lf, Cf).The operating mode and applied control strategies are similar to what have been described. Under normal operating conditions, the static bypass switch is controlled to switch on and the normal grid voltage is delivered directly to the load side via this bypass switch. When an abnormal condition is detected, the static bypass switch will be switched OFF and the inverter will be controlled to inject a desired missing voltage in series with the supply voltage to ensure the power supply of sensitive loads. There are totally two different kinds of control strategies in the proposed PB-AVQR system. When the grid voltage is lower than the rated voltage, an in-phase control strategy will be adopted and a phase-shift control strategy will be applied when the supply voltage is higher than the nominal voltage.

Working principle of the PB-AVQR is different compared with that of the DySC due to its unique shunt converter structure. When the proposed configuration is analyzed, both the operating states of the switches (V1, V2) and the trigger angles of the thyristors (VT1, VT2) should be taken into consideration. So, a simplified PB-AVQR (SPB-AVQR) circuit shown in Fig. 2 where two thyristors (VT3, VT4) in the proposed PB-AVQR are replaced by two diodes (D1, D2), is firstly introduced to better explain its working principles. The following analysis will be based on the SPB-AVQR which can be regarded as a special type of PB-AVQR.

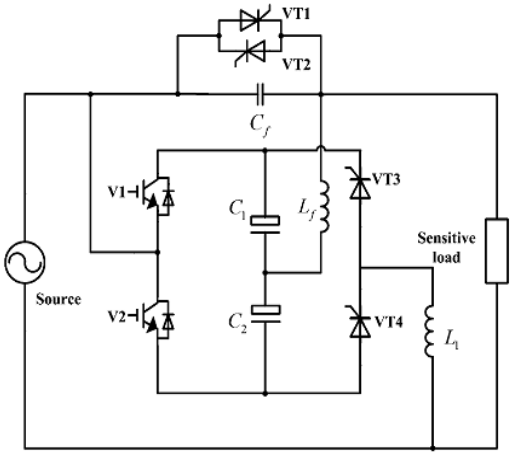

Fig.1.Proposed PB-AVQR Topology.

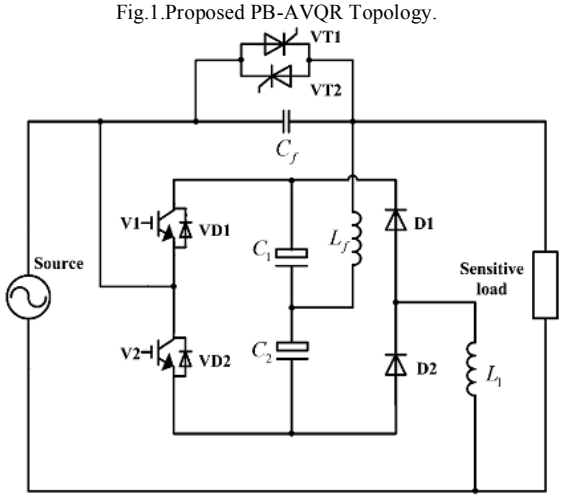

Fig.2.SPB-AVQR Topology.

The only difference between these two configurations is that the shunt converter of the PB-AVQR is controllable while the shunt converter of the SPB-AVQR is uncontrollable. That is to say, the dc-link voltage of the SPBAVQR represents the upper limit of the dc-link voltage in the PB-AVQR structure. So, theoretical

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conclusions drawn with the SPB-AVQR are basically applicable to the PB-AVQR.

As shown in Fig. 2, switches V1 and V2 are now also parts of the parallel circuit, which means that the dc-link voltage will be affected by the on/off status of the switches. So, the turn on and turn off conditions of the compensation process should be considered to understand the working principles about the parasitic boost circuit of the SPB-AVQR. Figs. 3 and 4 illustrate four different operating conditions of the SPB-AVQR within one switching cycle during the positive and negative half-cycle of the sinusoidal supply voltage separately. Both the compensation process and charging process can be explained based on these operating conditions.

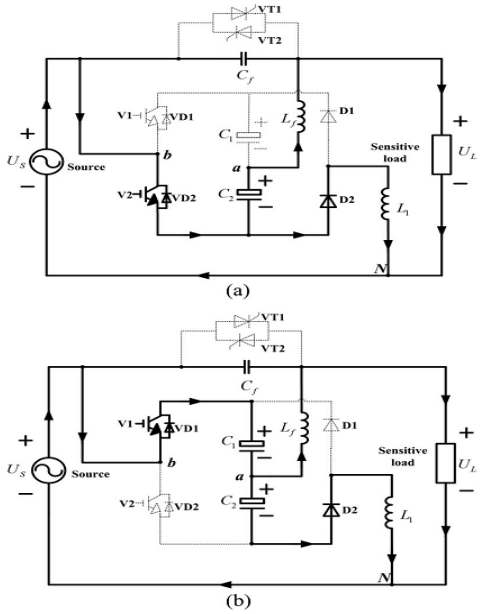

Fig.3. Operating Conditions during Positive Half-Cycle. (A) V2 Switched On (B) V2 Switched Off.

In Figs. 3 and 4, the solid line means that there is current flowing through and arrows depict directions. Operating conditions during the positive half-cycle are illustrated in Fig. 3. When V2 is switched on, as shown in Fig. 3(a), the grid charges the inductor L1 via the diode D2 and the capacitorC2 discharges to maintain the load voltage.

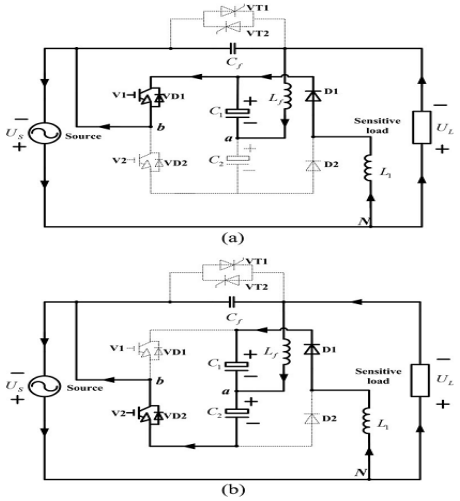

Fig. 4.Operating Conditions during Negative Half-Cycle. (A) V1 Switched On. (B) V1 Switched Off.

When V2 is switched off, as shown in Fig.3.(b), the energy stored in the inductor during previous period is released to dc-link capacitors C1 and C2 through VD1 which is the anti parallel diode of V1. Operating conditions during the negative half-cycle are given in Fig. 4. When V1 is switched on, as shown in Fig.4 (a), the inductor L1is charged via the diode D1, and the load is compensated by the capacitorC1. When V1 is switched off, as shown in Fig. 4(b), the energy stored in L1 is released through VD2, which is the anti parallel diode of V2, to capacitorsC1 andC2. So, in each half-cycle of the grid, one capacitor of the dc-link discharges to provide the energy needed for the compensation, and this energy is actually obtained from the supply source via the charging process described earlier.

Apparently, the charging circuit of the proposed configuration works exactly like a boost circuit and the dc-link voltage in this situation is controlled by the duty ratio of the two switches. So, the compensation ability of the SPB-AVQR is theoretically unlimited as long as the grid is strong enough to provide the needed power. However, as the boost circuit is parasitic on the series inverter, and the two switches are actually controlled according to the missing voltage, there still exist some restrictions. The relationships between the dc-link voltage and other system parameters will be discussed in the next section. In Figs. 3 and 4, two endpoints of the inverter are marked as a and b. Parts of the waveforms obtained at the inverter side and load side under four operating conditions are schematically showninFig.5, where UaN represents the voltage between a and N. As shown in Fig.6., when V1/V2 is switched on/off, the dc-link voltage will be added/subtracted to the supply voltage to get a switching pulse voltage UaN and the switching harmonics of UaN

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will be filtered by Lf and Cf to get a smooth load voltage. So, the load voltage will be maintained at its rated value if the inverter is properly controlled according to the required missing voltage during sags.

III. MODELING AND THEORETICAL ANALYSIS

DC-link voltage is a key parameter to evaluate the compensation ability about a series compensation device since it decides the maximum value of the injected compensation voltage. In this section, in order to evaluate the compensation ability of the proposed topology and verify its feasibility in mitigating long duration deep sags, relationships between the dc-link voltage and other system parameters will be derived based on the circuit model of the aforementioned operating conditions. As can be seen from Figs. 3 and 4, working principles during the positive and negative half-cycle of the supply voltage are the same, so the following analysis will be focused on the situation in the positive half-cycle.

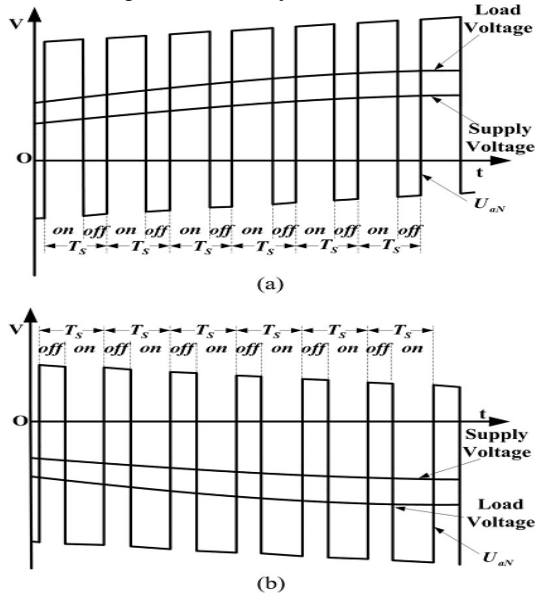

Fig. 5 Waveforms of Supply Voltage, Load Voltage, and Uan. (A) V2 On/Off. (B) V1 On/Off.

The control strategy applied for voltage sags is in-phase compensation, so the energy needed to maintain the load voltage in one half-cycle can be expressed as follows:

$$E_0 = \frac{T_0 \Delta V}{2V_{\text{ref}}} P_0 \tag{1}$$

Where T0 is the grid voltage period time, Vref is the rated rms value of the load voltage, P0 is the rated load power, and ΔV is the rms value of the missing voltage. In steady-state compensation, the energy needed for the compensation should completely be provided by the residential grid which is also the charging energy through the parasitic boost circuit in this case. So the charging energy provided during T0/2 referred to as E1 equals to E0. E0 can be easily obtained according to (1), but the calculation ofE1 involves with the operating conditions shown in Fig. 3. The simplified circuit model of Fig. 3is illustrated in Fig. 6, where compensation loop including the filter and the load is ignored and only the charging circuit is considered.

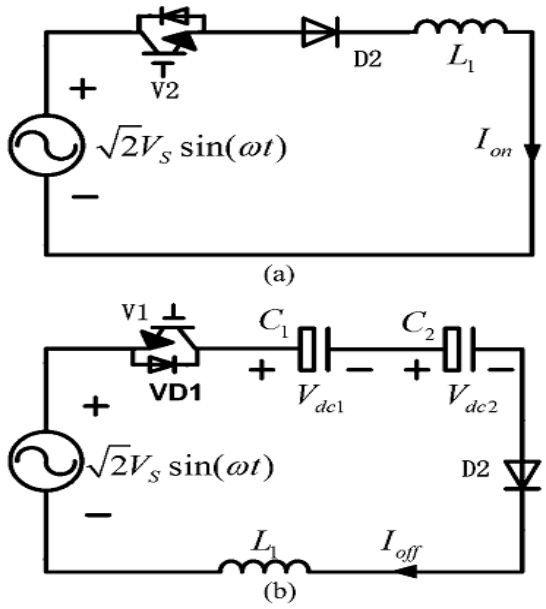

Fig.6. Simplified Circuit Model. (A) V2 Turned On. (B) V2 Turned Off.

In Fig. 6, VS is the rms value of the supply voltage. Two state equations can be obtained based on Fig. 6 and written as follows:

$$\begin{cases} L_1 \dfrac{dI_{\text{on}}}{dt} = \sqrt{2}V_S \sin(\omega t) \\ L_1 \dfrac{dI_{\text{off}}}{dt} = \sqrt{2}V_S \sin(\omega t) - V_{\text{dc1}} - V_{\text{dc2}}. \end{cases} \tag{2}$$

According to the analysis will be significantly simplified if some realistic approximations are carried out. Then (2) can be discredited into (3) based on two following assumptions: C1 and C2 are well designed so thatVdc1andVdc2can be regarded equal without considering their ripple voltages; the switching frequency is much higher than the line frequency that the supply voltage in the nth switching cycle can be treated as a constant value where t_{onn} and t_{offn} are, respectively, the turn-on and turn-off time of V2 in the nth switching cycle, Ts is the switching period, V_{dc} is the steady-state dc-link voltage, and ΔI_{onn} or ΔI_{offn} represents the variation amount in charging current during t_{onn} or t_{offn}.

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$$\begin{cases} L_1\Delta I_{\text{on}n} = \sqrt{2}V_S\sin(\omega nT_s)t_{\text{on}n} \\ L_1\Delta I_{\text{off}n} = [\sqrt{2}V_S\sin(\omega nT_s) - 2V_{\text{dc}}]t_{\text{off}n} \end{cases} \quad (3)$$

As the analysis is within the positive half-cycle of the grid, there exists a constraint: n≤T0/2Ts. Apparently, t_{onn} and t_{offn} here are actually the inverter's duty cycle and they can be expressed as (4) when two-level symmetric regular-sampled PWM method is adopted

$$\begin{cases} t_{\text{on}n} = \dfrac{T_s}{2}\left[1 + \dfrac{\sqrt{2}\Delta V\sin(\omega nT_s)}{V_{\text{dc}}}\right] \\ t_{\text{off}n} = \dfrac{T_s}{2}\left[1 - \dfrac{\sqrt{2}\Delta V\sin(\omega nT_s)}{V_{\text{dc}}}\right] \end{cases} \quad (4)$$

The recursion formula of the charging current at the end of the nth switching cycle can be obtained by combining (3) and (4)

$$I_{\text{off}n} = I_{\text{off}(n-1)} + \frac{T_s}{L_1}[\sqrt{2}V_{\text{ref}}\sin(\omega nT_s) - V_{\text{dc}}] \quad (5)$$

Where I_{offn} represents the charging current instantaneous value at the end of the n^{th} switching cycle and ΔI_{onn} can be derived at the same time

$$\Delta I_{\text{on}n} = \frac{\sqrt{2}T_sV_S\sin(\omega nT_s)}{2L_1}\left[1 + \frac{\sqrt{2}\Delta V\sin(\omega nT_s)}{V_{\text{dc}}}\right] \quad (6)$$

The energy stored in an inductor is related to the current that flows through it, so the charging energy provided by the grid via the parasitic boost circuit in the n^{th} switching cycle can be expressed and then rearranged as follows:

$$E_{\text{in}n} = \frac{1}{2}L_1\Delta I_{\text{on}n}^2 + L_1I_{\text{off}(n-1)}\Delta I_{\text{on}n} \quad (7)$$

$I_{off(n-1)}$ in (7) can be superimposed according to the recursion formula shown in (5). Before the expression is given, there are some features about the charging current should be clarified: 1) the value of the charging current cannot be lower than zero as the current flowing through a diode is unidirectional; 2) the value of the charging current can either be zero or nonzero and its value always decreases after increasing in one half-cycle of the sinusoidal grid voltage. Then, the nonzero terms of the charging current can be derived as follows:

$$I_{\text{off}(n-1)} = \sum_{k=n_0}^{n-1}\frac{T_s}{L_1}\left[\sqrt{2}V_{\text{ref}}\sin(\omega kT_s) - V_{\text{dc}}\right] \quad (8)$$

Where n_0 is the initial superposition instant and I_{offn} is always equal to zero when n is smaller thann0. So, n0 can be calculated according to (5) and expressed as follows:

$$n_0 = \text{ceil}\left(\frac{T_0\arcsin\frac{V_{\text{dc}}}{V_{\text{ref}}}}{2\pi T_s}\right) \quad (9)$$

Where ceil(•) represents the rounded up function and the arcsine function here ranges from 0 to π/2. Furthermore, when the charging current calculated by (8) decreases to the value no more than zero, n will reach its upper limit denoted byne. Substituting (6), (8), and (9) into (7), the energy provided by the supply in the nth switching cycle can be written as follows:

$$E_{\text{in}n} = \frac{T_s^2V_S^2A^2}{4L_1}(1+\sqrt{2}BA)^2 + \frac{\sqrt{2}T_S^2V_SA}{2L_1V_{\text{dc}}} \times (V_{\text{dc}} + \sqrt{2}\Delta VA)\sum_{k=n_0}^{n-1}(\sqrt{2}V_{\text{ref}}C - V_{\text{dc}}) \quad (10)$$

Where

$$A = \sin\omega nT_s$$

$$B = \frac{\Delta V}{V_{\text{dc}}}$$

$$C = \sin\omega kT_s$$

E1 now can be obtained if (10) is added with n ranging from 1to T0/2Ts. So, the overall energy balance equation can be written as follows:

$$E_1 = \frac{T_s^2V_S^2}{4L_1}\left(\sum_{n=1}^{\frac{T_0}{2T_s}}A^2 + 2\sqrt{2}B\sum_{n=1}^{\frac{T_0}{2T_s}}A^3 + 2B^2\sum_{n=1}^{\frac{T_0}{2T_s}}A^4\right) + \frac{T_s^2\sqrt{2}V_S}{2L_1}\sum_{n=n_0}^{n_e}\left[(A+\sqrt{2}BA^2)\sum_{k=n_0}^{n-1}(\sqrt{2}V_{\text{ref}}C - V_{\text{dc}})\right] = \frac{T_0\Delta V}{2V_{\text{ref}}}P_0 = E_0 \quad (11)$$

The charging current peak value I_{max} is considered to arise at the switching cycle after the value of (8) reaches its upper limit. So I_{max} is expressed as follows:

$$I_{\max} = \frac{\sqrt{2}T_sV_S\sin(\omega n_{\max}T_s)}{2L_1}[1+\sqrt{2}B\sin(\omega n_{\max}T_s)] + \sum_{n=n_0}^{n_{\max}}\frac{T_s}{L_1}(\sqrt{2}V_{\text{ref}}C - V_{\text{dc}}) \quad (12)$$

Where n_{max} is the switching cycle when I_{offn} reaches its maximum value and n_{max} can be written as follows:

$$n_{\max} = \text{ceil}\left[\frac{T_0(\pi - \arcsin\frac{V_{\text{dc}}}{V_{\text{ref}}})}{2\pi T_s}\right] \quad (13)$$

So far, the main features of the SPB-AVQR topology can be described by (11) and (12). As shown in (11), the dc-link voltage is not only related to the supply voltage, but also associated with the charging inductance, load active

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p-ISSN: 2348-6848
e-ISSN: 2348-795X
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power, and switching frequency. However, the dc-link voltage cannot be obtained directly from (11) asn0andnecannot be computed with unknown dc-link voltage. So, an iterative algorithm is applied to estimate the dc-link voltage, where Ts, VS, T0, Vref, L1, and P0 are all treated as constants. A flow chart of the adopted calculating method is illustrated in Fig. 7, whereVdc0is the initial value for V_{dc} and ΔV_{dc} is the iterative step. The algorithm is terminated if the error betweenE0andE1is smaller than the error tolerance ε. Moreover, the charging current can be calculated by (12) and (13) as long as V_{dc} is obtained

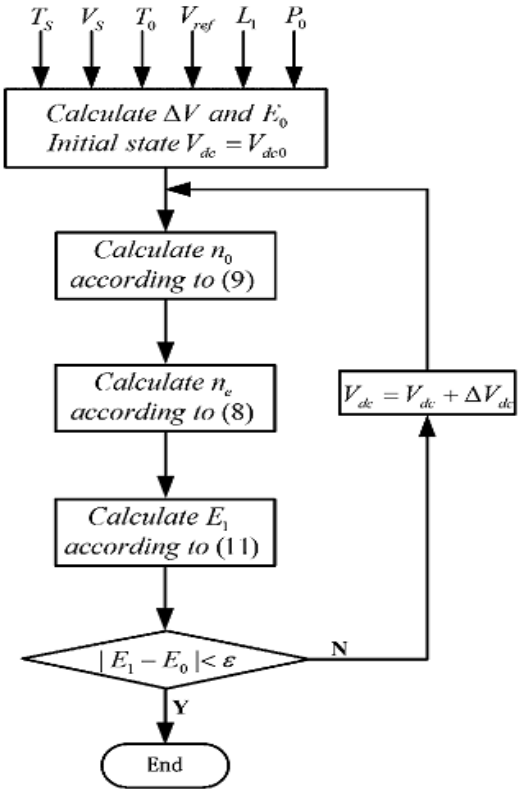

Fig.8. Flow chart for calculating V_{dc}.

It presents that the steady-state charging current peak value increases with the decreasing of the supply voltage and it can be suppressed by increasing the charging inductance. Although conclusions drawn from the theoretical analysis for the SPB-AVQR can also be applied to the proposed PB-AVQR topology, there still exist some differences in their dc-link voltages. When the proposed PB-AVQR is discussed, the trigger pulse angle α for VT3 and VT4 should also be taken into consideration. In the PB-AVQR circuit, the charging process begins after the VT3 or VT4 is triggered, so the initial superposition instant n0 in (11) is now determined by α denoted byn1 and the energy balance equation is written as follows:

$$\frac{T_s^2 V_S^2}{4L_1}\left(\sum_{n=n_1}^{n_e} A^2 + 2\sqrt{2}B\sum_{n=n_1}^{n_e} A^3 + 2B^2\sum_{n=n_1}^{n_e} A^4\right) + \frac{T_s^2\sqrt{2}V_S}{2L_1}\sum_{n=n_1}^{n_e}\left[(A+\sqrt{2}BA^2)\sum_{k=n_1}^{n-1}(\sqrt{2}V_{\mathrm{ref}}C - V_{\mathrm{dc}})\right] = \frac{T_0\Delta V}{2V_{\mathrm{ref}}}P_0 \quad (14)$$

Here, ne is still determined by (8) as aforementioned and $n_1$can be derived as follows:

$$n_1 = \mathrm{ceil}\left(\frac{\alpha T_0}{2\pi T_s}\right) \quad (15)$$

Furthermore, the thyristors are triggered only once in each half-cycle and the current through them should be higher than the holding current to maintain the triggered state. So, α is required to meet the constraint expressed as follows:

$$\sqrt{2}V_{\mathrm{ref}}\sin\alpha > V_{\mathrm{dc}} \quad (16)$$

The charging current peak value of the PB-AVQR can still be described by (12) as long asn0is substituted withn1. As can be seen from (14) and (15), the trigger pulse of the PB-AVQR will certainly affect its dc-link voltage and charging current.

IV.MATLAB/SIMULINK RESULTS

Here simulation is carried out in several load conditions, in that 1) Implementation of DySC topology 2) Proposed Active Voltage Quality Regulator Topology, 3) Proposed Active Voltage Quality Regulator Topology with Non-Linear Load, 4) Proposed Active Voltage Quality Regulator Topology with Closed Loop Controller.

Case 1: Implementation of DySC Topology

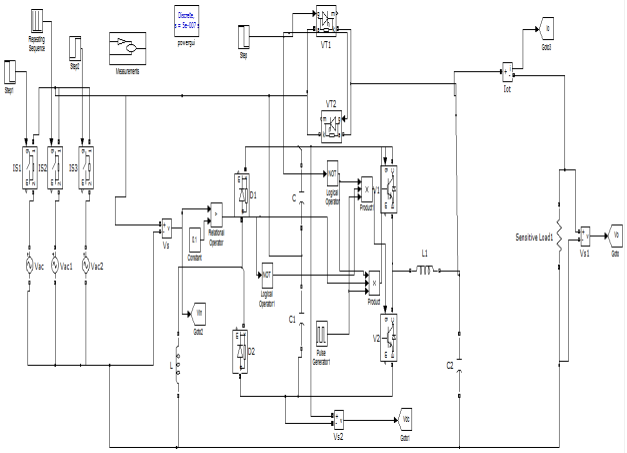

Fig.9 Matlab/Simulink Model of DySC Topology by using Matlab/Simulink platform.

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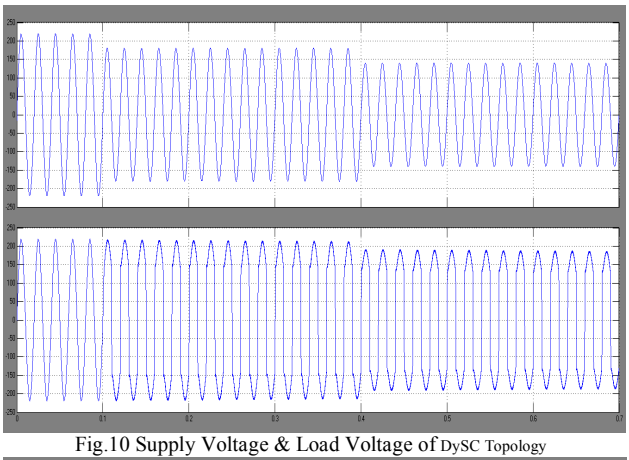


Fig.10 Supply Voltage & Load Voltage of DySC Topology

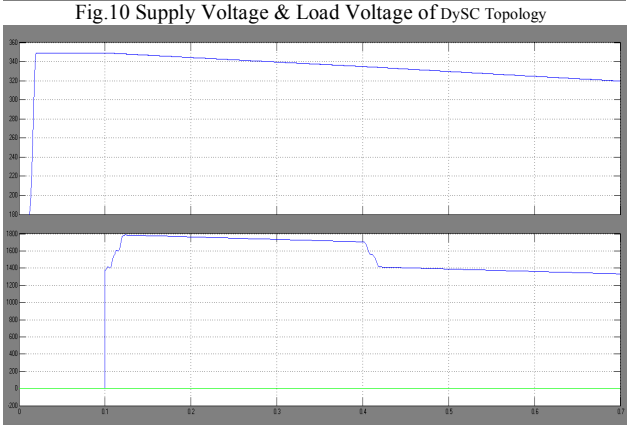


Fig.11 DC Link Voltage & Active, Reactive Power.

Fig. 10 shows the simulation results of the DySC topology voltage drops to 180 V at 0.1 s and then falls to 100 V at 0.4 s, when the supply voltage is 180V, the DySC can effectively compensate for the voltage sag; however, when the supply voltage drops to 100 V, the load voltage becomes not sinusoidal as the maximum injected compensation voltage is limited by the low steady-state dc-link voltage. Fig. 11 also indicates that the DySC can only mitigate deep sags for a few line cycles depending on the energy stored in dc-link capacitors as its steady-state dc-link voltage is always lower than the peak value of the supply voltage.

Case 2: Proposed Active Voltage Quality Regulator Topology

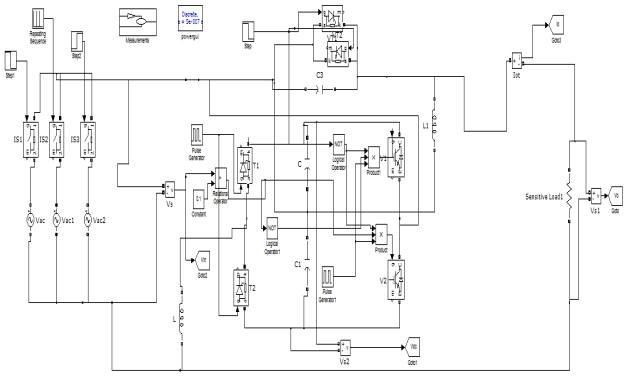
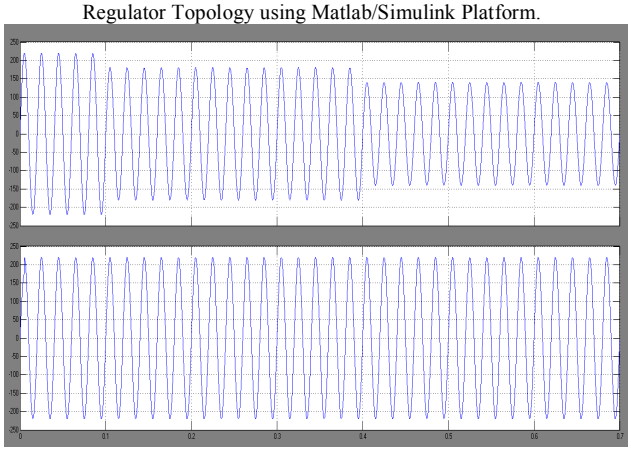
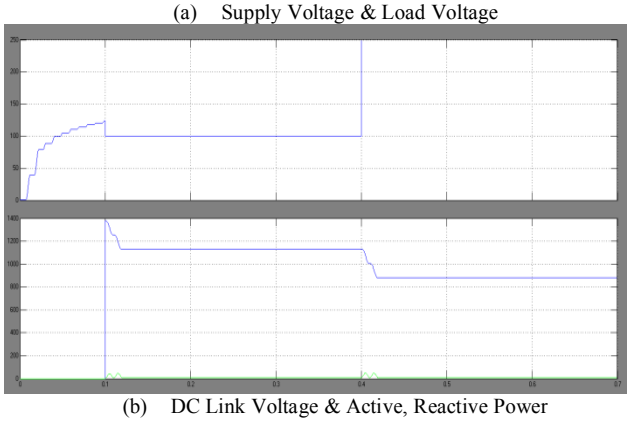


Fig.12 Matlab/Simulink Model of Proposed Active Voltage Quality Regulator Topology using Matlab/Simulink Platform.



(a) Supply Voltage & Load Voltage



(b) DC Link Voltage & Active, Reactive Power

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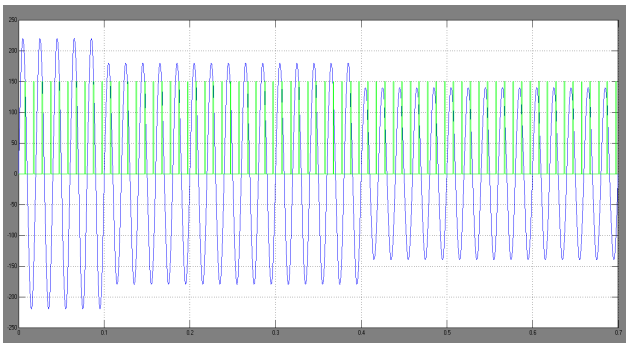
Volume 03 Issue 13
September 2016



(c) Input Voltage & Switching States

Fig.13 (a) Supply Voltage & Load Voltage, (b) DC Link Voltage & P-Q Power, (c) Input Voltage & Switching States of Proposed Active Voltage Quality Regulator Topology.

Case 3: Proposed Active Voltage Quality Regulator Topology with Non-Linear Load

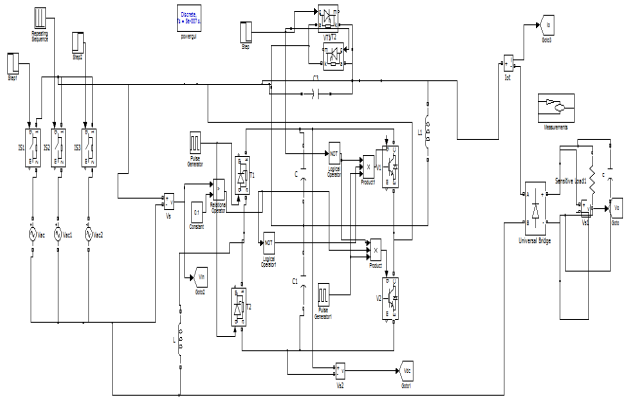


Fig.14 Matlab/Simulink model of Proposed Active Voltage Quality Regulator Topology with Non-Linear Load using Matlab/Simulink platform.

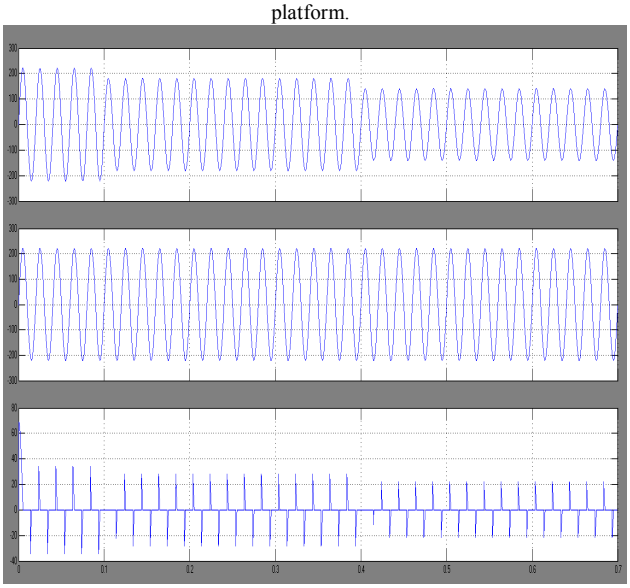


Fig.15 Input Voltage, Output Voltage, Input Current of Proposed Active Voltage Quality Regulator Topology with Non-Linear Load, due to non-linear diode bridge rectifier load attains the non-linear characteristics of voltage & current.

Case 4: Proposed Active Voltage Quality Regulator Topology with Closed Loop Controller

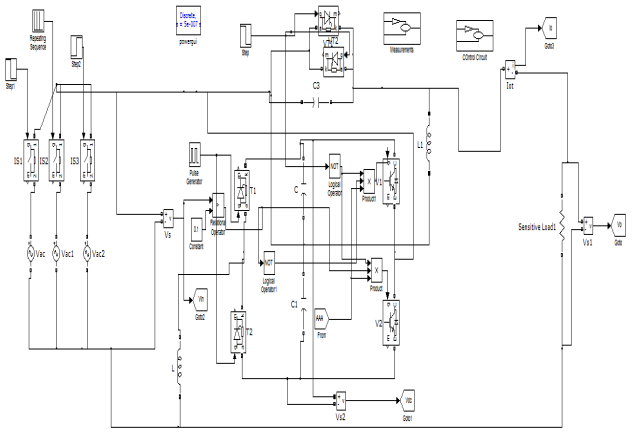
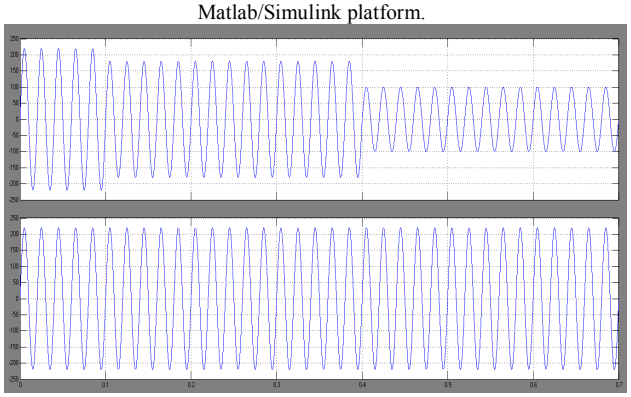
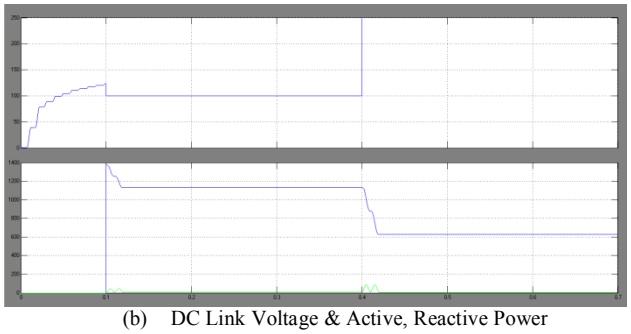


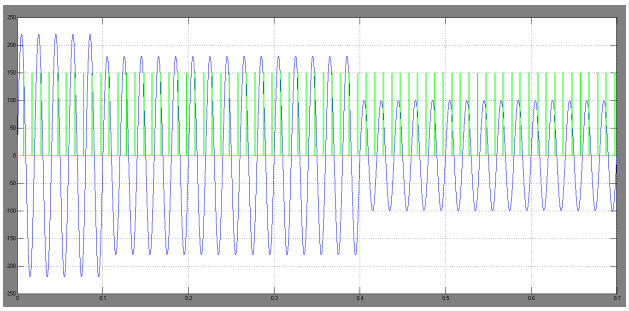
Fig.16 Matlab/Simulink Model of Proposed Active Voltage Quality Regulator Topology with Closed Loop Controller using Matlab/Simulink platform.



(a) Supply Voltage & Load Voltage



(b) DC Link Voltage & Active, Reactive Power



(c) Input Voltage & Switching States

Fig.17 (a) Supply Voltage & Load Voltage, (b) DC Link Voltage & P-Q Power, (c) Input Voltage & Switching States of Proposed Active Voltage Quality Regulator Topology under Closed-Loop Condition.

V.CONCLUSION

This paper has presented a novel transformer less active voltage quality regulator with parasitic boost circuit operates under closed loop condition to mitigate long duration deep voltage sags with good stability factor and low error components. The proposed PB-AVQR topology is derived from the DySC circuit and the compensation performance is highly improved without increasing the cost, weight, volume, and complexity. The feasibility and effectiveness of the proposed topology in the compensation for long duration deep voltage sags that are lower than half of its rated value. The operating efficiency of the proposed PB-AVQR system also remains at a relatively high level as the dc-link voltage adaptive control method is adopted. In a conclusion, the proposed PB-AVQR topology in this paper provides a novel solution for long duration deep voltage sags with great reliability and compensation performance.

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