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Model Predictive Decoupled Active and ReactivePower Control for High-Power Grid-ConnectedFour-Level Diode-Clamped Inverters

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Abstract:

In this paper, a model predictive scheme is proposed to control the grid-connected high-power four-level diode-clamped inverter. To predict the future behavior of active and reactive grid power values and dc link capacitor voltages, a discrete-time model of the inverter is developed in synchronous reference frame. The controller uses all the possible switching states of the inverter for the prediction and evaluates them using a cost function. The switching state, which minimizes the cost function, is then chosen and applied at the next sampling interval. The switching frequency minimization is also achieved by including an extra constraint in the cost function. A simplified extrapolation method with reduced computational burden is proposed to safeguard the semiconductor devices during the dynamic changes in reference power values. The performance of the proposed method is investigated with the perturbations in the grid filter and dc link parameters. The feasibility of the proposed method is verified through simulation and experimental results, showing good dynamic and steady-state performance. .

Keywords

DC–AC power conversion, model predictive control (MPC), multilevel converters, power control, and wind energy.

1. Introduction

Installed wind energy capacity has been exponentially increasing over the last few years. Meanwhile, the size of megawatt (MW) wind turbines has steadily increased. Currently, 7.5-MW wind turbines are available in the market, and 10–15-MW turbines are anticipated in the near future [1]. At this high power level, the use of low-voltage (LV) converters is not an appropriate solution. For instance, a 7.5 MW/ 690 V turbine requires a parallel connection of 10 two-level converters, each rated at 750 kW/690 V and bulky cables (due to high line current of 6276 A) to carry power from the nacelle to the bottom of the tower. These cables increase the cost to the turbine and decrease the efficiency of the whole system due to high power loss (I2R) in the cable [2]. These technical and economic issues have motivated wind turbine manufacturers to use medium-voltage (MV) converters at high power levels [1]–[3]. Unlike the MV drives that are fed by standard utility voltages of 2.3, 3.3, 4.16, 6, 6.6, 6.9, 7.2, 10, 11, and 13.8 kV, there is no such standard for wind turbines. Current commercial wind turbines are rated at 3–4 kV rating, and with the increasing power levels, it is expected that the voltage rating may increase further.

The three-level converter has been widely studied in literature [2], [4], [5], but the application of diode-clamped converters with higher (four or more) levels has not been analyzed for the production of wind power. This paper proposes a four-level diode-clamped inverter for the grid connection of MV-MW wind energy conversion systems (WECSs). For a given filter size, better power quality and grid code compliance can be achieved due to the increased equivalent converter switching frequency. The converter can be operated at higher levels of voltage without connecting the switching devices in series.

The voltage-oriented control (VOC) [3], [6] is a popular classical control scheme adopted by the wind energy industry. To apply this technique to a four-level inverter, properly tuned synchronous reference frame (SRF) PI controller, complex modulation [pulse width modulation (PWM) or space-vector modulation (SVM)] [7], and dc link capacitor voltage control are necessary. Moreover, the grid voltage

harmonics and control delay will degrade the performance of the PWM/SVM-based controller [8].

In recent years, the finite-control set model predictive control (FCS-MPC) has found many applications in power electronics [9]–[15]. This method is simple and completely eliminates the need for PI controllers and modulation stage. A preliminary simulation study has been done by Cortes et al. for the predictive current control of four-level inverters with resistive load [16]. In this paper, the FCS-MPC concept is extended for the high-power MV-WECS. The proposed control scheme controls the active and reactive grid power values and dc link capacitor voltages by selecting the best one among the 64 possible switching states.

To increase the reliability of the semiconductor switches, the switching frequency is minimized and maintained below 1 kHz by properly choosing the sampling frequency and weighting factor for the cost function. During step change in reference power values, the vector angle extrapolation [17] exhibits better performance than the Lagrange extrapolation method [13], [14], [18]; however, it is not suitable for the SRF references. In this paper, a simplified extrapolation method is proposed in SRF, and this will eliminate the voltage spikes during the step change in reference power values. The performance of the proposed controller with the grid filter and dc link parameter variations is also studied. To validate the proposed method, simulations are carried out on a high-power (4 MVA/4 kV) system using MATLAB/Simulink software and then experimentally verified on a low-power prototype (5 kW/208 V) using a dSPACE DS1103 controller.

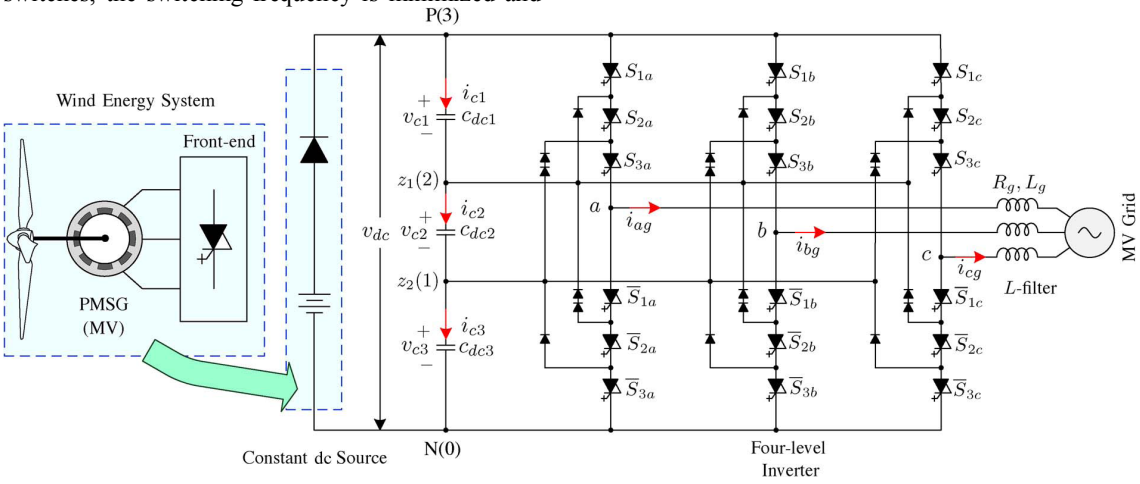

Fig. 1. Topology of grid-connected four-level diode-clamped inverter

TABLE I
SWITCHING STATES AND INVERTER TERMINAL VOLTAGES ($x = a, b, c$)

S_x	S_{1x}	S_{2x}	S_{3x}	$\overline{S}_{1x}$	$\overline{S}_{2x}$	$\overline{S}_{3x}$	v_{xN}
3	1	1	1	0	0	0	$v_{c3} + v_{c2} + v_{c1}$
2	0	1	1	1	0	0	$v_{c3} + v_{c2}$
1	0	0	1	1	1	0	v_{c3}
0	0	0	0	1	1	1	0

This paper is organized as follows. In Section II, the modelling of inverter and dc link is presented in SRF, followed by the proposed control strategy in Section III. The simulation and experimental results are discussed in Sections IV and V, respectively, and finally, conclusions are given in Section VI.

2. Grid-Connected Four-Level Inverter Model

The configuration of grid-connected four-level diode clamped inverter is shown in Fig. 1. The MV permanent magnet synchronous-generator (PMSG)-based WECS, along with the front-end rectifier, is replaced by a constant dc voltage source. The inverter is connected to the MV grid through an Inductive L filter. In this paper, active power, reactive power, and dc link capacitor voltages are considered to be controlled by the inverter, whereas the net dc link voltage is controlled by the rectifier. The inverter terminal voltages with respect to the switching states are given in Table I [16]. A total of 37 voltage vectors with 64 (43) switching combinations are available for this inverter. In order to achieve decoupled control for the grid active and reactive power values, the modeling is performed in SRF. Thread-axis of the SRF is aligned with the grid voltage vector, and as a result, q-axis grid voltage becomes zero [3]. With this process, the grid active and reactive power values can be calculated as

$$\left.\begin{aligned} P_g &= \tfrac{3}{2}(v_{dg}\, i_{dg} + v_{qg}\, i_{qg}) = +\tfrac{3}{2} v_{dg}\, i_{dg} \\ Q_g &= \tfrac{3}{2}(v_{qg}\, i_{dg} - v_{dg}\, i_{qg}) = -\tfrac{3}{2} v_{dg}\, i_{qg} \end{aligned}\right\}, \qquad v_{qg} = 0. \tag{1}$$

The grid currents can be expressed in SRF in terms of inverter voltages, grid voltages, and filter parameters. This is demonstrated as [6]

$$\frac{d}{dt}\begin{bmatrix} i_{dg} \\ i_{qg} \end{bmatrix} = \mathrm{A}\begin{bmatrix} i_{dg} \\ i_{qg} \end{bmatrix} + \mathrm{B_i}\begin{bmatrix} v_{di} \\ v_{qi} \end{bmatrix} + \mathrm{B_g}\begin{bmatrix} v_{dg} \\ v_{qg} \end{bmatrix} \tag{2}$$

where

$$\mathrm{A} = \begin{bmatrix} \frac{-R_g}{L_g} & \omega_g \\ -\omega_g & \frac{-R_g}{L_g} \end{bmatrix} \mathrm{B_i} = \begin{bmatrix} \frac{1}{L_g} & 0 \\ 0 & \frac{1}{L_g} \end{bmatrix} \mathrm{B_g} = \begin{bmatrix} \frac{-1}{L_g} & 0 \\ 0 & \frac{-1}{L_g} \end{bmatrix} \tag{3}$$

Where Lg is the grid filter inductance, and Rg is the internal resistance of the inductor. vdi, vqi, vdg, and vqg are d- and q-axis inverter and grid voltages, respectively.

As expressed below, the inverter voltages can be obtained from the switching signals and dc link capacitor voltages

$$\left.\begin{aligned} v_{aN} &= v_{c1} S_{1a} + v_{c2} S_{2a} + v_{c3} S_{3a} \\ v_{bN} &= v_{c1} S_{1b} + v_{c2} S_{2b} + v_{c3} S_{3b} \\ v_{cN} &= v_{c1} S_{1c} + v_{c2} S_{2c} + v_{c3} S_{3c} \end{aligned}\right\}. \tag{4}$$

The above natural frame (abc) inverter voltages can be Converted to synchronous frame (dq) as

$$\begin{bmatrix} v_{di} \\ v_{qi} \end{bmatrix} = \frac{2}{3}\begin{bmatrix} \cos\theta_g & \cos\left(\theta_g - \frac{2\pi}{3}\right) & \cos\left(\theta_g - \frac{4\pi}{3}\right) \\ -\sin\theta_g & -\sin\left(\theta_g - \frac{2\pi}{3}\right) & -\sin\left(\theta_g - \frac{4\pi}{3}\right) \end{bmatrix}\begin{bmatrix} v_{aN} \\ v_{bN} \\ v_{cN} \end{bmatrix} \tag{5}$$

Where θg is grid voltage angle, which can be obtained by an SRF phase-locked loop (PLL) [6].

The dc link capacitor voltages can be expressed in terms of dc link capacitor currents as follows [19]:

$$\left.\begin{aligned} v_{c1}(t) &= v_{c1}(0) + \tfrac{1}{C_{\mathrm{dc1}}} \int_{0+}^{t} i_{c1}(\tau)\, d\tau \\ v_{c2}(t) &= v_{c2}(0) + \tfrac{1}{C_{\mathrm{dc2}}} \int_{0+}^{t} i_{c2}(\tau)\, d\tau \\ v_{c3}(t) &= v_{c3}(0) + \tfrac{1}{C_{\mathrm{dc3}}} \int_{0+}^{t} i_{c3}(\tau)\, d\tau \end{aligned}\right\}. \tag{6}$$

The capacitor currents (i.e., ic1, ic2, and ic3) can be estimated from the grid currents (i.e., iag, ibg, and icg), and thus, there is no need to measure them. This is demonstrated by

$$\begin{aligned} i_{c1} &= K_{1d}\, i_{dg} + K_{1q}\, i_{qg} \\ i_{c2} &= K_{2d}\, i_{dg} + K_{2q}\, i_{qg} \\ i_{c3} &= K_{3d}\, i_{dg} + K_{3q}\, i_{qg} \end{aligned} \tag{7}$$

Where K1d, K1q, K2d, K2q, K3d, and K3q are variables in SRF, and they can be obtained from natural frame gains and grid voltage angle θg. It should be noted that the capacitor currents are mean values. The natural frame gains can expressed in terms of switching states as follows:

$$\left.\begin{aligned} K_{1x} &= \mathrm{sgn}(3 - S_x) \\ K_{2x} &= \mathrm{sgn}(2 - S_x) \\ K_{3x} &= \mathrm{sgn}(1 - S_x) \end{aligned}\right\}, \qquad x = a, b, c \tag{8}$$

Where K1x, K2x, K3x ∈ {−1, 0, 1}, and sgn is a signum function. The modeling of dc link voltages in SRF gives flexibility in digital implementation. This will be further discussed in Section VI.

From (1)–(8), it can be understood that the grid active and reactive power values and dc link capacitor voltages are related to the switching signals, and they can be controlled with an appropriate selection of switching state.

3. PROPOSED CONTROL STRATEGY

The proposed MPC scheme is shown in Fig. 2, where the wind turbine, generator, and rectifier with the total dc link voltage control are represented by a battery in series with a diode. The reference reactive power command (Q∗ g) is provided by the grid operator, and this can be set to zero for unity, negative for leading, and positive for the lagging power factor. The active power reference P∗ g is

obtained by the maximum power point tracking (MPPT) algorithm. In commercial wind turbines, the MPPT is performed using the wind turbine characteristics and measured (using anemometer) wind speed. To simplify the analysis, the per-unit P∗ g is considered to be a cubic of per-unit wind speed [3]

$$\text{p.u. } P_g^*(k) \propto \text{p.u. } v_w^3(k). \tag{9}$$

The grid voltage and current vectors are defined as follows:

$$\left.\begin{aligned} \mathbf{v_g^m} &= [v_{ag}^m \quad v_{bg}^m \quad v_{cg}^m]^T \\ \mathbf{i_g^m} &= [i_{ag}^m \quad i_{bg}^m \quad i_{cg}^m]^T \end{aligned}\right\} \tag{10}$$

Where superscript m denotes the measured quantity.

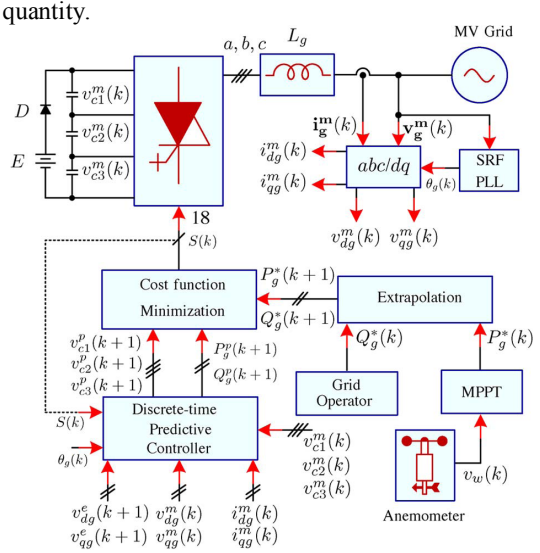

Fig. 2. Proposed predictive power control and dc link capacitor voltage balancing scheme for a grid-connected four-level inverter.

The discrete-time model for the grid active and reactive power values can be obtained from (1) for one-step horizon time (k + 1), as demonstrated below

$$\left.\begin{aligned} P_g^p(k+1) &= \tfrac{3}{2}[v_{dg}^e(k+1)\, i_{dg}^p(k+1) \\ Q_g^p(k+1) &= \tfrac{3}{2}[v_{dg}^e(k+1)\, i_{qg}^p(k+1) \end{aligned}\right\} \tag{11}$$

Where superscripts p and e denote the predicted and extrapolated quantities.

For a stiff grid, vedg (k + 1) = vmdg (k), and thus, no extrapolation is needed. For weak grids, the following fourth-order Lagrange extrapolation method can be used [13], [14], [18]:

$$v_{dg}^e(k+1) = 4v_{dg}^m(k) - 6v_{dg}^m(k-1) + 4v_{dg}^m(k-2) - v_{dg}^m(k-3). \tag{12}$$

The discrete-time future dq-axis grid currents can be obtained from (2) for the one-step prediction horizon as follows:

$$\begin{bmatrix} i_{dg}^p(k+1) \\ i_{qg}^p(k+1) \end{bmatrix} = \mathbf{\Phi} \begin{bmatrix} i_{dg}^m(k) \\ i_{qg}^m(k) \end{bmatrix} + \mathbf{\Gamma_i} \begin{bmatrix} v_{di}^p(k+1) \\ v_{qi}^p(k+1) \end{bmatrix} + \mathbf{\Gamma_g} \begin{bmatrix} v_{dg}^m(k) \\ v_{qg}^m(k) \end{bmatrix} \tag{13}$$

Where vpdi(k + 1) and vpqi(k + 1) are the predicted inverter voltages in (k + 1) state using the 64 possible switching states. Φ, Γi, and Γg are discrete-time parameter matrices, which can be computed offline as shown below

$$\left.\begin{aligned} \mathbf{\Phi} &= e^{\mathbf{A}T_s} \\ \mathbf{\Gamma_i} &= \mathbf{A}^{-1}(\mathbf{\Phi} - \mathbf{I_{2x2}})\mathbf{B_i} \\ \mathbf{\Gamma_g} &= \mathbf{A}^{-1}(\mathbf{\Phi} - \mathbf{I_{2x2}})\mathbf{B_g} \end{aligned}\right\}. \tag{14}$$

TABLE II
CALCULATION OF NUMBER OF SWITCH CHANGES ($x = a, b, c$)

swc_x	$S_x(k+1)$			
	3	**2**	**1**	**0**
$S_x(k_{op}) = \mathbf{3}$	0	2	4	6
$S_x(k_{op}) = \mathbf{2}$	2	0	2	4
$S_x(k_{op}) = \mathbf{1}$	4	2	0	2
$S_x(k_{op}) = \mathbf{0}$	6	4	2	0

The discrete-time model for dc link voltages can be obtained from (6) as

$$\left.\begin{aligned} v_{c1}^p(k+1) &= v_{c1}^m(k) + \tfrac{T_s}{C_{dc1}}\, i_{c1}^p(k+1) \\ v_{c2}^p(k+1) &= v_{c2}^m(k) + \tfrac{T_s}{C_{dc2}}\, i_{c2}^p(k+1) \\ v_{c3}^p(k+1) &= v_{c3}^m(k) + \tfrac{T_s}{C_{dc3}}\, i_{c3}^p(k+1) \end{aligned}\right\} \tag{15}$$

where ipc1(k + 1), ipc2(k + 1), and ip c3(k + 1) are predicted dc link currents, which can be obtained from (7) and (8). The control objectives such as regulation of active and reactive power values, dc link capacitor voltage balancing, and switching frequency minimization are included in a cost function as follows:

$$g(k+1) = \left\|P_g^*(k+1) - P_g^p(k+1)\right\| + \left\|Q_g^*(k+1) - Q_g^p(k+1)\right\| + \lambda_{dc} * \left(\left[v_{c1}^p(k+1) - v_{c2}^p(k+1)\right]^2 + \left[v_{c2}^p(k+1) - v_{c3}^p(k+1)\right]^2 + \left[v_{c3}^p(k+1) - v_{c1}^p(k+1)\right]^2 \right) + \lambda_{swc} * (swc_a + swc_b + swc_c) \quad (16)$$

Where λdc and λswc are weighting factors for the capacitor volt- age balancing and switching frequency reduction, respectively. swcx is the number of semiconductor commutations involved in phase-x, which can be calculated, as shown in Table II.

In this paper, sampling time of 100 μs is used to deal with the 64 switching states. At this higher sampling time, the reference power values should be extrapolated to the (k + 1) state for high-performance control. Since the reference power values are dc quantities, no extrapolation is needed during steady-state operation. In practical WECS, the wind speed, and thus the active power reference, dynamically changes; as a result, an extrapolation method should be used.

The Lagrange extrapolation [13], [14], [18] can be used. However, this method produces unnecessary spikes during the step changes. The vector angle extrapolation method overcomes this issue [17]. However, this method is based on real and imaginary (stationary frame, α, β) quantities. To use the vector angle extrapolation to manage active and reactive power values, the following procedure should be used.

1) Estimate $i_{dg}^*(k)$ and $i_{qg}^*(k)$ from $P_g^*(k)$ and $Q_g^*(k)$ using (1).
2) Estimate $i_{\alpha g}^*(k)$ and $i_{\beta g}^*(k)$ from $i_{dg}^*(k)$ and $i_{qg}^*(k)$.
3) Extrapolate $i_{\alpha g}^*(k)$ and $i_{\beta g}^*(k)$ to $i_{\alpha g}^*(k+1)$ and $i_{\beta g}^*(k+1)$ using vector angle method.
4) Estimate $i_{dg}^*(k+1)$ and $i_{qg}^*(k+1)$ from $i_{\alpha g}^*(k+1)$ and $i_{\beta g}^*(k+1)$.
5) Estimate $P_g^*(k+1)$ and $Q_g^*(k+1)$ from $i_{dg}^*(k+1)$ and $i_{qg}^*(k+1)$ using (1).

As shown in this example, it is a complex approach and increases the computational burden. To overcome this issue, a simplified extrapolation method is proposed. Since the reference active and reactive power values are of dc quantities, they can be simply extrapolated to the (k + 1) state as follows:

$$\left.\begin{aligned} P_g^*(k+1) &= P_g^*(k-1) \\ Q_g^*(k+1) &= Q_g^*(k-1) \end{aligned}\right\}. \quad (17)$$

For the purpose of comparison, the Lagrange extrapolation method [18] is given as follows:

$$P_g^*(k+1) = 4P_g^*(k) - 6P_g^*(k-1) + 4P_g^*(k-2) - P_g^*(k-3) \quad (18)$$

$$Q_g^*(k+1) = 4Q_g^*(k) - 6Q_g^*(k-1) + 4Q_g^*(k-2) - Q_g^*(k-3). \quad (19)$$

Compared with the Lagrange extrapolation, the proposed approach uses only one past value, which can be simply implemented using the "Variable Time Delay" block in the MATLAB/Simulink environment. This approach gives the same result as the vector angle extrapolation but with a less computational burden, particularly in SRF.

4. SIMULATION RESULTS

To validate the proposed control scheme, simulations are carried out with a one-step prediction horizon using MATLAB/ Simulink software with the parameters as indicated in Table V (see the Appendix). The dc link diode (D) is assumed to be ideal with the zero forward voltage drop. Unless otherwise stated, the cost function includes all the four variables men- tioned in (16).

In order to assess the performance of the proposed control scheme, the following parameters are defined as per the guide- lines given in [9], [13], and [14]: percentage mean absolute active power tracking error %epg, percentage mean absolute reactive power tracking error %eqg, percentage mean abso- lute dc link capacitor voltages deviation %evc, percentage total harmonic distortion %THD, and average device switching frequency fsw.

The simulation results with different active and reactive power references are shown in Fig. 3. The wind speed vw profile is shown in Fig. 3(a), where it linearly increases from a cut-in wind speed of 3 m/s (0.25 p.u.) and reaches the rated value of 12 m/s (1 p.u.) at 0.6 s. A step change in wind speed from 12 to 10.12 m/s (0.8434 p.u.) is applied at 0.8 s. The reference active power P∗ g and measured active power Pg are shown in Fig. 3(b). P∗g is proportional to the wind speed and changes from 4 MW (1 p.u.) to 2.4 MW (0.6 p.u.) at 0.8 s. The active power tracks to its reference very well during the transient and steady- statecondition. The reference and grid reactive power values, i.e., Q∗g and Qg, respectively, are depicted in Fig. 3(c). A step change in Q∗ g from 0 to 1.2 Mvar (0.3 p.u.) is applied at 1.0. At

TABLE III
STEADY-STATE ANALYSIS WITH SIMULATION RESULTS

Case	P_g^*(pu)	Q_g^*(pu)	$\%e_{pg}$	$\%e_{qg}$	$\%e_{vc}$	%THD	f_{sw}(Hz)
SS1	1.0	0	4.90	1.63	0.45	3.41	854
SS2	0.6	0	3.91	1.37	0.75	4.80	886
SS3	0.6	0.3	4.85	2.98	0.66	5.36	776
SS4	0.6	−0.7	3.45	3.20	0.38	3.29	991

t = 1.5 s, another step change in Q∗g is applied from 0 to−2.8 Mvar (−0.7 p.u.). During time intervals 1–1.3 s and 1.5–1.8 s, grid apparent power Sg is found to be 2.6833 MVA (0.671 p.u.) and 3.6878 MVA (0.922 p.u.), respectively. Thephase-a grid current iag magnitude is proportional to Sg, as shown in Fig. 3(d). The total dc link voltage vdc is maintained at its reference value by the battery supply, as shown in Fig. 3(e). In addition, as demonstrated in Fig. 3(f), perfect balancing of the dc link capacitor voltages has been achieved during different active and reactive power references. From these results, it can be established that the grid active and reactive power values can be controlled in a decoupled manner, similar to the classical control schemes, but with a simpler approach.

The performance of the proposed controller during four steady-state operating conditions (as shown in Fig. 3) is sum- marized in Table III. Reference tracking errors epg and eqg are maintained below 5%, and thus, they validate the reference tracking term defined in the cost function. The capacitor volt- ages are well balanced with an error magnitude of less than 1%. This facilitates the reduced voltage stress on the semiconductor switches. The THD is maintained below 5% except for SS3, where the switching frequency is much lower (776 Hz) than the other operating conditions. The switching frequency is maintained below 1 kHz, and this enhances the reliability of the semiconductor switches.The proposed predictive control method is compared with the classical decoupled VOC [3] in steady state, and the results are presented in Figs. 4–6. The active and reactive power references are considered to be 1.0 p.u. (4 MW) and 0 p.u., respectively

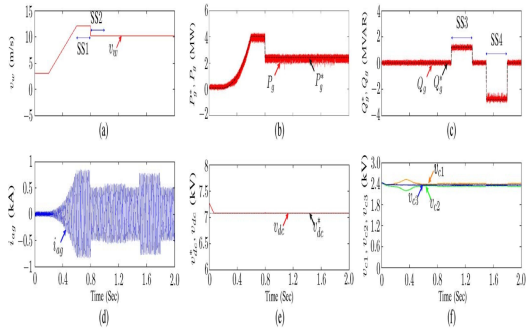

Fig. 3. Simulation results with dynamic active and reactive power references: (a) wind speed profile (vw); (b) reference and measured grid active power values (P∗g and Pg); (c) reference and measured grid reactive power values (Q∗g and Qg); (d) phase-a grid current (iag); (e) reference and total dc link voltages (v∗dcand vdc); and (f) dc link capacitor voltages (vc1, vc2, and vc3). (Case SS1). The dc link capacitor voltages are assumed balanced, and thus, weighting factor λdc is set to zero. With this assumption, the number of calculations for the predictive con- trol decreased, and as a result, the device switching frequency fsw is decreased from 854 to 680 Hz and no weighting factor is used either for the switching frequency minimization. The in phase disposition modulation, which gives the best harmonic profile, is used in the decoupled VOC. In order to make the device switching frequency same as predictive control, the carrier frequency is set to 2040 Hz.

The comparison between the classical and proposed methods in terms of reference tracking is presented in Fig. 4. The proposed method exhibits better performance compared with the classical method. The epg and eqg for the classical method are 1.1%, and 0.8%, whereas for the proposed method, they are 0.98%, and 0.75%, respectively. Inverter line–line voltage viab and its fast Fourier transform (FFT) with the classical and proposed methods are shown in Fig. 5. The classical method produces harmonics around carrier frequency and its multiples, whereas the proposed method produces harmonics spread over the whole FFT window. However, the peak magnitude of harmonics with the proposed method is less compared with the classical method, and as a result, less THD is observed. The phase-a grid current iag and its FFT are depicted in Fig. 6, where the THD is found be lower for the proposed method in contrast to the classical controller. Despite the lower switching frequency compared with the operating condition SS1 depicted in Table III, the THD is lower because the cost function includes only reference tracking.

The performance of the Lagrange and the proposed extrap- olation methods are analyzed and compared in Fig. 7. With a step change in the reference active power from 0.2 to 0.4 p.u., the Lagrange extrapolation method produces a dip in the active power, which, in turn, produces a spike in the inverter output line–line voltage, as shown in Fig. 7(a). This voltage spike is undesirable because it will damage the semiconductor switches. It is important to note that the voltage spike is produced due to the oscillations in the extrapolated reference active power, P∗g (k + 1), which is shown in the box in Fig. 7(a). The reasonis that the Lagrange method uses present and past three values for the calculation of future value [refer to (18) and (19)]. The extrapolated grid voltage (vedg(k + 1)) and predicted grid currents (ipdg(k + 1), ip qg(k + 1)) do not contribute to this voltagespike [refer to (11)]. The voltage spike occurs even for a small step change in reference active and reactive power values, and thus, it is not advisable to use Lagrange extrapolation method. This problem has been rectified with the proposed extrapolation method, as shown in Fig. 7(b); thus, it guarantees safe operation of the semiconductor devices. The proposed method uses only one past value and eliminates the oscillations in P∗g (k + 1), asshown in the box in Fig. 7(b). In order to verify the proposed dc link balancing algorithm, two cases are considered by connecting an external resistor Rx (11.46 p.u.) and capacitor Cx (15.33 p.u.) across the dc link capacitor Cdc2 at a time of t = 0.7 s Even with the step connection of the resistor, the controller takes action in a few sampling instants, and thus, the capacitor voltages continue to be balanced, as shown in Fig. 8(a). With the step connection of Cx, the capacitor voltages diverge, as shown in Fig. 8(b), but the controller forces the capacitor voltages to be balanced while maintaining the grid power values at their reference values (of SS1). As a consequence, the capacitor voltages become balanced, with a fast recovery time of 0.4 s. This case may happen when any of the dc link capacitor is damaged while it is in the parallel connection. The currents through Rx and Cx are also shown in Fig. 8(a) and (b), respectively.

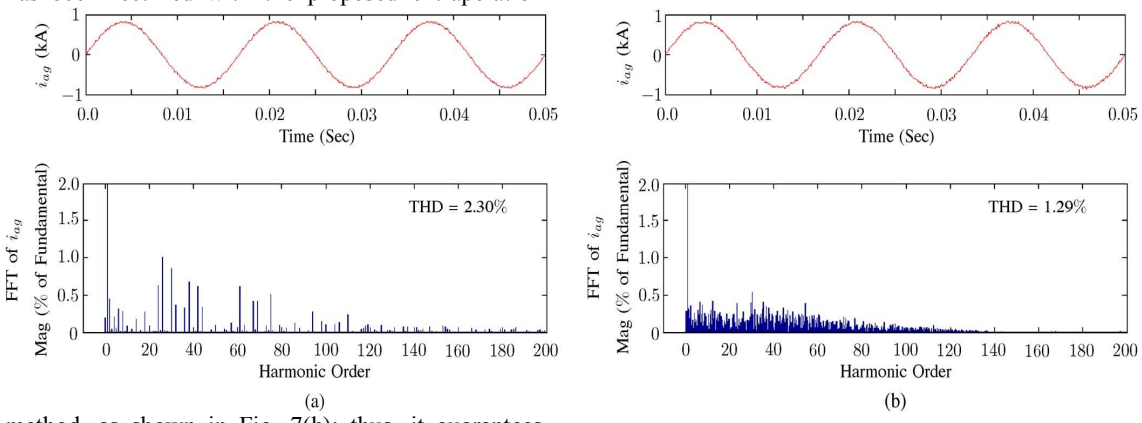

Fig. 5. Simulation results for inverter line–line voltage and its FFT with: (a) classical decoupled VOC and (b) predictive control.

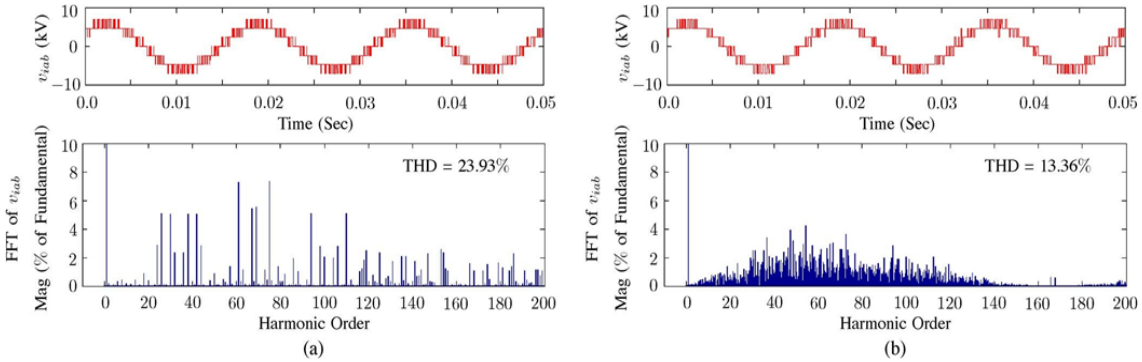

Fig. 6. Simulation results for (i) active power Pg and (ii) inverter line–line voltage viab with: (a) Lagrange extrapolation and (b) proposed extrapolation.

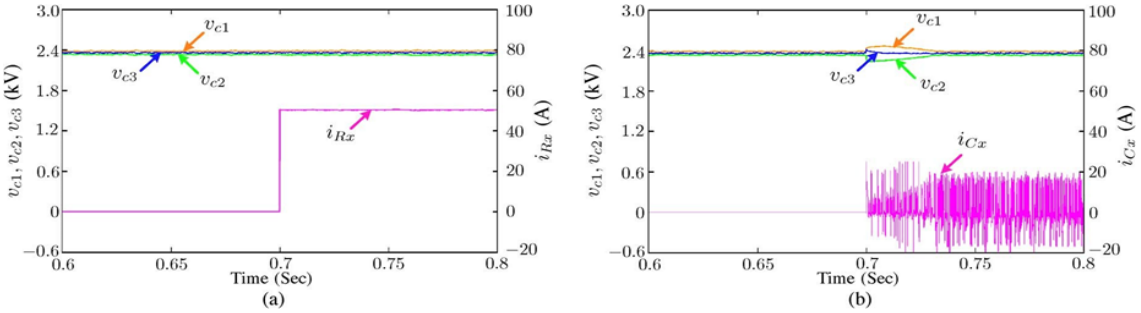

Fig. 7. Simulation results for dc link capacitor voltage balancing with: (a) external resistor Rx across dc link capacitor Cdc2 and (b) external capacitor Cx across dc link capacitor Cdc2.

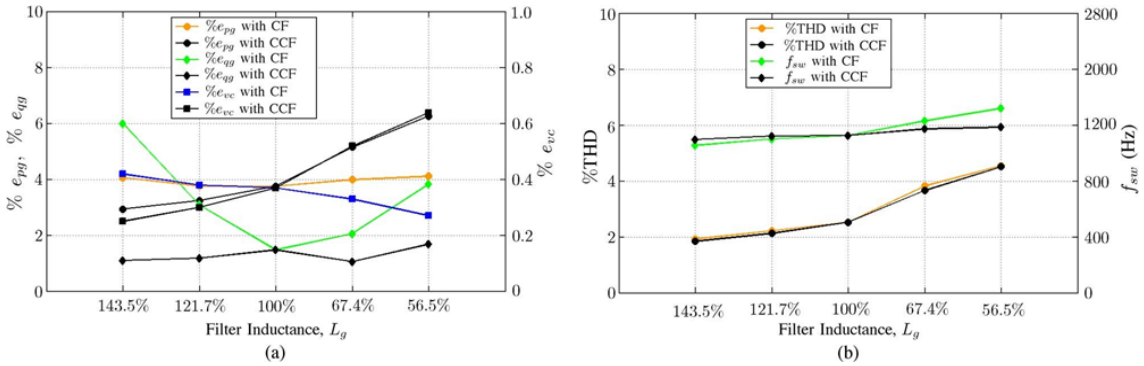

Fig. 9. Simulation results with grid filter parameter variations: (a) comparison of %epg, %eqg, and %evc and (b) comparison of %THD and fsw(Hz). CF: changes to filter. CCF: changes to controller and filter.

These results validate that the proposed controller can work very well even with the dc link parameter variations. To demonstrate the robustness of predictive control with the filter parameter variations, two cases are considered. In the first case (CF: changes to the filter), the filter inductance is considered to change from 143.5% to 56.5%, but this information is not provided to the controller. The control algorithm uses a rated filter inductance value of 100% (0.2 p.u. = 2.1 mH). This is the typical case in a grid-connected system, where the power system impedance randomly changes, and as a consequence, the equivalent filter value changes.

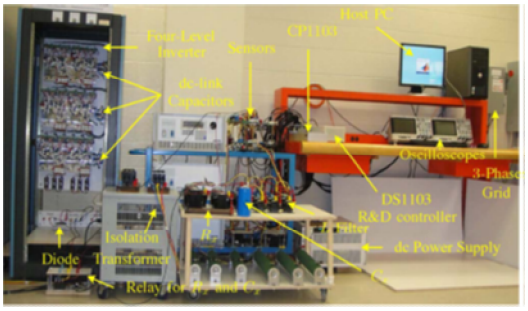

Fig. 9. Photograph of experimental test bench.

In the second case (CCF: changes to the controller and filter), the correct values of the filter are given to the controller for the purpose of comparison. To simplify the analysis, the switching frequency minimization is not considered, and thus, λswc = 0. Although the filter parameters change, the controller chooses a switching state that produces the minimal error in the reference tracking and capacitor voltage balancing. As shown in Fig. 9(a) and (b), the difference between the CF and CCF conditions is found to be very small in the Lg variation range of 130%–70%.

5. Experimental Results

In order to verify the performance of the proposed control strategy, an experimental test bench has been developed, as shown in Fig. 10. The inverter and controller parameters are listed in Table V (see the Appendix). The inverter was controlled by a dSPACE DS1003 rapid prototyping board. The currents and voltages are measured by LEM LA55-P andLV25-P sensors, respectively, and sent to the controller through a CP1103 I/O connector. The inverter switches, clamping diodes, and gate drivers are developed by Semikron SKM75GB123D, SKKD75F12, and SKHI22B, respectively. The inverter is connected to the grid through an isolation transformer, and its impedance is added to the filter values.To compensate for the computational delay

provided by the digital signal processor, the cost function is calculated with a two-step prediction horizon [20], i.e., g(k + 2), and then the selected switching state is applied at (k + 1) sampling instant, as shown in Fig. 11. Because of the SRF modeling of dc link voltages, idg(k + 1) and iqg(k + 1) can be used straightly in the prediction of ic1(k + 2), ic2(k + 2), and ic3(k + 2) [refer to (7)]. If the modeling is done in a natural frame, then idg(k + 1) and iqg(k + 1) should be converted to iag(k + 1), ibg(k + 1), and icg(k + 1) during each sampling interval, and this will increase the computational burden. Due to the (k + 2) predictions and the SI parameter values, the weighting factors obtained in the experiments are different from the simulations, but their impact on the controller remains same.

The experimental results with the different active and reactive power references are shown in Fig. 12. Similar to the simulations, the decoupled control of active and reactive power values is achieved with the fast dynamic response and less steady-state error. The dc link capacitor voltages are tightly regulated during all the operating conditions. The steady-state analysis has been carried out and summarized in Table IV. The higher tracking errors in experiments can be attributed to the

TABLE IV
STEADY-STATE ANALYSIS WITH EXPERIMENTAL RESULTS

Case	P_g^*(pu)	Q_g^*(pu)	$\%e_{pg}$	$\%e_{qg}$	$\%e_{vc}$	%THD	f_{sw}(Hz)
SS1	1.0	0	5.08	2.59	0.39	3.82	845
SS2	0.6	0	4.05	2.34	0.63	5.23	900
SS3	0.6	0.3	4.56	3.25	0.51	4.88	731
SS4	0.6	−0.7	3.87	3.89	0.29	3.70	998

Delay provided by the sensors, insulated-gate bipolar transistor (IGBT) gate drivers, and also losses in the system. Since the predictions are in (k + 2), evc is found to be smaller than in simulations. The Lagrange and proposed extrapolation methods are experimentally analyzed and compared in Fig. 13. As confirmed by the simulations, the Lagrange extrapolation method produces a dip in the active power and a spike in the inverter output voltage, as shown in Fig. 13(a). The oscillations in the extrapolated reference active power P∗ g (k + 2) are also shown in Fig. 13(a). The proposed extrapolation method eliminates the voltage spike, as shown in Fig. 13(b), and protects the semiconductor switches. The dc link dynamics with the external resistor Rx and capacitor Cx across Cdc2 is shown in Fig. 14(a) and (b), respectively. Similar to the simulations, balancing of the dc link capacitor voltages has been maintained even with the step connection of Rx and Cx. The recovery time is found to be 1.3 s with Cx, which is higher compared with the simulations. This difference is established due to the different weighting factors and SI values of the grid current and the dc link capacitor used in the prototype. The effect of the filter parameter variations on the proposed controller is experimentally analysed and presented in Fig. 15(a) and (b). Only a small difference is observed between the CF and CCF cases, similar to the simulation results, with the Lg variation in a range of 130%–70%. These results validate the robustness of the proposed controller with the filter parameter variations.

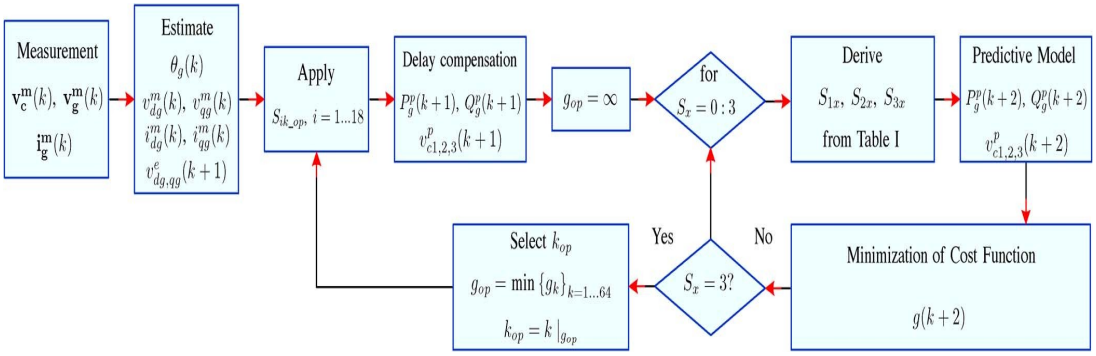

Fig. 10. Proposed predictive control algorithm with delay compensation.

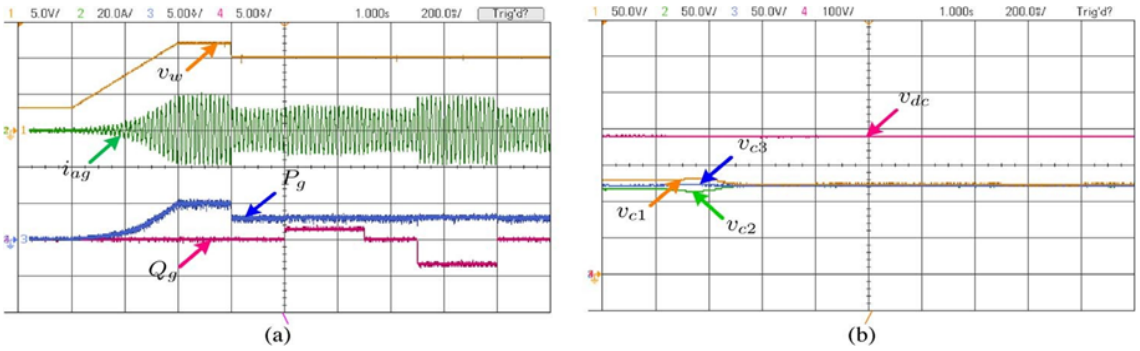

Fig. 11. Experimental results with dynamic active and reactive power references: (a) Ch1: wind speed profile (5 V/div); Ch2: phase-a grid current (20 A/div); Ch3: measured grid active power (5 kW/div); and Ch4: measured grid reactive power (5 kvar/div); (b) Ch1–Ch3: dc link capacitor voltages (50 V/div); Ch4: total dc link voltage (100 V/div). Timescale: 200 ms/div.

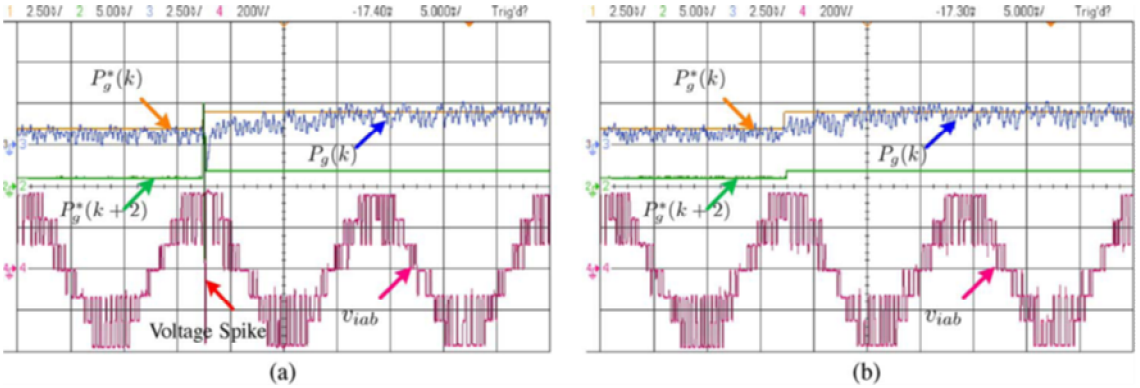

Fig. 12. Experimental results during the step change in active power reference: (a) with Lagrange extrapolation and (b) with the proposed extrapolation. Ch1: reference active power (2.5 kW/div); Ch2: extrapolated reference active power (5 kW/div); Ch3: measured grid active power (2.5 kW/div); and Ch4: inverter line–line voltage (200 V/div).

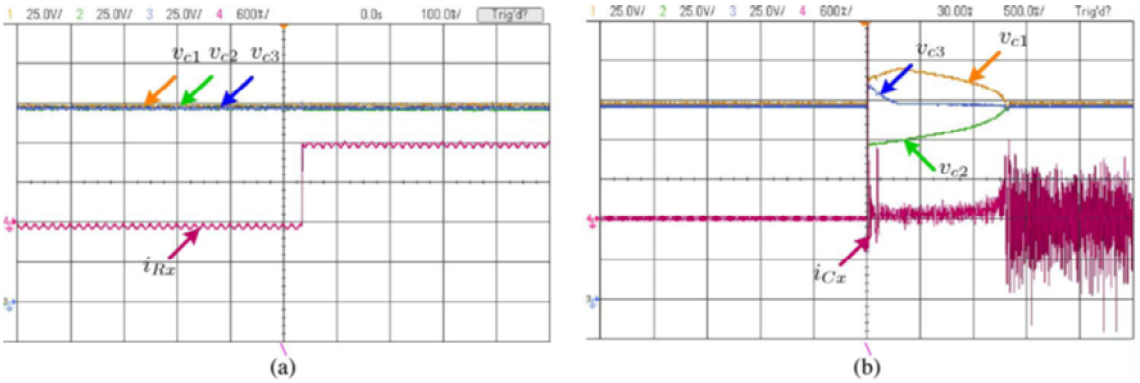

Fig. 13. Experimental results for the dc link capacitor voltages balancing with: (a) external resistor Rx across dc link capacitor Cdc2 and (b) external capacitor Cx across dc link capacitor Cdc2. Scope (a) Ch1–Ch3: dc link capacitor voltages (25 V/div) and Ch4: current through Rx (600 mA/div) and timescale: 100 ms/div. Scope (b) Ch1–Ch3: dc link capacitor voltages (25 V/div) and Ch4: current through Cx (600 mA/div) and timescale: 500 ms/div.

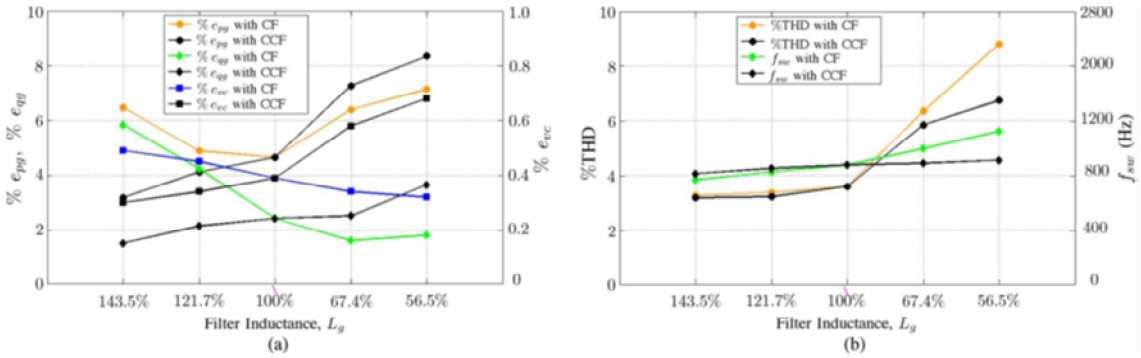

Fig. 15. Experimental results with grid filter parameter variations: (a) comparison of %epg, %eqg, and %evc and (b) comparison of %THD and fsw(Hz).CF: changes to filter. CCF: changes to controller and filter.

6. Conclusion

In this paper, a simple and intuitive approach using the predictive control has been presented in SRF for the high- power MV grid-connected four-level diode-clamped inverter. A fast dynamic response has been achieved by eliminating the internal current control loops and modulators. Compared with the classical decoupled VOC, a better reference tracking and power quality has been achieved. The decoupled active and reactive power control, along with dc link capacitor voltage balancing, has been achieved during all operating conditions. The reliability of the semiconductor switches has been im- proved by maintaining the switching frequency below 1 kHz. The proposed extrapolation method provides a simple and computationally inexpensive approach to mitigate the problem of voltage spikes during the dynamic changes in the reference power values. In addition, it has been demonstrated that the control scheme can compensate for perturbations in the dc link and grid filter parameter changes, whereas the grid power values continue to effectively track their references.

APPENDIX

The parameters used in the simulation and experimental tests are summarized in Table V.

TABLE V
GRID-CONNECTED FOUR-LEVEL INVERTER PARAMETERS

Variable	Description	Simulation		Experimental	
		SI	pu	SI	pu
S_g	Apparent Power (kVA)	4000	1.0	5	1.0
v_g	Grid L-L *rms* Voltage (V)	4000	–	208	–
i_g	Grid *rms* Current (A)	577.35	1.0	13.88	1.0
f_g	Grid Frequency (Hz)	60	1.0	60	1.0
R_g	Filter Resistance (Ω)	0.042	0.0105	0.091	0.0105
L_g	Filter Inductance (mH)	2.1	0.2	4.6	0.2
C_{dc}	dc-link Capacitance (μF)	10200	15.33	4700	15.33
v_{dc}^*	Ref dc-link Voltage (V)	7071	3.062	367	3.062
E	Battery Voltage (V)	7071	3.062	373	3.108
R_x	External Resistance (Ω)	46.24	11.56	100	11.56
C_x	External Capacitance (μF)	10200	15.33	4700	15.33
λ_{dc}	Weight Factor	500	–	150	–
λ_{swc}	Weight Factor	30000	–	5	–
T_s	Sampling Time (sec)	100μ	–	100μ	–
Base Values					
v_{bg}	Base *rms* Voltage (V)	2309.4	1.0	120	1.0
Z_{bg}	Base Impedance (Ω)	4.0	1.0	8.6528	1.0
L_{bg}	Base Inductance (mH)	10.6	1.0	23.0	1.0
C_{bg}	Base Capacitance (μF)	663.15	1.0	306.56	1.0

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