International Journal of Research
Available at https://edupediapublications.org/journals
p-ISSN: 2348-6848
e-ISSN: 2348-795X
Volume 03 Issue 14
October2016

Fuzzy Bridgeless Power Factor Correction Based Converter Welding Applications

Shevva swathi
M-tech Student Scholar
Department of Electrical & Electronics Engineering,
Scient institute of technolgy, ibrahimpatnam;
Ranga reddy (Dt); Telangana, India.
Email:shevva.swathi5@gmail.com

K.SREEPAL REDDY
Associate Professor
Department of Electrical & Electronics Engineering,
Scient institute of technolgy, Ibrahimpatnam;
Ranga reddy (Dt); Telangana, India.
Email:sreepalpid@gmail.com

Abstract– This concept deals with a new single-phase bridgeless AC-DC converter for AWPS (Arc Welding Power Supply) with an ability to improve the power factor at AC mains. The PFC (Power Factor Correction) converter is based on high frequency isolated Cuk converter topology. The conduction losses are reduced by eliminating the DBR (Diode Bridge Rectifier) in classical converter topology. The proposed converter topology is designed to operate in DCM (Discontinuous Conduction Mode) for simple control and to minimize the EMI (Electromagnetic Interference). The DCM operation also facilitates to achieve a unity power factor at AC mains. This converter regulates constant voltage at the output in the range of welding currents and inherent parametrical short-circuit current limit to improve the weld bead quality. The dynamic and steady state responses of the proposed AC-DC converter are included to validate the capability of converter for welding power supply. The proposed concept can be implemented to fuzzy logic controlled applications by using mat lab/Simulink software.

Keywords—Arc Welding Power Supply (AWPS), Bridgeless, Power Quality, Total Harmonic Distortion (THD),Cuk Converter.

I INTRODUCTION

Modern Arc Welding Power Supply (AWPS) employs controllable high frequency (HF) DC-DC power converter(s) with excellent dynamic and steady state performance compounded with stringent voltage-current regulation. Generally, robustness, portability and simplicity are amongst the prevailing design criteria [1] for the AWPS. Moreover, to ensure suitably systematized metal droplet transfer through the established arc, AWPS should limit the welding load current even during the short circuit condition and must operate satisfactorily over a very wide load range i.e. from rated load to short-circuit condition. Also, a broad span of controlled load current is essential to enhance the welding action. Thus, in order to control the welding characteristics, the output DC voltage along with the output DC current, must always be regulated [2].

Mainly the conventional switched mode power supplies (SMPSs) for welding applications comprise a front-end uncontrolled diode bridge rectifier (DBR) followed by a bulk DC-link capacitor [3]. The presence of the DBR generally leads to problems such as high conduction loss and increased harmonic currents thus creating interference in power and communication lines. In the past few years, bridgeless (BL) power factor corrected (PFC) converters have gained huge attention and popularity due to their higher efficiency. In an effort to improve the Power Quality (PQ) of the SMPSs, various BL boost converter based topologies have been reported in the literature [4] adhering to the stringent requirements put forth by the international PQ standard IEC 61000-3-2 [5].

A considerable amount of work on BL boost PFC converter has been carried out because of its low cost, simplicity and high performance in terms of efficiency and PF. Nonetheless, the BL boost PFC converter suffers from some major limitations such as high start-up inrush current, lack of current limiting during overload conditions and ineptness to step down the input voltage. However, these are some of the essential prerequisites in designing an SMPS for welding applications. A BL buck converter has a poor PFC capability and also does not support short-circuit operating conditions. Among various buck-boost converters, Cuk converter offers high quality input and output currents due to the presence of inductors at both input and output side of the converter [6]. Thus, considering a BL PFC Cuk converter that is capable of yielding lower voltage at the output would be a viable alternative.

The objective of this paper is to design and model a single phase AWPS using BL-Cuk converter at the front end and a PWM full-bridge (FB) DC-DC converter for high-frequency isolation at the load

International Journal of Research
Available at https://edupediapublications.org/journals
p-ISSN: 2348-6848
e-ISSN: 2348-795X
Volume 03 Issue 14
October2016

end. Its meritorious features include output voltage stability and short-circuit withstand capability. The BL -Cuk converter is designed to operate in Discontinuous Conduction Mode (DCM) to attain inherent PFC at the input AC mains [7-8]. Independent closed loop control functions are used in both stages. A Pulse Width Modulation (PWM) control strategy has been implemented with a constant switching frequency of 50 kHz. Its fast dynamic response during load variations leads to a better arc stability and uniform weld bead quality. The detailed analysis and design of the proposed AWPS are discussed in following sections to illustrate its improved performance in terms of unity PF and reduced THD in the AC mains current at different loads and supply voltage conditions. The efficacy of the proposed improved PQ AWPS is demonstrated by means of simulation results using MATLAB/SIMULINK tool.

II PROPOSED BL CONVERTER BASED AWPS

The proposed BL -Cuk converter based AWPS is shown in Fig.3.1. The absence of front end DBR and the presence of only two semiconductor switches (one diode and one power switch) in the current flowing path during each switching cycle minimizes the conduction losses and improves the thermal management as compared to the conventional PFC converters. In this topology, two Cuk DC-DC converters are connected back-to-back followed by an isolated FB buck converter.

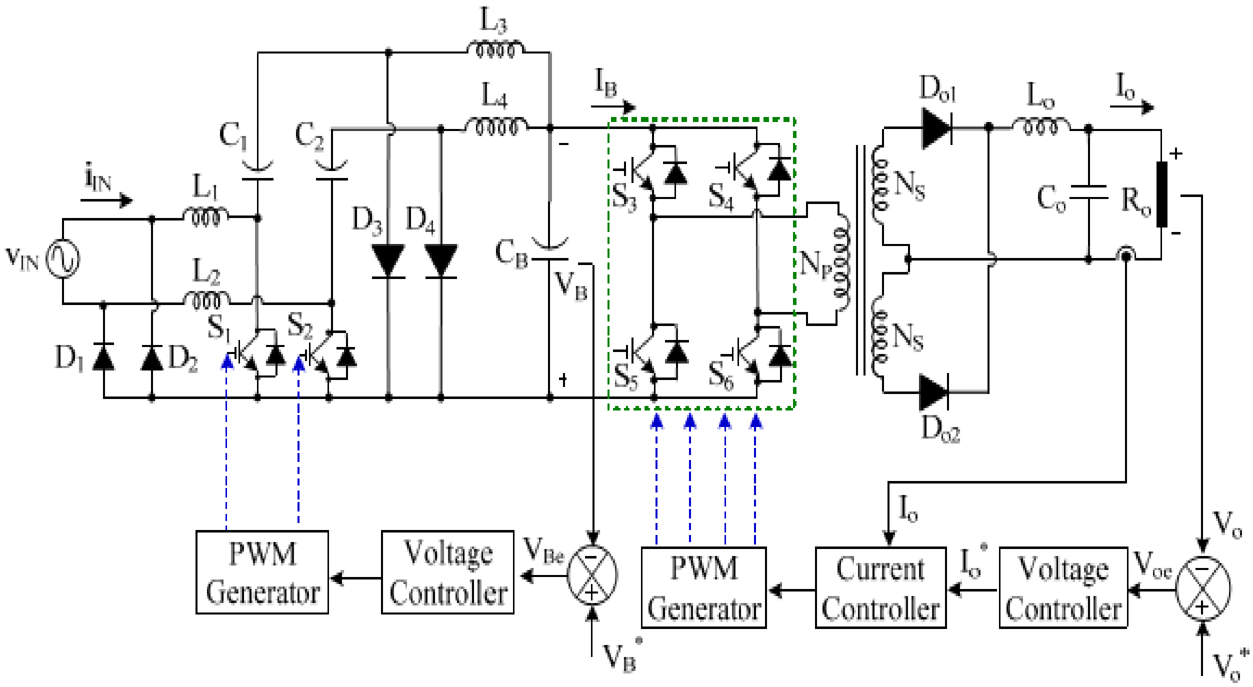


Fig 1 Schematic of BL Cuk converter and isolated FB converter based AWPS

Fig 2a and 2b depict the operation of the proposed topology during positive and negative half cycles of the input ac mains. Out of the two back-to-back connected Cuk converters, one operates during the positive half and the other during the negative half of the power frequency cycle. This further brings down the thermal stresses, as well as conduction losses.

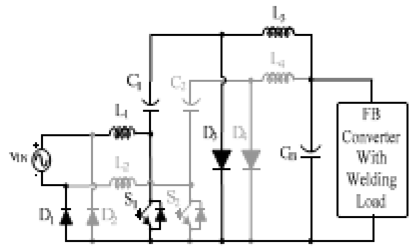
a) Configuration: The proposed circuit (Fig.3.1) comprises of a single phase AC mains feeding two Cuk converters which, in turn, feed a FB buck converter having a high frequency transformer (HFT) and a welding load. The first stage consisting of the PFC BL-Cuk converter rectifies the input AC mains voltage into an intermediate regulated DC voltage. The second stage is formed by using an isolated FB buck converter, to convert the output of the BL-Cuk converter into a DC output voltage of desired magnitude.

The DCM operation of the output inductors ($L_3$and L_4) of BL-Cuk converter results in an excellent PF pre-regulator operation and adds additional features such as zero current turn-on in the power switches $S_1$and S_2, and zero-current turnoff in diodes $D_3$and D_4. This in turn, minimizes the turn-on switching losses of the power switches and enhances the reverse recovery of the output diodes significantly. In

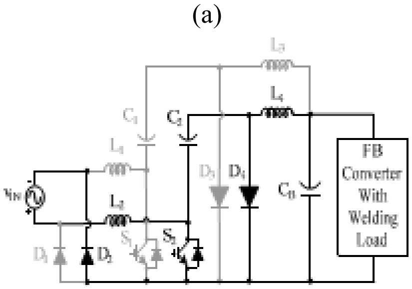
International Journal of Research
Available at https://edupediapublications.org/journals
p-ISSN: 2348-6848
e-ISSN: 2348-795X
Volume 03 Issue 14
October2016

the second stage, the FB buck DC-DC converter comprises of four power switches (S_3, S_4, S_5 and S_6), a HFT with its secondary center-tapped, a half-wave rectifier and an L_o-C_o filter at the output side. Since work-piece is a part of the power supply circuit, it must be earthed; thus, an isolation transformer is essential in AWPS to ensure safety. The resistance, R_o is considered as the welding load.

B) Operating Stages: The proposed BL AWPS is formed by connecting two Cuk converters, each functioning over a half-cycle period of the supply voltage. The operating principle of the BL-Cuk converter is explained for one half cycle of the supply frequency; in the other half cycle also the converter performs in a similar manner.



(a)



(b)

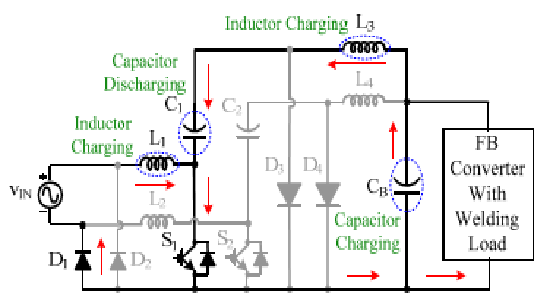
Fig 2. Operating circuits of the proposed BL Cuk converter based AWPS during positive and negative half-cycles of the supply voltage. (a) during positive half cycle; (b) during negative half cycle.

As shown in Fig 2(a), during the positive half-cycle, switch S_1, inductors $L_1$and L_3, diodes $D_1$and D_3 and capacitors C_1transfer the energy from the source to the DC link capacitor, CB. The voltage VBacross the DC-link capacitor CB is controlled and fed as an input to the isolated FB converter. Likewise, L_2-S_2-C_2-L_4-D_4, conduct through diode D_2during the negative half cycle of the input voltage as shown in Fig 2(b). For the analysis, all semiconductor devices are assumed to be ideal. The capacitances CBand Coare sufficiently large such that the voltage ripple across them can be neglected. The inductors L_3 and L_4 are designed such that the current through these inductors become discontinuous during each switching cycle. For the positive half-cycle of the input voltage, vin, there are three intermediate operating stages of the BL-Cuk converter for every switching cycle which are described as follows.

Stage I: Referring to Fig 3(a), when power switch S_1 is turned on, a positive supply voltage, vinis applied to the input inductor, L_1. So, the current through the input inductor, i_{L1}starts increasing linearly and flows through diode D_1. The intermediate capacitor $C_1$is discharged through the output inductor, $L_3$and the DC-link capacitor, CBthereby energizing the inductor, L_3. Hence the current, i_{L3}also rises linearly.

Stage II: During the turn-off state of S_1, diode D_3becomes forward biased providing a path for the inductor currents, $i_{L1}$and i_{L3}. The inductors, $L_1$and L_3transfer the stored energy to the capacitors $C_1$and CBrespectively. Thus the inductor currents start falling linearly. This interval continues till the inductor currents become equal and opposite (i.e. i_{L1}= $-i_{L3}$) and current through the diode, D_3reaches zero.

Stage III: This stage is initiated when both switch $S_1$and the diode $D_3$are turned off as the sum of inductor currents $i_{L1}$and i_{L3}becomes zero. Thus the converter enters into DCM operation as shown in Fig 3(c). The currents through inductors $L_1$and L_3remain constant and continue to charge the intermediate capacitor, C_1. Consequently, the DC-link capacitor CBdischarges to supply the load i.e. FB converter connected to it. The inductors act as current sources and the voltages across them is zero throughout this interval. Fig 3(d) illustrates the DCM waveforms during the positive half cycle of the supply voltage over one PWM switching period. Stage III is completed when switch $S_1$is triggered to restart the operating cycle again.



(a)

International Journal of Research
International Journal of Research
Available at https://edupediapublications.org/journals
p-ISSN: 2348-6848
e-ISSN: 2348-795X
Volume 03 Issue 14
October2016

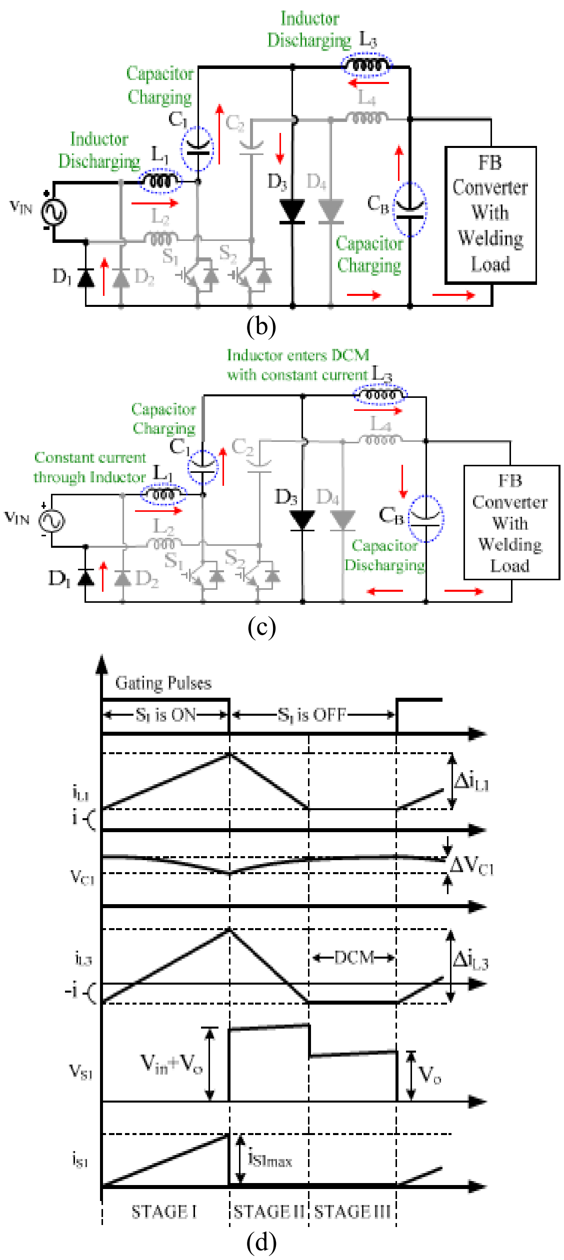


Fig 3 Operating stages of BL Cuk converter during steady state. (a) Stage I; (b) Stage II; (c) Stage III; (d) Waveforms during one switching period

The controlled DC output (V_B, I_B) of the BL-Cuk converter is further fed to the FB buck converter which is intended to operate in Continuous Conduction Mode (CCM). In the FB converter, the switching pairs S_3-S_6 and S_4-$S_5$are turned on alternately during each half cycle of a switching period. The voltage V_B, is applied across the primary winding of the HFT. When both the switching pairs are turned off, then the output rectifier diodes $D_{o1}$and D_{o2}act as freewheeling diodes. At the output, L_o-$C_o$filter provides a ripple-freeoutput DC voltage.

C) Control Strategy: Pulse Width Modulation (PWM) technique is used with a constant switching frequency (=50kHz) to ensure DCM operation of the BL-Cuk converter. This minimizes the number of sensors required thereby cutting down on the cost. However, the same control signal can be used to drive both power switches, $S_1$and S_2, which considerably simplifies the control circuit. With minimal amount of control circuitry, the proposed AWPS design is very compact and economical. The BL converters are operated in DCM by incorporating voltage mode control technique. The DCM operation of the PFC stage ensures high PF at the input and excellent voltage regulation at the output DC-link.

The DC-link voltage, V_B is compared with the reference voltage, V_B* to generate the voltage error, V_{Be} which is fed to a Proportional-Integral (PI) controller whose output is compared with a 50 kHz ramp signal to generate the firing signals for the switches $S_1$and S_2. The PI controller provides excellent line-load regulation. Dual loop control scheme is employed in the isolated FB converter to incorporate short circuit protection. The sensed output DC voltage, Vois compared with the reference DC voltage, V_o*. This error voltage signal, V_{oe} is further fed to another PI voltage controller to generate a reference signal, I_o*. This serves as the reference for the output load current, Io. Now, I_o* is compared with the actual Ioso that it is prevented from exceeding the desired limit. The output of the PI current controller is given to the PWM generator where it is compared with the HF ramp signal to generate gating pulses for the isolated FB converter.

III DESIGN OF PROPOSED BL CONVERTER BASED AWPS

The complete design and analysis of the BL converter based AWPS are presented in this section. During the analysis, the power switches and the diodes are assumed to be ideal. In order to derive the necessary component design, the supply voltage, v_{in} is considered to be a constant during one switching frequency (f_s) cycle as f_s is much higher than the line frequency, f.

A) Design Of Bl-Cuk Converter:

For the sake of simplicity, a single module of Cuk converter, operating in positive half cycle of the supply voltage is considered for this analysis. The PFC BL-Cuk converter is designed to maintain a constant DC-link voltage (V_B) of 400 V with the inductors (L_3 and L_4) operating in DCM. The average value, $V_{inav}$of the supply voltage ($v_{in,rms}$= 220 V) is given as,

$$V_{inav} = \frac{2\sqrt{2}v_{in}}{\pi} = \frac{2\sqrt{2}*220}{\pi} = 198.07V \quad (1)$$

On applying the volt-second balance to the BL Cuk converter, one obtains,

$$\frac{V_B}{V_m} = \frac{D_B}{\sqrt{K}} \quad (2)$$

Where,

$$K = \frac{2f_s}{R_B}\left(\frac{L_1L_3}{L_1+L_3}\right) = \frac{2f_sL_{eq}}{R_B} \quad (3)$$

$$L_{eq} = \frac{L_1L_3}{L_1+L_3} \quad (4)$$

$$R_B = \frac{V_B}{I_B} = \frac{400}{5} = 80\ \Omega \quad (5)$$

Also, $D_B$is the on-time of the power switches $S_1$and S_2, V_B is the DC-link voltage and f_S is the switching frequency (=50kHz) of the BL Cuk converter.

The integral of the inductor voltages must be zero over one switching period. Thus the expression for duty cycle, D_B is given by,

$$D_B = \frac{V_B}{V_{inav}+V_B} = \frac{400}{198.07+400} = 0.668 \quad (6)$$

In order to operate the converter in DCM,

$$K < K_c < \frac{V_m^2}{2(V_m+V_B)^2} < \frac{(311)^2}{2(311+400)^2} < 0.0956 \quad (7)$$

The value of K is taken around two-thirds of K_c to ensure DCM operation of the proposed BL Cuk converter. Thus, K is selected as 0.06373.

$$L_{eq} = \frac{R_BK}{2f_s} = \frac{80*0.06373}{2*50000} = 50.984\ \mu H \quad (8)$$

If Δi_{L1} and $\Delta i_{L3}$are considered to be the permissible current ripple in the inductors $L_1$and L_3respectively, then the change in inductor currents (Δi_{L1} and Δi_{L3}) is determined from the on period of the semiconductor devices as,

$$\Delta i_{L1} = \frac{V_{inav}D_B}{L_1f_s}$$

Thus,

$$L_1 = \frac{D_BV_{inav}}{f_s(\Delta i_{L1})} = \frac{0.668*198.07}{50000*1.993} = 1.327\ mH \quad (9)$$

where f_S is 50 kHz. The value of the input inductor, $L_1$is estimated to be 1.5mH. Using eqns. (3.4), (3.8) and (3.9),

$$L_3 = \frac{L_1L_{eq}}{L_1-L_{eq}} = \frac{(1.327*10^{-3})(50.984*10^{-6})}{(1.327*10^{-3})-(50.984*10^{-6})} = 53.021\mu H \quad (10)$$

The selected value of inductor, $L_3$is 40 μH to achieve DCM operation. To minimize the input current oscillation, the resonant frequency of C_1, $L_1$and L_3should be greater than the line frequency. Moreover, the resonant frequency of $C_1$and L_3must be less than the switching frequency to attain constant voltage during every switching cycle. Therefore, the value of the intermediate capacitor, C_1can be approximated as,

$$C_1 = \frac{1}{\omega_r^2(L_1+L_3)}$$

$$= \frac{1}{(2\pi*5000)^2(1.327*10^{-3}+53.021*10^{-6})} = 0.734\ \mu F \quad (11)$$

$\omega_L < \omega_r < \omega_s$; ω_L = line frequency,
where
ω_r = resonant frequency,
ω_s = switching frequncy

The resonant frequency is selected to be 5 kHz. The DC-link capacitor, CBvalue can be calculated from eqn. (3.8) for a given voltage ripple in the DC-link voltage, V_B as,

$$C_B = \frac{I_B}{4\pi f(\Delta V_B)} = \frac{5}{4*\pi*50*40} \cong 0.2\ mF \quad (12)$$

***B) Design Of Isolated Fb Buck Converter*:**

For an isolated FB buck converter operating in CCM, the voltage conversion ratio can be derived by applying the constant volt-second relationship on the output inductor, L_o.

$$\left\{V_B\left(\frac{N_S}{N_p}\right)-V_o\right\}\left(\frac{t_{on}}{T_s}\right)-\left\{V_o\left(\frac{t_{off}}{T_s}\right)\right\}=0 \quad (13)$$

Thus the duty cycle, Dffor switches S_1, S_2, S_3, S_4, is given as,

$$D_f = \frac{V_o}{2V_B}\left(\frac{N_P}{N_S}\right) \quad (14)$$

Considering

International Journal of Research
Available at https://edupediapublications.org/journals
p-ISSN: 2348-6848
e-ISSN: 2348-795X
Volume 03 Issue 14
October2016

$$D_f = 0.35, \left(\frac{N_P}{N_S}\right) = \frac{0.35*2*400}{20} = 14$$

If the permissible ripple current is ΔiLo(10% of Io) then the value of output inductor, Lofor CCM operation can be estimated as,

$$L_o = \frac{V_o\left(0.5-D_f\right)}{f_s(\Delta i_{Lo})} = \frac{20*(0.5-0.35)}{50000*10} = 6\mu H \qquad (15)$$

To ensure CCM operation of the inductor, the selected value
of L_o= 9μH.
The voltage ripple on output capacitor Cois calculated as,

$$\Delta V_o = \frac{V_o\left(1-2D_f\right)}{32\, f_s^2 L_o C_o} \qquad (16)$$

The output capacitor value is calculated for a given voltage ripple as,

$$C_o = \frac{V_o\left(1-2D_f\right)}{32 f_s^2 L_o(\Delta V_o)} = \frac{20*(1-0.7)}{32*50000^2*6*10^{-6}*2} \cong 7\mu F \qquad (17)$$

The complete design specifications for both the converters (BL Cuk and isolated FB buck converter) calculated using the above equations are listed in the Appendix.

IV. INTRODUCTION TO FUZZY LOGIC CONTROLLER

L. A. Zadeh presented the first paper on fuzzy set theory in 1965. Since then, a new language was developed to describe the fuzzy properties of reality, which are very difficult and sometime even impossible to be described using conventional methods. Fuzzy set theory has been widely used in the control area with some application to dc-to-dc converter system. A simple fuzzy logic control is built up by a group of rules based on the human knowledge of system behavior. Matlab/Simulink simulation model is built to study the dynamic behavior of dc-to-dc converter and performance of proposed controllers.

Furthermore, design of fuzzy logic controller can provide desirable both small signal and large signal dynamic performance at same time, which is not possible with linear control technique. Thus, fuzzy logic controller has been potential ability to improve the robustness of dc-to-dc converters. The basic scheme of a fuzzy logic controller is shown in Fig 5 and consists of four principal components such as: a fuzzification interface, which converts input data into suitable linguistic values; a knowledge base, which consists of a data base with the necessary linguistic definitions and the control rule set; a decision-making logic which, simulating a human decision process, infer the fuzzy control action from the knowledge of the control rules and linguistic variable definitions; a de-fuzzification interface which yields non fuzzy control action from an inferred fuzzy control action [10].

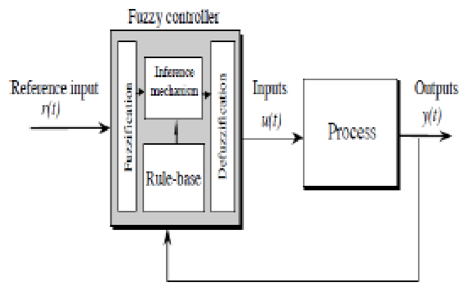


Fig 4 General Structure of the fuzzy logic controller on closed-loop system

The fuzzy control systems are based on expert knowledge that converts the human linguistic concepts into an automatic control strategy without any complicated mathematical model [10]. Simulation is performed in buck converter to verify the proposed fuzzy logic controllers.

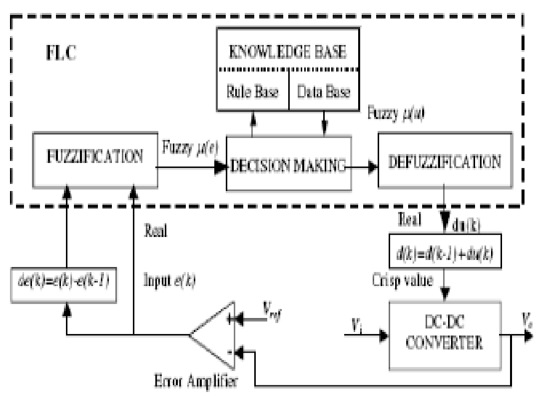


Fig 5 Block diagram of the Fuzzy Logic Controller (FLC) for dc-dc converters

Fuzzy Logic Membership Functions:

The dc-dc converter is a nonlinear function of the duty cycle because of the small signal model and its control method was applied to the control of boost converters. Fuzzy controllers do not require an exact mathematical model. Instead, they are designed based on general knowledge of the plant. Fuzzy controllers are designed to adapt to varying operating points. Fuzzy Logic Controller is designed to control the output of boost dc-dc converter using Mamdani style fuzzy inference system. Two input variables, error (e) and change of error (de) are used in this fuzzy logic system. The single output variable (u) is duty cycle of PWM output.

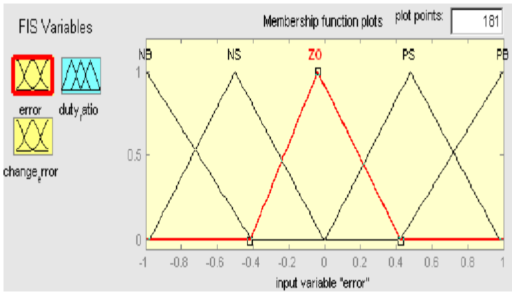


Fig 6 The Membership Function plots of error

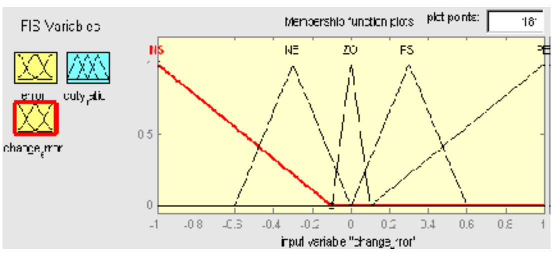


Fig 7 The Membership Function plots of change error

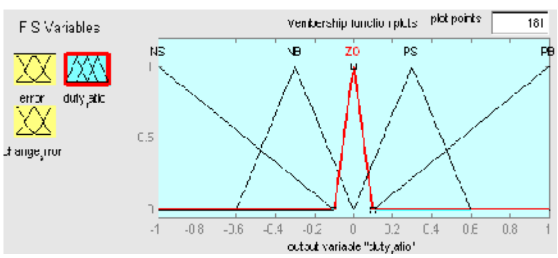


Fig 8 the Membership Function plots of duty ratio

IV MATLAB/SIMULINK RESULTS

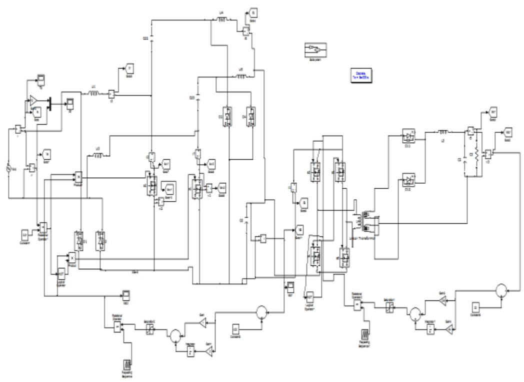


Fig 9 Simulation model of BL Cuk converter and isolated FB converter based AWPS

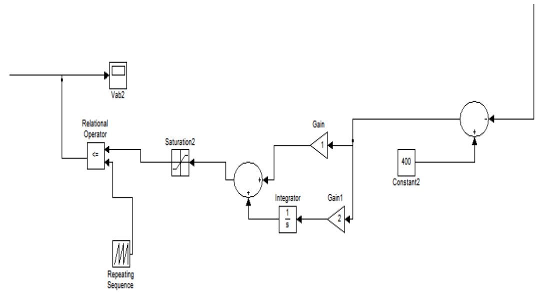


Fig 10 Simulation model of Control circuit diagram

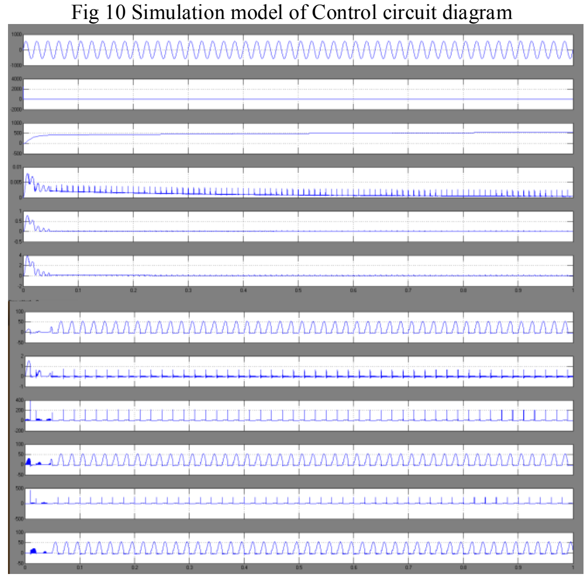


Fig 11 Simulation waveform of Steady state behavior of proposed AWPS at 220 V AC mains and 100% load.

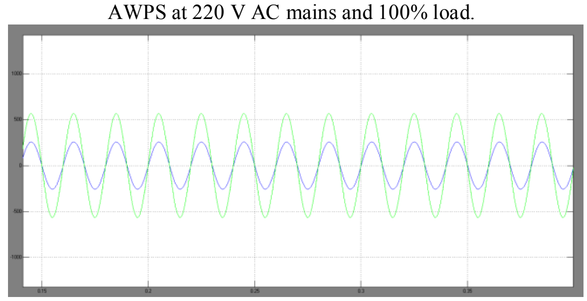


Fig 12 Simulation waveform of Input voltage and current

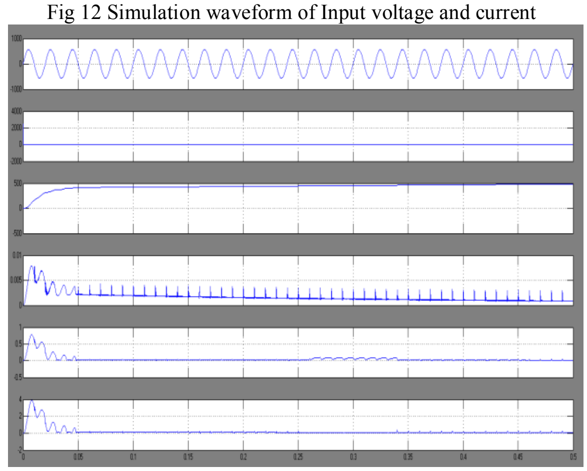


Fig 13 Simulation waveform of Dynamic performance of the proposed AWPS at 20% load

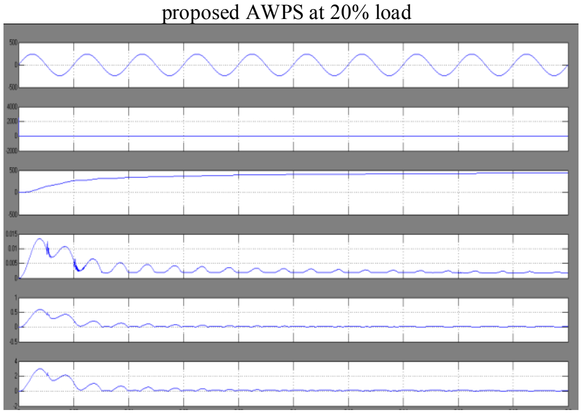


Fig 14 Simulation waveform of Dynamic performance of the proposed AWPS at VIN of 170 V and full load condition

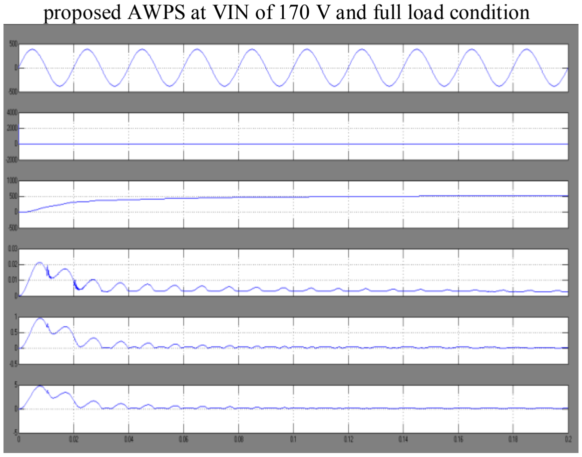


Fig 15 Simulation waveform of Dynamic performance of the proposed AWPS at VIN of 270 V and full load condition

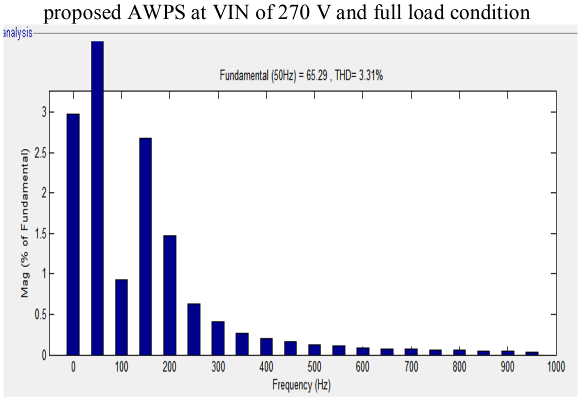


Fig 16 Simulation waveform of Harmonic analysis

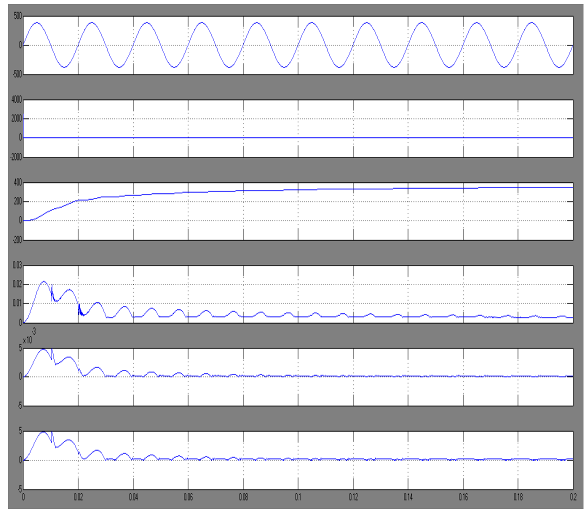


Fig 17 Simulation waveform of Dynamic performance of the proposed AWPS during over-current condition

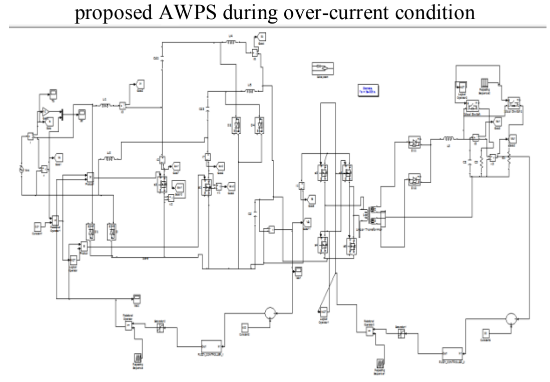


Fig 18 Simulation model of Fuzzy based BL Cuk converter

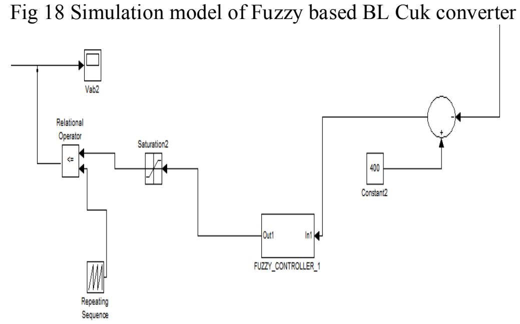


Fig 19 Simulation model of Fuzzy logic control circuit diagram

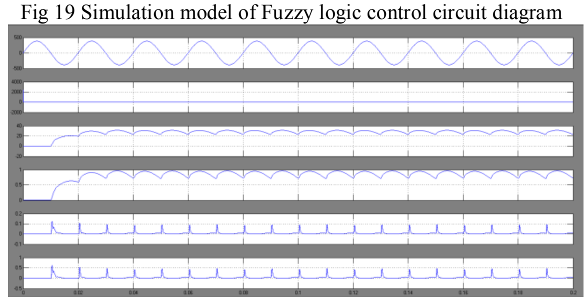


Fig 20 Simulation waveform of Dynamic performance of the proposed AWPS at V_{IN} of 270 V and full load condition

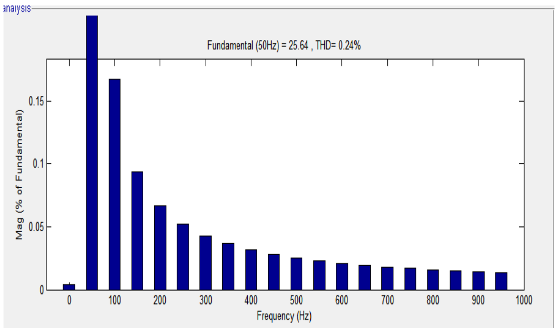


Fig 21 Simulation waveform of Harmonic analysis

V CONCLUSION

A BL-Cuk converter based 2 kW AWPS has been designed with low input current THD and less conduction losses. The proposed circuit topology is a good solution as it offers excellent PFC features at the front end while the FB converter provides output isolation along with the over-current and startup protection. The component count has also reduced by integrating two power conversion stages. The quality of weld is enhanced by controlling the output side parameters to regulate the heat and mass input to the weld pool. Furthermore, it can be inferred from the obtained results that the proposed BL converter based system has provided robustness and fast response. It is evident from the obtained results that the THD of the AC mains current is well below 5% for both full load as well as light load conditions and for the complete range of operating AC mains voltage from 170V to 270V. The PF has also remained close to unity making it suitable for wide-range of line/load operations. In all, it can be concluded that the proposed BL converter based topology conforms to the requirements of the international standard IEC 61000-3-2 expected out of an AWPS.

REFERENCES

[1] J. Schupp, W. Fischer and H. Mecke, “Welding arc control with power electronics”, in Proc. Of Power Electronics and Variable Speed Drives, 2000, pp. 443-450.

[2] J. Shklovski and K.Janson, “Development of constant-power source for arc welding”, in Proc. of Biennial Baltic Electronics Conference (BEC), 2012, pp. 255-258.

[3] B. Singh, S. Singh, A. Chandra and K. Al-Haddad, “Comprehensive Study of Single-Phase AC-DC Power Factor Corrected Converters with High-Frequency Isolation”, IEEE Trans. on Industrial Informatics, vol. 7, no. 4, pp. 540-556, Nov. 2011.

[4] L. Huber, Y. Jang, and M. M. Jovanovic, “Performance Evaluation of Bridgeless PFC Boost Rectifiers,” IEEE Trans. Power Electronics, vol. 23, pp. 1381-1390, May 2008.

[5] Limits for Harmonic Current Emissions, International Electro technical Commission Standard, 61000-3-2, 2004.

[6] M. Brkovic and S. Cuk, “Input current shaper using Cuk converter,” in Proc. of IEEE INTELEC’92, 1992, pp. 532-539.

[7] A.A. Fardoun, E.H. Ismail, A.J. Sabzali and M.A. Al-Saffar, “A Comparison between Three Proposed Bridgeless Cuk Rectifiers and Conventional Topology for Power Factor Correction”, in Proc. of IEEE ICSET, 2010, pp. 1-6.

[8] B. Singh and V. Bist, “Improved power quality bridgeless cuk converter fed brushless DC motor drive for air conditioning system”, IET Power Electronics, vol. 6, no. 5, pp. 902-913, 2013.