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A Low-Noise Transimpedance Amplifier For Blm-Based Ion Channel Recording

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ABSTRACT

High-throughput screening (HTS) using ion channel recording is a powerful drug discovery technique in pharmacology. Ion channel recording with planar bilayer lipid membranes (BLM) is scalable and has very high sensitivity. A HTS system based on BLM ion channel recording faces three main challenges: (i) design of scalable microfluidic devices; (ii) design of compact ultra-low-noise transimpedance amplifiers able to detect currents in the pA range with bandwidth >10 kHz; (iii) design of compact, robust and scalable systems that integrate these two elements. This paper presents a low-noise transimpedance amplifier with integrated A/D conversion realized in CMOS 0.35 μm technology. The CMOS amplifier acquires currents in the range ±200 pA and ±20 nA, with 100 kHz bandwidth while dissipating 41 mW. An integrated digital offset compensation loop balances any voltage offsets from Ag/AgCl electrodes. The measured open-input input-referred noise current is as low as 4 fA/√Hz at ±200 pA range. The current amplifier is embedded in an integrated platform, together with a microfluidic device, for current recording from ion channels. Gramicidin-A, α-haemolysin and KcsA potassium channels have been used to prove both the platform and the current-to-digital converter.

Keywords:

transimpedance amplifier; current sensing circuit; low-noise amplifier; low-noise current sensor; noise; ion channel recording; bilayer lipid membranes; electrophysiology

Introduction

Ion channels are nanoscale pores that sit in the cell membrane, allowing communication of the cell with the external environment through ionic currents. The open/close behavior of ion channel is modulated through different mechanisms, e.g., voltage, ligand binding, pH change, or mechanical strain. Channels are crucial for the control of physiology and any malfunction is at the root of a variety of pathologies and diseases [1]. Ion channel recording is an important component of the next generation HTS diagnostic tools used for drug discovery, DNA sequencing and single molecule detection [2]. There are two main techniques for ion channel screening:

i. Patch clamp, where a glass pipette, or a micro-aperture in a solid-state device is used to pull a patch of cell membrane [1,3,4] (Figure 1).

ii. Planar bilayer lipid membranes (BLM), where a single ion channel is inserted into a lipid bilayer suspended over a micro-aperture [5] (Figure 1).

Again the current is read by a low-noise transimpedance amplifier. The picture also shows the electrical equivalent model of the BLM, consisting of a high value resistor (of the order of GΩ or greater) in parallel with a capacitance C_S.

The patch-clamp technique is widely used in modern HTS instruments. The advantages of patch-clamp are high fidelity, since the ion channels exist in their native physiological environment, together with a high level of automation and parallelization [4,6]. This technique suffers from low specificity and high noise since a number of different ion channels are measured together, and also the membrane provides a large capacitance. On the contrary, BLM technique provide excellent electrical sealing and high sensitivity detection, down to single molecule, with minimum noise and capacitance [7,8,9]. The design of HTS system based on BLM ion channel recording faces three main challenges [10]:

i. A microfluidic device allowing stable, reliable and automatic BLM formation.

ii. A fast low-noise electronic interface ables to acquire pA currents.

iii. A compact, robust and scalable system containing an array of microfluidic devices and electronic interface.

This paper focuses on the second challenge above; the other two challenges have been discussed previously [11,12,13]. The electronic readout is a key element in the design of a BLM-based HTS system. The main requirements for the electronic interface are low-noise (noise floor <10 fA/√Hz), high-sensitivity (transresistance >1 GΩ) and wide-bandwidth (>10 kHz) [14,15]. Specific requirements are mainly related to the kind of ion channel under investigation. For instance, potassium ion channels, such as KcsA, have fast responses (100 μs) and zero-voltage conductivity lower than 100 pS, resulting in currents of the order of a few pA with applied voltages lower than 100 mV [16]. In general an ion channel has (i) very high output impedance (from 1 to 100 GΩ); (ii) noise level smaller than 1 pArms at 1 kHz; (iii) open/close events ranging from few milli-seconds to hundreds of micro-seconds and (iv) capacitance of the order of tens of pF [10,15,17].

The benchmark for low-noise low-current recording is the Axon Axopatch 200B, which has 100 kHz bandwidth and input-referred noise of 6 fA/√Hz in resistive mode and of 0.7 fA/√Hz in capacitive mode, but it is a bulky instrument not suitable for parallel recording [18]. A great number of low-noise low-current readout circuits have been presented in the literature in the last few years, but none of them completely fits the requirements. Hsu *et al.* [19] presented two different designs both achieving 5 fA/√Hz (160 fArms at 1 kHz) but with different weaknesses: one has 560 kHz bandwidth but an insufficient gain of 100 MΩ; while the other has enough gain (4.7 GΩ) over a narrow bandwidth of 1 kHz. Moreover, both the circuits are realized using discrete components, so they are not the best solutions when highly-parallel (>1024 channels) HTS systems have to be designed. Jafari *et al.* [20], as well as Crescentini *et al.* [13], presented very low-noise CMOS frontends with high gain (>1 GΩ) and noise floor as low as 2 fA/√Hz (63 fArms at 1 kHz) and 3 fA/√Hz (95 fArms at 1 kHz) respectively, but they are limited in acquisition bandwidth, which was lower than 10 kHz. Rosenstein *et al.* [21] described a fast current readout IC for high-throughput DNA sequencing; the

circuit has more than 1 MHz bandwidth but the noise floor is limited to 12 fA/√Hz (380 fArms at 1 kHz).

This paper presents a low-noise transimpedance amplifier realized in CMOS 0.35 µm technology with a measured input-referred noise as low as 4 fA/√Hz (133 fArms at 1 kHz), a gain of 2.25 GΩ and 100 kHz bandwidth. The transimpedance amplifier is based on integrator-differentiator scheme [14]. The CMOS implementation is scalable in terms of the number of concurrently acquired channels while minimizing the stray input capacitance and interference, with benefits in the noise performance since the noise is linked to the input capacitance [13,14]. An integrator-differentiator scheme provides a current sensing interface with the lowest noise floor, but suffers from saturation of the integrator stage [14]. To avoid saturation while maintaining a wide acquisition bandwidth and limiting the noise sources, we propose a periodic reset of the readout circuits at frequency f_R with A/D sampling at frequency $f_S >> f_R$, disregarding the reset behavior. In this way the folding noise due to sampling is reduced and the bandwidth is not limited by the reset. A second-order delta-sigma (ΔΣ) analog-to-digital converter (ADC) oversamples the signal at 10 MHz and generates a 1-bit 10 MS/s digital stream that is decimated by digital FIR filter implemented on a FPGA. This solution simplifies the signal routing when concurrently acquiring a great number of channels, and gives a flexible bandwidth-noise trade-off to the user by acting on the oversampling ratio (OSR) parameter in the decimator filter [22]. The system also integrates a digital offset cancellation loop (OCL) balancing any voltage offset from Ag/AgCl electrodes. The amplifier has been validated, together with microfluidic devices by measuring the activity of three different ion channels: gramicidin-A, α-haemolysin and KcsA potassium channels.

Section 2 briefly presents the overall platform and the microfluidic devices then describes the implementation of the CMOS transimpedance amplifier circuit with detailed noise analysis. Finally, Section 3 reports experimental measurements and validation of the proposed readout circuit. Advances in microelectronics and biomedical technologies have made it possible to realize body area networks, brain computer interfaces and other kinds of implantable systems. Some important

applications of these systems are to analyze EEG, ECG or neural signals for further medical diagnosis and scientific research [I]. And as revealed by biological study neural signals are typically IO-lOOOflV in amplitude and span a bandwidth of O.IHz-lO kHz. Due to the electrochemical effects on the surface of electrodes while being implanted in human body, a quite large DC offset will arise, which greatly challenges the design of precise front-end amplifiers featuring low noise, high CMRR, high input impedance and electrode DC offset suppression. Meanwhile, power consumption should be minimized and bandwidth could be set wide enough for neural signals. Four gm-stage amplifiers, auto correction feedback (ACFB) loop and capacitor- coupled topologies have been used in the proposed amplifier. The capacitor-coupled topology has several merits over others such as high input impedance, raiI-to-raiI sensing and high power 978-1-4799-3282-5/14/$31.00 m014 IEEE efficiency[l]. Meanwhile, good matching between capacitors also improves the gain accuracy and CMRR. Chopping technique is widely used for high precision CMOS amplifiers to achieve low offset and low noise, which consequently brings about high frequency ripple. On-chip filters can alleviate the ripple effectively [2], but they require more area and power consumption. The ACFB loop which consumes less power and area, can achieve appreciable reduction of noise and ripples [3]. In section II, this novel architecture is presented. The Simulation results are illustrated in section III. Finally, a conclusion is drawn in section IV

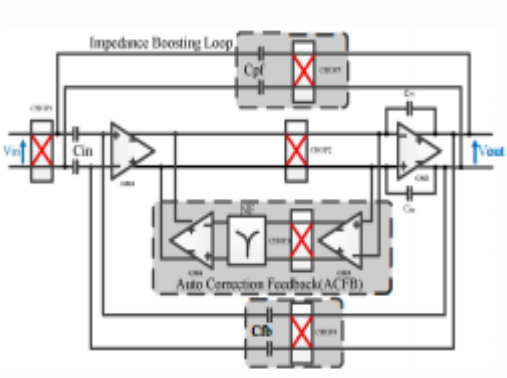

Figure I: Architecture of the whole amplifier

The Main Amplifier with ACFB :

The main amplifier employs ACFB loop to achieve low DC offset and low-frequency noise suppression, so the introduced ripple caused by the chopping can be reduced. The two stages of the main amplifier and the ripple cancellation loop is shown in the Figure 2. There is an unwanted initial input offset voltage associated with Gm], it will be

modulated by CHOP2 only, which [mally appears as ripple at the output. The ripple can be attenuated by an off chip post low pass filter at the cost of reducing the bandwidth available for the signal[3]. Furthermore, it requires additional components, area and cost for its implementation. There have already been a lot of papers reported the on-chip ripple cancellation techniques. One is to employ both auto zeroing and chopping [1], whose drawback is that it requires two input stages working in ping-pong mode so that wasting much more power and chip area for input stages. Some others also employ a switched-capacitor filter in its signal path to filter the ripple out, which consequently introduces the noise penalty due to aliasing and requires complicated design for compensation network. Amplifiers employing ACFB loop are propose in this paper. [t senses the modulated ripple at its output, and forms a local feedback loop to null out the initial offset. The proposed method is shown in Figure 1. A transconductance amplifier, paralleled to the output of the CHOP2, is employed to sense the modulated ripple, which will be demodulated down to DC by a third chopping (CHOP3)that operates with the same clock as the CHOPI and CHOP2. Then the DC signal gets through the notch filter creating a null voltage at the output of the NF. Finally the DC offset at the output of Gml will be nulled by the null voltage.

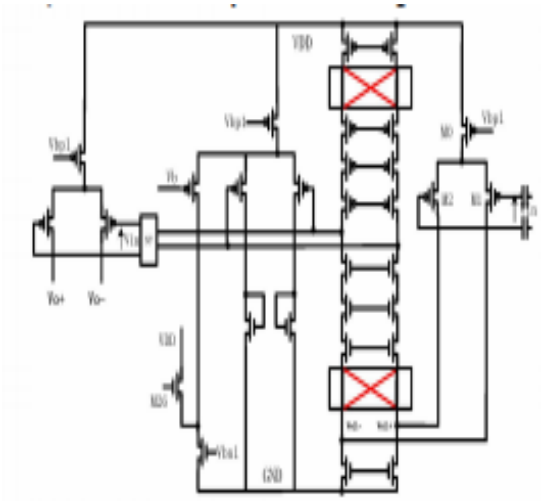

Figure 2: ACFB loop

The ACFB loop needs a really large Gm3 to ensure the whole system working in right mode. However, it will waste too much power to get this done through normal amplifier topology. So, we use a forth cascade amplifier to achieve its high gain. As shown in Figure 2, Gm3 has a gain of more than I60dB with a current below 4flA, which senses the output ripple well. M26 is working as a compensation current source to adjust the phase margin of the common mode feedback of the ACFB loop to make sure the sensed ripple will not cause oscillation. When the loop transfer function is concerned, the loop gain can be analyzed

by breaking the loop into two parts. The first part is the gain from the output of notch filter to the output of CHOP2. According to Kirchhoff's voltage law: Gm4 '' Gm2T hop F 'In+ = rchop 27r Jj.hopCm 27r JjchopCL responding to the test voltage of Vi,,, CL is the load capacitance while Cm is the miller capacitance of Gm2. The second part is the gain from the output of CHOP2 to the breaking point. The characteristic of the sinc filter is described in [5], and the combined gain is shown in (2)

The DC gain of ACFB2 is limited by the output resistance of Gm3. So the cascode topology is essential to make it large enough to suppress the residual ripple [6]. At the same time we should take care not to have much capacitance at the output of Gm3 for it creates the conductance together with CHOP3. The overall loop gain of ACFB is

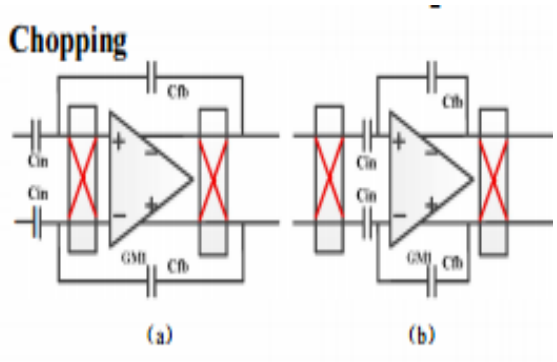

Figure 3: Two types of the location of choppers

Two types of the location of choppers The location of the chopping in this topology has a large influence on the performance of the front-end amplifier. As is proposed in the Figure 3(a), despite that the input offset can be filtered by the Cin, Cin has to be at least hundreds of pF to avoid noise performance deterioration, which will cost too much area. As a result we choose the topology in the Figure 3(b), in which Cin can only be several pF. Nevertheless, the unfiltered DC offset will be modulated into ripple. Thus, additional DC cancelling loop is needed. Impedance Boosting Loop Input impedance of Figure 1 is limited by fch' When Cin is 10pF and fch 40kHz, Rin is 1.25MO, which is too small for bio-interface. So in this topology we employed a positive feedback loop offering current to the input capacitance to boost input impedance as shown in Figure I.Here Cpf is set close to Cfb to boost impedance. Offset Isolation Capacities As shown in the Figure 2, in the ACFB loop what we need is a large Gm3. While the DC offset in the input of Gm2, wherever it comes from, may satisfy the third transconductance amplifier easily that would made the whole work of ACFB loop crash in vain. So in the input of Gm3 we

employed two isolation capacities to separate the DC offset.

The comparison with other amplifier is summarized in Table 1, from which it could be concluded that this proposed front-end amplifier offers technical advantages of reasonable low power, low noise, high input impedance and high CMRR for bio-signal.

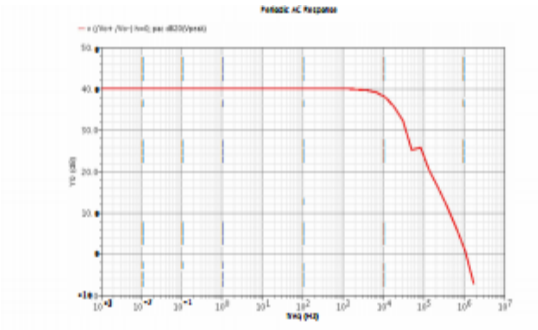

Figure 4: PAC analysis result

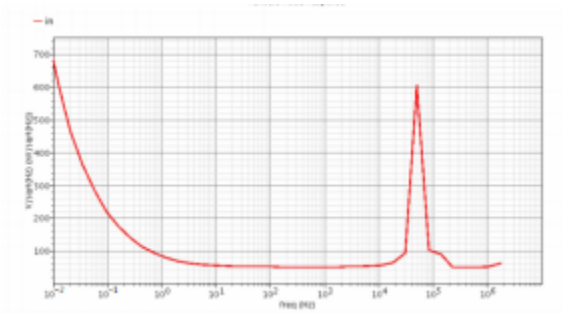

Figure 5: P-noise

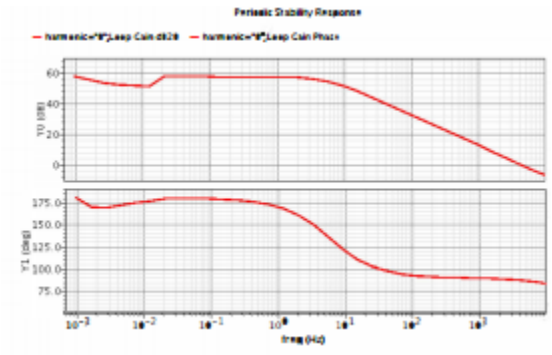

Figure 6: ACFB loop Periodic-AC result

CONCLUSION:

A front-end amplifier utilizing auto correction feedback, chopping and capacitors 978-1-4799-3282-5/14/$31.00 m014 IEEE coupled technique is proposed, which achieves a DC gain of 40dB, a GBW of 1.2MHz and input noise as 50.561nV/'I'Hz with a load capacitance of 5pF, while consuming a total current of 72/lA with a supply of 1.8V. In comparison with some published works recently, the proposed OTA has quite good performances, which indicates that it is suitable for biomedical electronics such as EEG, ECG and neural recording.

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