International Journal of Research
Available at https://edupediapublications.org/journals
p-ISSN: 2348-6848
e-ISSN: 2348-795X
Volume 03 Issue 14
October2016

DG Integration and Voltage Sag Compensation using Dynamic Voltage Restorer

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Abstract-The dynamic voltage restorer (DVR) is a custom power device used for voltage compensation of sensitive loads against voltage disturbances in power distribution lines. The DVR can regulate the load voltage from the problems such as sag, swell, and harmonics in the supply voltages. Hence, it can protect the critical consumer loads from tripping and consequent losses. The existing control strategies either mitigate the phase jump or improve the utilization of dc link energy by the following: 1) reducing the amplitude of the injected voltage or 2) optimizing the dc bus energy support. In this paper, an enhanced sag compensation strategy is proposed, which mitigates the phase jump in the load voltage while improving the overall sag compensation time. An analytical study shows that the proposed method significantly increases the DVR sag support time compared with the existing phase jump compensation methods. The simulation results are presented by using Matlab/Simulink software.

Index Terms—Dynamic voltage restorer (DVR), voltage phase jump compensation, voltage sag compensation, voltage source inverter (VSI).

I. INTRODUCTION

In the early days of power transmission voltage deviation during load changes, power transfer limitation was observed due to reactive power unbalances. Modern power systems are complex networks, where hundreds of generating stations and thousands of load centers are interconnected through long power transmission and distribution networks [1-2]. The main concern of customer is the quality and reliability of power supply at various load centers. Even though power generation in most well-developed countries is fairly reliable, the quality of supply is not. Power distribution system should ideally provide their customers an uninterrupted flow of energy with smooth sinusoidal voltage at the contracted magnitude and frequency [3]. However, in practice power system especially the distribution system, have numerous non-linear loads, which are significantly affect the quality of power supply. As a result, the purity of waveform of supply lost. This ends up producing many power quality problems [4].

To improve power quality, custom power devices are used. In 1995 the concept of custom power is first explained by Hingorani [5-7]. The thought of custom power (CP) identifies with the utilization of electronic controllers for power system network. There are number of custom power units which are given below, Distribution Statcom (DSTATCOM), Dynamic Voltage Restorer (DVR), Unified power quality conditioner (UPQC), Active
Power Filters, Battery Systems (BESS), Distribution Series Capacitors (DSC), Surge Arresters (SA), Un-interruptible
Power Supplies (UPS), Solid State Fault Current Limiter (SSFCL), Solid-State Transfer Switches (SSTS), and Static Electronic Tap Changers (SETC) [8]. Dynamic Voltage Restoration (DVR) is a method and apparatus used to sustain, or restore, an operational electric load during sags, or spikes, in voltage supply. DVRs are a class of custom power devices for providing reliable distribution power quality. They employ a series of voltage boost technology using solid state switches for compensating sags/swells [9-11].

II. OVERVIEW OF DVR OPERATION

In this section, different sag compensation approaches [12] are briefly discussed. The phasor representations of these methods are given in Fig.1. The phasor $\underset{V_G}{\rightarrow}$and $\underset{V_G}{\rightarrow}$represent the rated and sagged grid voltages, respectively, whereas $\underset{V_L}{\rightarrow}$and $\underset{V_L}{\rightarrow}$are the load voltages before and after the sag. To effectively highlight the differences mong these methods, P_{DVR} and Q_{DVR} are also incorporated in the phasor diagrams. This is mainly to illustrate the amount of active and reactive powers demanded by each method. All of the quantities are drawn considering the load current $(\underset{I_L}{\rightarrow})$as reference phasor.

A .In-Phase Compensation

In this type of compensation, DVR injects the smallest possible voltage magnitude in phase with the sagged grid voltage. However, as seen from Fig.2(a),

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Volume 03 Issue 14
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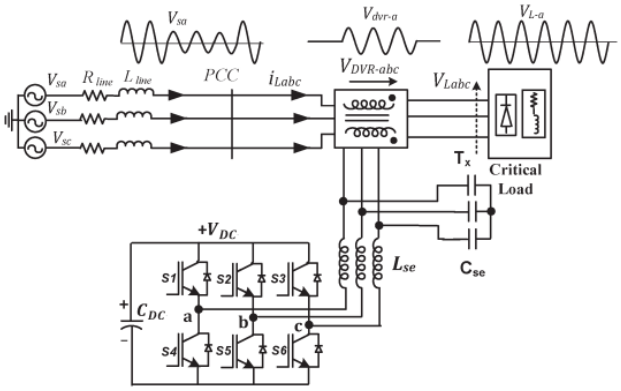

Fig. 1. Basic DVR-based system configuration.

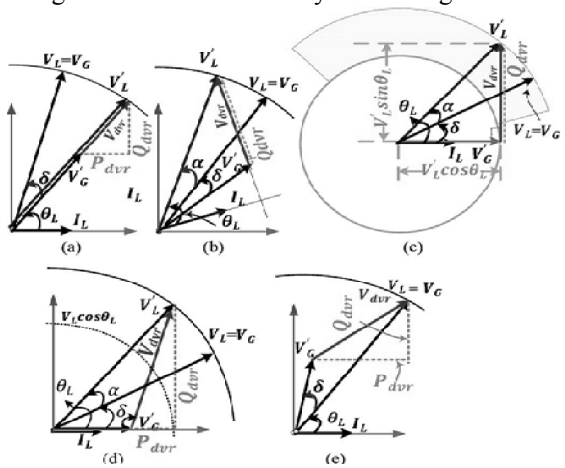

Fig.2. Per-phase phasor representation of the basic compensation topologies for DVR. (a) In-phase injection. (b) Quadrature injection. (c) Quadrature injection limiting case. (d) Energy-optimized injection (e) Presag injection.

This method cannot correct the phase jump. The DVR-injected voltage magnitude and angle are given as

$$V_{\mathrm{DVR}} = \sqrt{2}\,(V_L - V_G') \tag{1}$$

$$\angle V_{\mathrm{DVR}} = \theta_L. \tag{2}$$

B. Quadrature Injection (Reactive Compensation)

In this method, the DVR injects voltage in quadrature with the load current, i.e., it corrects the sag with only reactive power. Using Fig.2 (b), the injected voltage magnitude and angle are given as

$$V_{\mathrm{DVR}} = \sqrt{2}\sqrt{V_L^2 + V_G'^2 - 2V_L V_G' \cos(\alpha + \delta)} \tag{3}$$

$$\angle V_{\mathrm{DVR}} = \frac{\pi}{2} \tag{4}$$

Where δ is the phase jump in the grid voltage due to the sag and α is the phase jump induced due to reactive power compensation. As reported in [12], the maximum sag depth (ΔVsag, max) that can be compensated using quadrature injection is closely related with the load power factor and can be expressed as

$$\Delta V_{\mathrm{sag-max}} \leq (1 - \cos\theta_L) \tag{5}$$

The corresponding maximum injected voltage is given

$$V_{\mathrm{DVR-max}} = \frac{V_G'}{1 - \Delta V_{\mathrm{sag,max}}} \sin\theta_L \tag{6}$$

Fig.2(c) shows the limiting case for quadrature injection where DVR supports the full load reactive power while the grid operates at unity power factor

C. Energy-Optimized Injection

This method is developed to enhance the performance of the quadrature injection method for the sag depth deeper than the limit in (5), where the DVR injects certain active power. The DVR voltage magnitude and injection angle can be calculated from Fig.2 (d)

$$V_{\mathrm{DVR}} = \sqrt{2}\sqrt{V_L^2 + V_G'^2 - 2V_L V_G' \cos(\theta_L)} \tag{7}$$

$$\angle V_{\mathrm{DVR}} = \tan^{-1}\left(\frac{V_L(\sin\theta_L)}{V_L\cos\theta_L - V_G'}\right) \tag{8}$$

D. Presag Compensation

In this method, both load voltage magnitude and phase are restored to presag values. Unlike the previous methods in Fig .2(a), (b), and (d), the presag method in Fig .2(e) can successfully compensate the phase jump. However, this phase jump correction requires an additional active power from the dc link capacitor. A positive phase jump leads to an increase in angle between the grid voltage and the load current, increasing the active power burden on DVR compared to negative phase jump. Using Fig .2(e), the injected voltage magnitude and angle can be written as

$$V_{\mathrm{DVR}} = \sqrt{2}\sqrt{V_L^2 + V_G'^2 - 2V_L V_G' \cos(\delta)} \tag{9}$$

$$\angle V_{\mathrm{DVR}} = \tan^{-1}\left(\frac{V_L\sin\theta_L - V_G'\sin(\theta_L - \delta)}{V_L\cos\theta_L - V_G'\cos(\theta_L - \delta)}\right) \tag{10}$$

III. POWER FLOW ANALYSIS AND MAXIMUM COMPENSATION TIME

As explained earlier, the presag method is the most energy intensive method, and the injected power can be quite high even for shallow sag depths. Based on the phasor diagram of Fig.2(e) [(9) and (10)], the active

power associated with the presag method can be expressed in terms of sag depth, phase jump, and load power factor as given in the following:

$$P_{\text{presag}} = \sqrt{3}V_L I_L\left(\cos(\theta_L) - (1 - \Delta V_{\text{sag}})\cos(\theta_L - \delta)\right) \quad (11)$$

A detailed derivation of (11) is given in Appendix A. the DVR active power for a range of variation in sag depth ($0.1 \le \Delta V_{sag} \le 0.9$) and power factor ($0.4 \le \cos\theta_L \le 0.9$). The phase jump δ is fixed at +25◦. As seen from the graph of the active power supplied by DVR is relatively high (>0.4 p.u.) for the presag method. The theoretical power flow analysis conducted previously holds true as long as there is a significant amount of energy in the dc link capacitor. However, in the actual system, since it has a finite amount of energy, the voltage across the dc link capacitor V_{dc} reduces. The following relationship should be satisfied at all time in order to achieve the adequate operation of DVR-VSI.

$$\frac{V_{\text{dvr}}}{n_t} \le \frac{m_{i-\max} V_{\text{dc}}}{2} \quad (12)$$

Where $n_t$is the turns ratio of the series transformer and m_{i-max} is the maximum modulation index of VSI. V_{dvr} is the injected phase to neutral voltage. V_{dc} is the dc link voltage. As soon as the dc link voltage decreases below V_{dc-min}, i.e., the limit set by (12), the DVR controller must stop the compensation process to avoid harmonics contamination in the load voltage.The energy stored in the dc link capacitor is equal to

$$E_{c-\text{dc}} = \frac{1}{2} C_{\text{dc}} V_{\text{dc}}^2 \quad (13)$$

The power flow out of the dc link capacitor in the steady state is given as

$$P_{c-\text{dc}} = \frac{1}{2} C_{\text{dc}} \frac{d}{dt} V_{\text{dc}}^2 \quad (14)$$

Considering a lossless DVR system, the dc power in (14) can be equated with the ac power of (11) to find the capacitor size. However, owing to the flow of active power, the dc link voltage drops, and the limit in (12) can be violated. This limitation restrains the DVR operation even though there is sufficient amount of stored energy in the dc link capacitor. Furthermore, the gradient of the dc link voltage d_{vdc}/dt is directly proportional to the DVR-injected active power, i.e., P_{dvr}. The lower the value of P_{dvr}, the smaller is the slope of the dc link voltage and the higher will be the time for which

$$V_{\text{dvr}}/n_t \le (m_{i-\max} V_{\text{dc}})/2.$$

This leads to the following two hypotheses.
1) The energy stored in the dc link capacitor can further be utilized.
2) The rate of change (fall) of the dc link voltage can further be optimized.
This brings another important variable in the power flow analysis which is the "maximum compensation time t_{c-max}." It is the direct measure of "useful" stored charge/energy in the dc link capacitor. The t_{c-max} can be determined from the boundary condition of (12) and (14) as given in the following:

$$t_{c-\max} = \frac{C * \left[V_{\text{dc}}^2 - \left(\frac{2 * V_{\text{dvr}}}{m_{i-\max} * n_t}\right)^2\right]}{2 * P_{\text{dvr}}} \quad (15)$$

A detailed derivation of (15) is given in Appendix B. To increase t_{c-max}, Meyer *et al.* suggested a method which decrease the injected voltage magnitude once the dc link voltage dropped to the threshold limit of (12) and allows further utilization of the dc link stored energy. However, as discussed in the introduction section, this method has no control on the injected active power and therefore is not the best choice for getting the maximum compensation time.

IV. PROPOSED COMPENSATION SCHEME

The work presented in this paper proposes an enhanced sag compensation method to extend the DVR compensation time. It optimizes the gradient of the dc link voltage (d_{vdc}/dt) by regulating the amount of active power injected by DVR. In the proposed method, the controller restores both phase and amplitude of the load voltage to the presag value and then initiates a transition toward the minimum active power (MAP) mode. The overall operation sequence and implementation of the proposed compensation method is discussed in the following subsections.

A. Phase Jump Detection and Presag Restoration

For detecting the phase jump, two PLLs are employed (one over the load voltage and another over the source voltage), giving θ_{VL} and θ_{Vg}, respectively. As soon as the sag is detected,the first step is to determine the DVR initial injection angle that avoids the phase jump at the load side. This is done by freezing the load voltage PLL that gives the presag angle (θ_{VLp}). On the other hand, the unrestricted grid voltage PLL gives the grid voltage phase (θ_{Vg}). The difference between these two angles gives the initial angle of injection Note that, in the steady state, both angles will be identical, and thus, the

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difference will be zero. For sag detection, the absolute difference between the reference load voltage (1 p.u.) and the actual grid voltage (p.u.) in synchronous reference frame is calculated as follows [7]

$$\left.\begin{aligned}\theta_{\text{init}} &= \theta_L + (\theta_{VLp} - \theta_{Vg}) \\ &= \theta_L + \delta\end{aligned}\right\} \quad (16)$$

$$\Delta V_{\text{sag}} = \left|1 - \sqrt{V_{gd}^2 + V_{gq}^2}\right| \quad (17)$$

As soon as ΔVsag >0.1, it is recognized as voltage sag.

B .Controlled Transition toward the MAP Mode

Once the presag voltage is successfully restored, after one cycle, a smooth transition toward the MAP mode is initiated and completed over the next one to two cycles. The final injection angle of DVR (θ_{fin}) is given as

$$\theta_{\text{fin}} = \begin{cases} \frac{\pi}{2} + \gamma, & \text{if } \Delta V_{\text{sag}} \le (1 - \cos\theta_L) \\ \pi - \tan^{-1}\left(\frac{V_L(\sin\theta_L)}{V_L\cos\theta_L - V_g'}\right), & \text{if } \Delta V_{\text{sag}} > (1 - \cos\theta_L) \end{cases} \quad (18)$$

A detailed derivation of (18) is given in Appendix C. The first part of (18) represents the self-supporting mode of operation in which the DVR absorbs active power (relatively very small amount) from the grid to overcome the system losses and thus maintains a constant voltage across the dc link capacitor. The term γ indicates the reduction in θ_{fin} due to loss component and is determined by the dc link (PI) controller. The second part of (18) represents a case where the self-supported dc link cannot be maintained due the constraint in (5). To ensure a smooth changeover, a transition ramp is defined between the initial and final operating points, as given in the following:

$$\theta_{\text{trans}} = \theta_{\text{init}} + \frac{\theta_{\text{fin}} - \theta_{\text{init}}}{\Delta T}(t) \quad (19)$$

Where ΔT determines the slope of the transition curve and is chosen as 30 ms.

C. Iterative Decrement in Injection Angle

In self-supporting mode, the DVR can compensate the sag for an indefinitely long time. However, for deeper sag depths, there is certain nonzero active power injected by DVR. This causes a reduction in the energy stored in the dc link capacitor, and consequently, its voltage reduces (gradually). To maintain the required voltage at the inverter output side, the controller increases the modulation index m_i until it reaches $m_{i-\max}$. This is the limiting case as explained by (12), beyond which the controller goes into over modulation and cannot maintain the rated load voltage. To avoid this over modulation condition, an iterative control loop is used, which constantly monitors the dc link voltage and decreases θ_{fin} in (18) to keep $V_{\text{dc}} > V_{\text{dc-min}}$ and is given as

$$\theta_{\text{fin}} = \theta_{\text{fin}} - \epsilon \quad (20)$$

Where ϵ *is* chosen as 0.01 rad.

V. OVERALL DVR SYSTEM CONTROL SCHEME

Fig.3 depicts the detailed block diagram of the proposed phase jump compensation method. A logic unit is employed to constantly monitor the grid voltage for sag detection using (17). To obtain the reference load voltage, the control system is divided into two sub modules: 1) phase jump detection plus DVR injection angle calculation and (2) MAP injection. To achieve a decoupled active and reactive power control, the phase of theline current is considered as the reference and is obtained by the PLL. The phase jump detection block computes the DVR initial (presag injection) angle and final (MAP injection) angle. Once the transition is over, the MAP block gives the reference voltage $V_{L*-abc} = V_{opt}$. As shown in Fig.3, the obtained DVR reference voltage $V_{dvr*}$is compared with the actual voltage in the stationary reference frame. A proportional-resonant (PR) controller with a large gain at the grid fundamental frequency is used for accurate tracking of V_{dvr*}. To compensate or DVR system losses, $V_{dvr*}$is added as a feed forward signal to the output of the PR controller. The dc link voltage is constantly monitored in an iterative control loop to regulate the injected voltage angle, thus avoiding over modulation. Note that this block is only required when the sag depth is close to the system design limit.

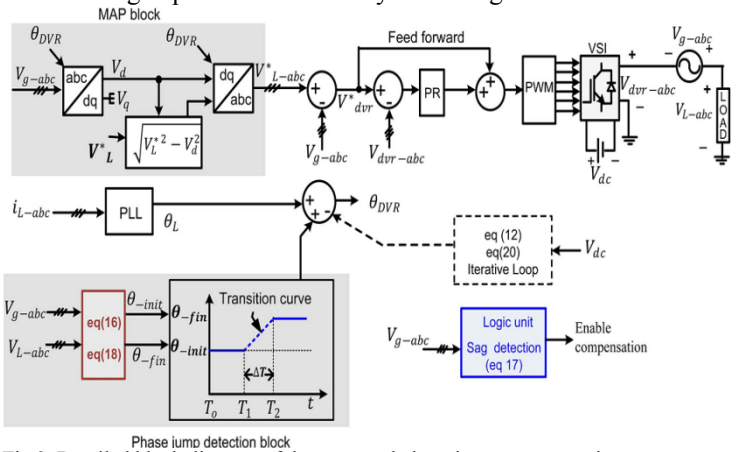

Fig.2. Detailed block diagram of the proposed phase jump compensation method with MAP injection.

VI A PHOTOVOLTAIC SYSTEM

International Journal of Research
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p-ISSN: 2348-6848
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Volume 03 Issue 14
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A photovoltaic system, converts the light received from the sun into electric energy. In this system, semi conductive materials are used in the construction of solar cells, which transform the self contained energy of photons into electricity, when they are exposed to sun light. The cells are placed in an array that is either fixed or moving to keep tracking the sun in order to generate the maximum power [9]. These systems are environmental friendly without any kind of emission, easy to use, with simple designs and it does not require any other fuel than solar light. On the other hand, they need large spaces and the initial cost is high.
PV array are formed by combine no of solar cell in series and in parallel. A simple solar cell equivalent circuit model is shown in figure. To enhance the performance or rating no of cell are combine. Solar cell are connected in series to provide greater output voltage and combined in parallel to increase the current. Hence a particular PV array is the combination of several PV module connected in series and parallel. A module is the combination of no of solar cells connected in series and parallel.

The photovoltaic system converts sunlight directly to electricity without having any disastrous effect on our environment. The basic segment of PV array is PV cell, which is just a simple p-n junction device. The fig.1.4 manifests the equivalent circuit of PV cell. Equivalent circuit has a current source (photocurrent), a diode parallel to it, a resistor in series describing an internal resistance to the flow of current and a shunt resistance which expresses a leakage current. The current supplied to the load can be given as.

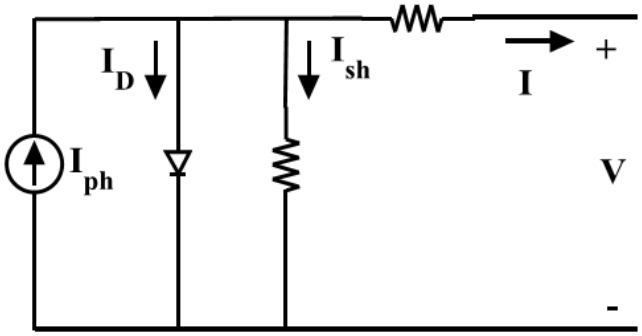

Fig 3 Equivalent circuit of Single diode modal of a solar cell

$$I = I_{PV} - I_O\left[\exp\left(\frac{V+IR_S}{aV_T}\right)-1\right]-\left(\frac{V+IR_S}{R_P}\right)$$

Where
IPV–Photocurrent current,
IO–diode's Reverse saturation current,
V–Voltage across the diode,
a– Ideality factor
VT –Thermal voltage
Rs – Series resistance Rp –Shunt resistance

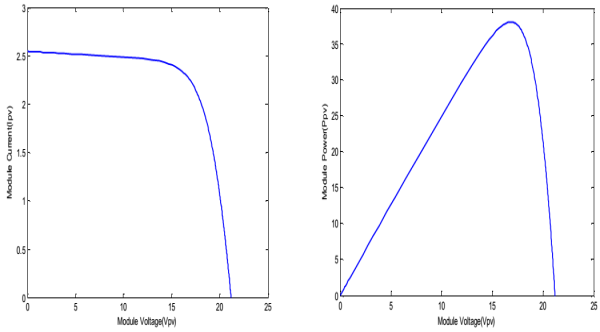

Fig.4 V-I & P-V Characteristics of a 36w PV module

VII .MATLAB/SIMULATION RESULTS

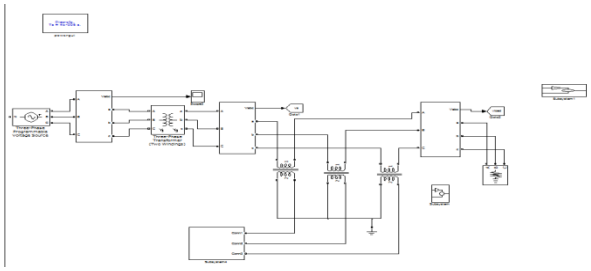
Fig 5 Matlab/simulation circuit of DVR-based system configuration.

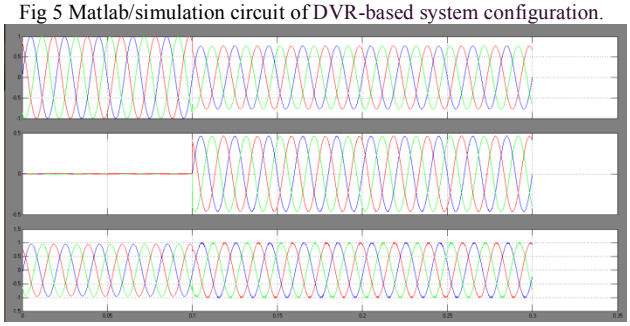
Fig 6 simulation wave form of source voltage, load voltage and DVR compensation output voltage of 25 %

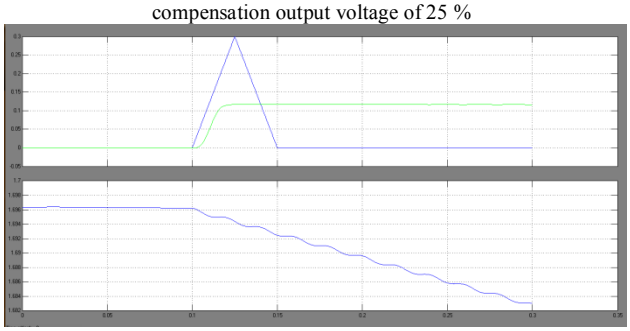
Fig 7 simulation wave form of active and reactive dc power and dc voltage of 25%

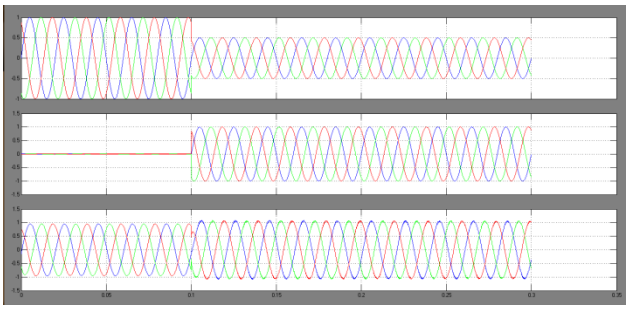

Fig 8 simulation wave form of source voltage, load voltage and DVR compensation output voltage of 50%

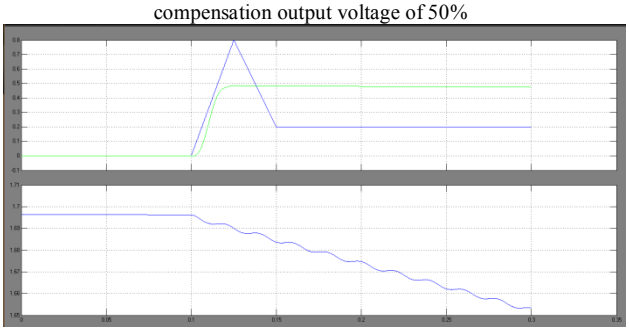

Fig 9 simulation wave form of active and reactive dc power and dc voltage of 50%

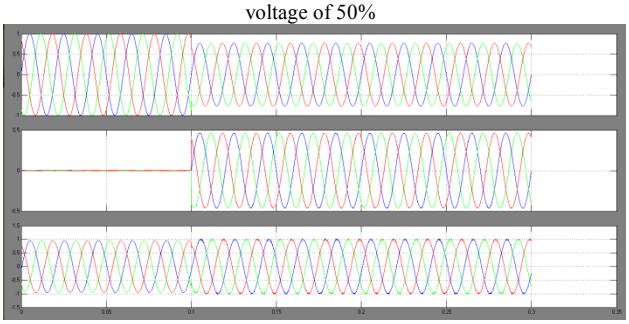

Fig 10 simulation wave form of source voltage, load voltage and DVR compensation output voltage with PV and UC

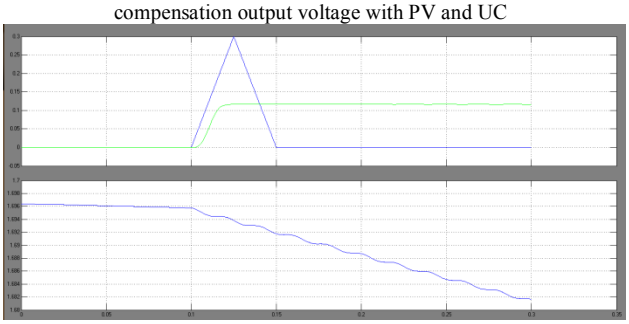

Fig 11 simulation wave form of active and reactive dc power and dc voltage with PV and UC

VII.CONCLUSIONS

This paper presents power and voltage quality problems such as voltage sage, swells and others. Also an overview of dynamic voltage restorer (DVR) is presented. DVRs are effective recent custom power devices for voltage sags and swells compensation. They inject the appropriate voltage component to correct rapidly any anomaly in the supply voltage to keep the load voltage balanced and constant at the nominal value. It is shown that the compensation time can be extended from 10 to 25 cycles (considering pre sag injection as the reference method) for the designed limit of 50% sag depth with 45◦ phase jump. Further extension in compensation time can be achieved for intermediate sag depths. This extended compensation time can be seen as a considerable reduction in dc link capacitor size (for the studied case more than 50%) for the new installation. The effectiveness of the proposed method has been evaluated with PV and UC in the DG through extensive simulations in MATLAB/Simulink.

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