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Enhancing Performance of Fuzzy controlled based New Hybrid Unified Power Quality Conditioner (HUPQC)

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Abstract: With the widespread use of large-capacity power electronic devices, there are too much harmonic current and harmonic voltage in power system at the same time. The active power filter (APF) or hybrid active power filter (HAPF) can only eliminate harmonic current or harmonic voltage, and possibility resonance. To eliminate harmonic current and harmonic voltage in power system simultaneously and enhance the capacity, the concept presents a hybrid unified power quality conditioner (HUPQC). Compared with UPQC, the HUPQC is made up of a hybrid series active power filter (the series device) and a shunt active power filter (the shunt device). The shunt device employs an injection circuit to lower the capacity of the active part to fit high-voltage power system. Designed reasonably, and controlled with composite control method, the HUPQC can filter the harmonic current and harmonic voltage effectively at the same time. At the end of this concept, the simulation results improve that the HUPQC can prove the power quality greatly and achieve satisfactory effect.The proposed concept is further implemented to Fuzzy controlled concept using Matlab/Simulink software

Keywords— Power Quality, Hybrid Unified Power Quality Conditioner, Shunt Hybrid APF, DVR, DC-DC Converter

I INTRODUCTION

Evolution in characteristics of electrical loads as a result of developing technology and rapidly increasing electricity demand cause electrical power quality to become an important issue. The most common electrical power quality problems in electrical distribution systems are sags, swells, voltage and current harmonics. Due to the inadequate performance of traditional compensation devices, development of advanced technology power electronics based compensation devices is needed for compensation of these power quality problems. With the increasing power quality problems in distribution systems, unified power quality conditioner (UPQC), which is formed from shunt APF and DVR connected to common dc link, is developed. UPQC is an advanced compensation system that is used for compensation of power quality problems such as voltage sag swell, current-voltage harmonics, voltage ripple, voltage-current imbalances, voltage flicker and reactive power compensation [1-4].

In recent papers related with UPQC, various UPQC topologies have been proposed for different purposes such as the multilevel UPQC [5] based on a three level neutral point clamped topology; the interline UPQC [6] where the series and shunt VSIs are connected to neigh boring feeders; the multi converter UPQC [7] in which three or more VSIs are applied to adjacent feeders similar to the interline UPQC; the modular UPQC [8,9] which is carried out by connecting several H-bridge VSI modules in cascade in each phase; the open UPQC [10,11] in which the series and shunt VSIs do not share a common dc link. In [12-14], UPQC topologies that include DC-DC converters in their DC links are suggested. In these studies DC-DC converters are used for charging energy storage devices in dc link of UPQC and in [15] are used for maintaining isolation between series and parallel inverters. In [16-19] hybrid UPQC topology formed from connection of DVR and SHAPF on common DC link is recommended.

In this paper, a new HUPQC topology is introduced that the dc link connection of shunt hybrid APF and DVR are realized by isolated bi-directional DC-DC converter. The rest of this paper is organized as follows: System description and power circuit topology of the proposed HUPQC is presented in Section 2. Control strategy is introduced in Section 3. Simulation results for different case studies are provided and discussed in Section 4. Conclusions of the study are given in Section 5.

II PROPOSED HUPQC SYSTEM:

The structure of the proposed HUPQC connected to a distribution system is shown in Fig. 1. As shown in this figure, HUPQC consists of a DVR, a SHAPF and an isolated bidirectional DC-DC converter. The DVR is connected in series with busbar through injection transformers *TR2*, *TR3* and *TR4* for each phase respectively. The SHAPF, which consists of passive filter and active power filter, is connected in parallel with nonlinear and sensitive loads at the end of busbar. The DVR and the SHAPF are connected back to back on their dc side via the isolated bi-directional DC-DC converter. The isolated bi-directional DC-DC converter is comprised of two symmetric H-bridge inverter, auxiliary reactances (*Ldc1* and *Ldc2*) and a high frequency transformer (*TR5*). The busbar is supplied from utility grid through a delta/wye power transformer (*TR1*). The nonlinear load is

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formed from a three phase diode rectifier load which supplies an *RC* load with 3% line reactor. The sensitive load contains balanced *RL* loads that need purely sinusoidal voltages and must be fully protected against voltage distortions such as sag and swell. The system parameters of the proposed HUPQC are provided

III HUPQC CONTROL SYSTEM:

The HUPQC control system is based on Synchronous Reference Frame (SRF) where the DVR and SHAPF inverters are controlled independently. By using the SRF based controller, the fundamental component of load currents and source voltages are derived in order to obtain the reference current and voltage waveforms and thus to produce the switching signals properly.

A. SHAPF Controller:

The control scheme of the SHAPF is based on synchronous reference frame method which presents easy implementation and low computational cost. Functions of the SHAPF controller are to compensate for the harmonic components of nonlinear load current and to regulate the voltage of the dc link capacitor (*Cdc2*). The controller of SHAPF is mainly formed from harmonic current reference generation and current controller, dc link voltage controller and PWM controller as shown in Fig. 2.

The harmonic compensation is performed by using direct current control strategy. The harmonic reference current is generated from load currents by using the SRF technique. The load currents (*ILa, ILb, ILc*) are firstly transformed in to dq domain (*ILd, ILq*) by using dq transformation and then passed

TABLE 1. SYSTEM PARAMETERS OF THE PROPOSED HUPQC

System Parameters	Values
Fundamental Frequency	f = 50 Hz
Switching Frequencies	DVR: 10 kHz, SHAPF: 20 kHz, DC-DC Converter: 20 kHz
Utility Supply	31.5 kV (L-L), phase angle 0°
Short Circuit Power	100 MVA, (R_s=0.496 ohm, L_s= 31.6 mH)
Step-down Transformer	*(TR1)* 1 MVA, Δ/Y, 31.5/0.4 kV, 5% leakage reactance
Busbar Voltage	V_s = 380 V (L-L)
Injection Transformer	*(TR2, TR3, TR4)* 4 KVA, 50 Hz, 150/150 V, 1% leakage reactance
Inverter side filter	Cut of freq.= 918 Hz, L_f=0.2 mH, C_f=150 uF, R_f=0.5 ohm, Damping resistor (R_d)=1 ohm
DC link Capacitor	C_{dc1} = 70 mF (DVR side)
DC Capacitor Voltage	V_{dc1} = 155 V (DVR side)
DC link Capacitor	C_{dc2} = 180 mF (SHAPF side)
DC Capacitor Voltage	V_{dc2} = 227 V (SHAPF side)
High Frequency Transformer	*(TR5)* 10 kVA, 20 kHz, 1:1, 2% leakage reactance
Auxilary Reactances	L_{dc1} = 12 uH, L_{dc2} = 18 uH
Passive Filter	Tuned Freq.=250 Hz, L_k=2 mH, C_k=200 uF
Nonlinear Load	3-phase diode rectifier that supplies RC load with 3% line reactor S = 10 kVA, THD=40%, pf = 0.97
Sensitive/Critical Load (Totally 11 kVAR)	1st load: 4 ohm, 90 mH, 5 kVAR 2nd and 3rd loads: 8 ohm, 225 mH, 2 kVAR 4th and 5th loads: 16 ohm, 450 mH, 1 kVAR

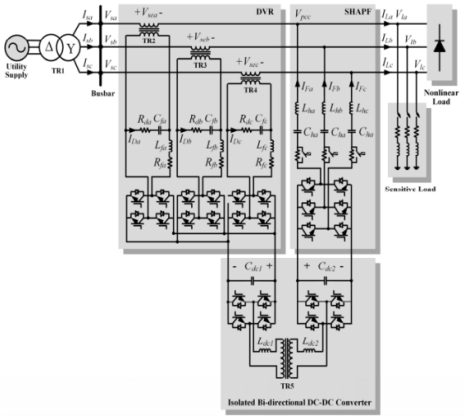

Fig.1.The structure of the proposed HUPQC system

Through a low pass filter (LPF) with cut of frequency of 10 Hz. The filtered components *(ILdfil, ILqfil)* are substracted from unfiltered components *(ILd, ILq)* to obtain harmonic current references in dq domain *(ILd,har, ILq,har)*. In order to generate the harmonic references in three phase coordinates *(ILa,har, ILb,har, I Lc,har)*, the inverse dq transformation is applied. The dq transformation matrix and the inverse transformation matix are given in *Eq. (1),(2)* and *(3),(4)* respectively.

$$T_{dq}^{abc} = \frac{2}{3}\begin{bmatrix} \sin\theta_a & \sin\left(\theta_a - 2\pi/3\right) & \sin\left(\theta_a + 2\pi/3\right) \\ \cos\theta_a & \cos\left(\theta_a - 2\pi/3\right) & \cos\left(\theta_a + 2\pi/3\right) \end{bmatrix} \quad (1)$$

$$\begin{bmatrix} I_{Ld} \\ I_{Lq} \end{bmatrix} = T_{dq}^{abc}\begin{bmatrix} I_{La} \\ I_{Lb} \\ I_{Lc} \end{bmatrix} \quad (2)$$

$$T_{abc}^{dq} = \begin{bmatrix} \sin\theta_a & \cos\theta_a \\ \sin\left(\theta_a - 2\pi/3\right) & \cos\left(\theta_a - 2\pi/3\right) \\ \sin\left(\theta_a + 2\pi/3\right) & \cos\left(\theta_a + 2\pi/3\right) \end{bmatrix} \quad (3)$$

$$\begin{bmatrix} I_{Lhara} \\ I_{Lharb} \\ I_{Lharc} \end{bmatrix} = T_{abc}^{dq}\begin{bmatrix} I_{Ld,har} \\ I_{Lq,har} \end{bmatrix} \quad (4)$$

In a similar way, the current harmonics of the SHAPF in three phase coordinate *(IFa,har, IFb,har, IFc,har)* are generated. The current harmonics of the SHAPF are then subtracted from the harmonic references *(ILa,har, ILb,har, ILc,har)* and the error signals of harmonic currents are obtained. The error signal of the current is multiplied by proportional controller *(Khar)* in order to obtain the error signal in voltage form.

The DC link voltage reference is obtained by using PI controller. In the DC link voltage controller, the

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SHAPF side DC link voltage *(Vdc2)* is subtracted from the reference value *(Vdc2ref)* and the resulting error signal (*Vdc2err*) is applied to PI controller. The DC link voltage controller reference signal *(Vdcref)* for each phases are obtained by using the inverse dq transformation matrix where the output of PI controller is the input of q component.

Finally, the three phase reference voltage signals *(Varef, V bref, Vcref)* are generated by adding up the harmonic voltage error signals and DC link voltage controller reference signals.

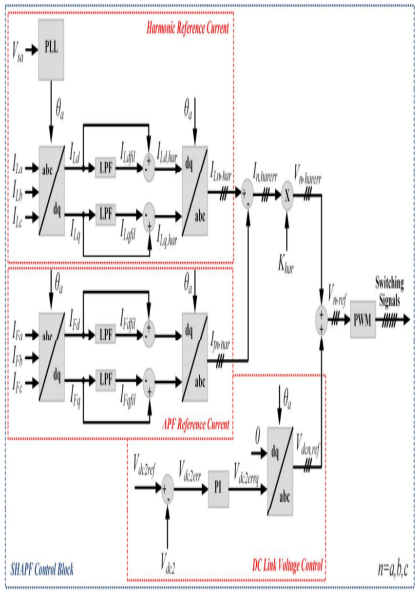

Fig.2. Block diagram of control algorithm for SHAPF

B. DVR Controller:

The controller of DVR is designed to control each phase independently that performs voltage measurements (*Vs* and *Vl*), sag/swell detection, reference voltage extraction and gate signal generation as it is presented in Fig.3.

In the proposed controller of DVR, three phase bus bar voltages (*vsa, vsb, vsc*) are measured and then the "per unit" transform is applied. The magnitude information "*A(t)*" is determined with the improved SRF based controller for each phase independently by using the per unit values of bus bar voltages and phase angles *ş(t)* obtained with EPLL. The improved SRF technique can be applied to realize the reference voltage when the unbalanced voltage sag/swell occurs unlike the conventional SRF. In the conventional SRF technique, the three phase voltage signals are used and an average magnitude value is produced as a result of calculated average values of d- and q- components for three phase. For this reason, the conventional SRF technique is not preferred in unbalanced voltage sag/swell conditions. On the other hand, the improved SRF technique produce the magnitude values separately for each phase as follows;

$$A(t)=\sqrt{V_{d,a}^2+V_{q,a}^2} \quad (5)$$

$$B(t)=\sqrt{V_{d,b}^2+V_{q,b}^2} \quad (6)$$

$$C(t)=\sqrt{V_{d,c}^2+V_{q,c}^2} \quad (7)$$

Fig.3 presents the d-q transformation for each phase by using the measured actual voltage value and the reference voltage values created virtually. The generation of reference values of two other phase are provided in Eq. (8), (9) and (10) by using the measured voltage information.

$$V_{ref,a}=V_a\angle(0^\circ) \quad (8)$$

$$V_{ref,b}=V_a\angle(-\frac{2\pi}{3})=V_a\angle(\frac{4\pi}{3})=-V_a\angle(\frac{\pi}{3}) \quad (9)$$

$$V_{ref,c}=-(V_a+V_{ref,b})=-V_a+V_a\angle(\frac{\pi}{3}) \quad (10)$$

The voltage sag/swell depth "*Sdepth*" can be found by subtracting the magnitude information from 1 pu value which should be in nominal conditon. When a sag or swell occurs, the "*S depth*" can be detected higher than the limit value of 10% (0.1 pu) and gives voltage sag/swell detection signal as a result of hysteresis comparator. The voltage sag/swell detection signal enables the PWM for each phase to produce switching signal with respect to the reference voltage.

The reference voltage is extracted in a closed loop control where the inputs are the *Sdepth*, the phase angle *ş(t)*, the load voltage *vL* and the filtering capacitor current *ID*. In closed loop controller, the feed forward voltage error *Verr* is determined firstly in according to the in-phase compensation strategy by subtracting the sag/swell voltage *(Vs)* from the reference voltage *(Vref)*. The reference voltage (*Vref)* is calculated by multiplying the 1 pu nominal voltage magnitue with *sinş(t)*. In the open loop controller, the error voltage (*Verr)* is directly fed to the PWM pulse generator through a gain *Kinv*. However, in the closed loop controller the error voltage *(Verr)* is added with the feedback voltage. In feedback block, the measured load voltage (*VL)* is firstly subtracted from the reference voltage and then multiplied with the voltage gain (*kv)* to get a virtual capacitor current reference. This virtual capacitor current is compared with the

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measured capacitor current, and the result is multiplied by the current gain (*kc)* to form the feedback voltage.

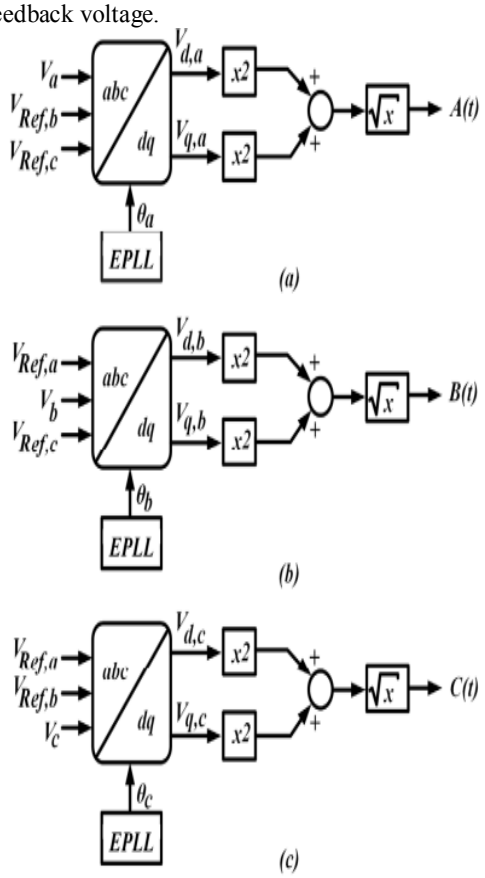

Fig.3. The improved SRF technique

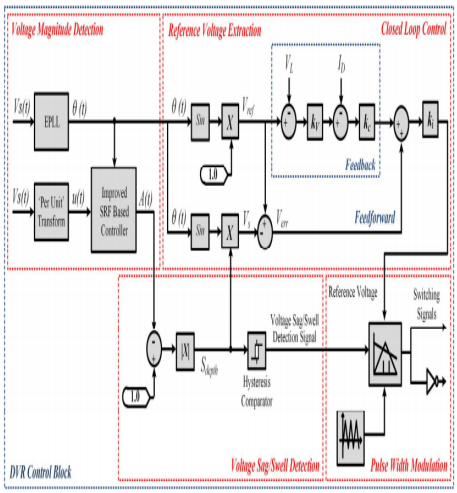

Fig.4. the structure of DVR control

C. DC-DC Converter Controller:

The isolated bi-directional controller is based on a single phase shift (SPS) method that the power transfer between DVR and SHAPF can be easily controlled by adjusting phase shift between the primary and secondary side voltages (*v1* and *v2*) of the high frequency transformer. The phase shift angle (ļ) between the square voltages *v1* and *v2* are determined by using PI controller.

IV INTRODUCTION TO FUZZY LOGIC CONTROLLER

L. A. Zadeh presented the first paper on fuzzy set theory in 1965. Since then, a new language was developed to describe the fuzzy properties of reality, which are very difficult and sometime even impossible to be described using conventional methods. Fuzzy set theory has been widely used in the control area with some application to dc-to-dc converter system. A simple fuzzy logic control is built up by a group of rules based on the human knowledge of system behaviour. Matlab/Simulink simulation model is built to study the dynamic behaviour of dc-to-dc converter and performance of proposed controllers. Furthermore, design of fuzzy logic controller can provide desirable both small signal and large signal dynamic performance at same time, which is not possible with linear control technique. Thus, fuzzy logic controller has been potential ability to improve the robustness of dc-to-dc converters. The basic scheme of a fuzzy logic controller is shown in Fig 5 and consists of four principal components such as: a fuzzification interface, which converts input data into suitable linguistic values; a knowledge base, which consists of a data base with the necessary linguistic definitions and the control rule set; a decision-making logic which, simulating a human decision process, infer the fuzzy control action from the knowledge of the control rules and linguistic variable definitions; a de-fuzzification interface which yields non fuzzy control action from an inferred fuzzy control action [10].

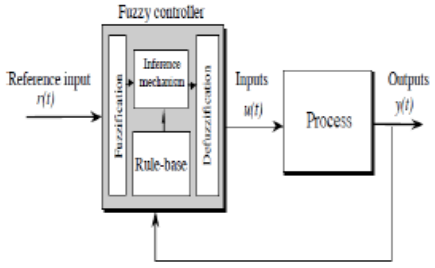

Fig.5. General Structure of the fuzzy logic controller on closed-loop system

The fuzzy control systems are based on expert knowledge that converts the human linguistic concepts into an automatic control strategy without any complicated mathematical model [10]. Simulation is performed in buck converter to verify the proposed fuzzy logic controllers.

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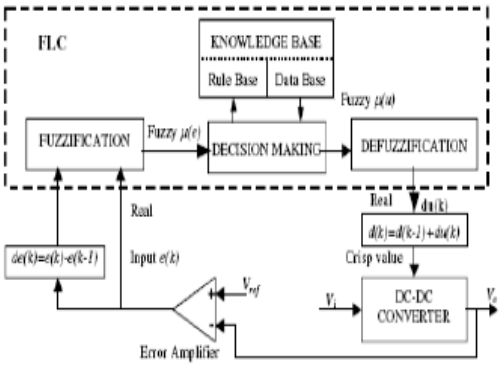

Fig.6. Block diagram of the Fuzzy Logic Controller (FLC) for dc-dc converters

A. Fuzzy Logic Membership Functions:

The dc-dc converter is a nonlinear function of the duty cycle because of the small signal model and its control method was applied to the control of boost converters. Fuzzy controllers do not require an exact mathematical model. Instead, they are designed based on general knowledge of the plant. Fuzzy controllers are designed to adapt to varying operating points. Fuzzy Logic Controller is designed to control the output of boost dc-dc converter using Mamdani style fuzzy inference system. Two input variables, error (e) and change of error (de) are used in this fuzzy logic system. The single output variable (u) is duty cycle of PWM output.

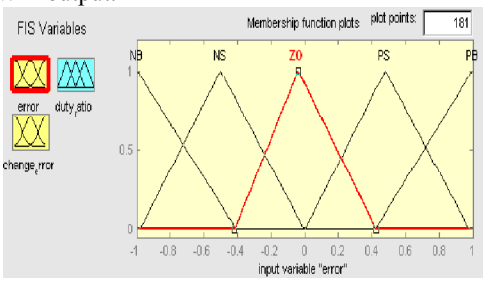

Fig. 7.The Membership Function plots of error

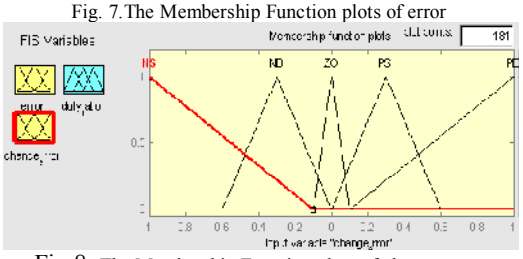

Fig.8. The Membership Function plots of change error

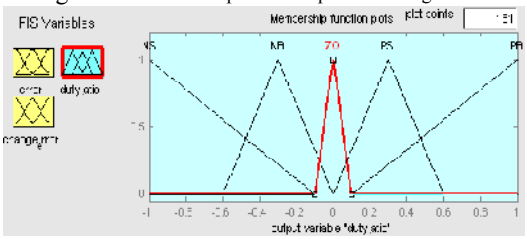

Fig.9. the Membership Function plots of duty ratio

B. Fuzzy Logic Rules:

The objective of this dissertation is to control the output voltage of the boost converter. The error and change of error of the output voltage will be the inputs of fuzzy logic controller. These 2 inputs are divided into five groups; NB: Negative Big, NS: Negative Small, ZO: Zero Area, PS: Positive small and PB: Positive Big and its parameter [10]. These fuzzy control rules for error and change of error can be referred in the table that is shown in Table II as per below:

Table II
Table rules for error and change of error

(de) \ (e)	NB	NS	ZO	PS	PB
NB	NB	NB	NB	NS	ZO
NS	NB	NB	NS	ZO	PS
ZO	NB	NS	ZO	PS	PB
PS	NS	ZO	PS	PB	PB
PB	ZO	PS	PB	PB	PB

V MATLAB/SIMULATION RESULTS:

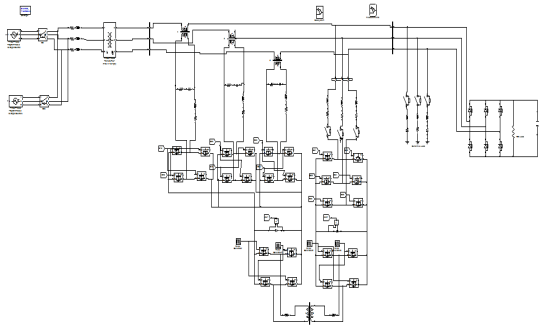

Fig 10 Simulation model for HUPQC system

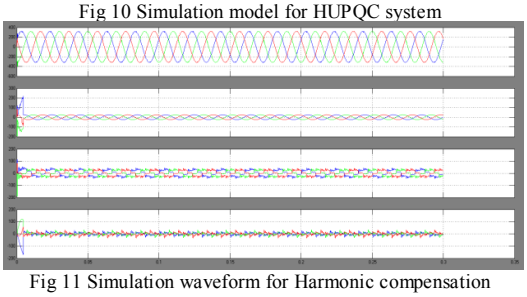

Fig 11 Simulation waveform for Harmonic compensation performance of the SHAPF

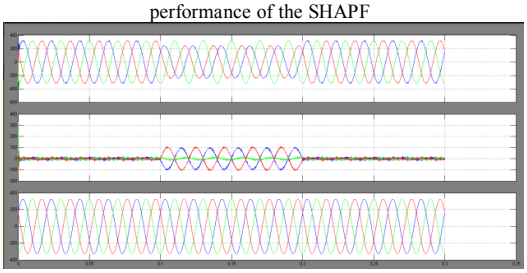

Fig 12Simulation waveform for load voltages of DVR sag/swell compensation

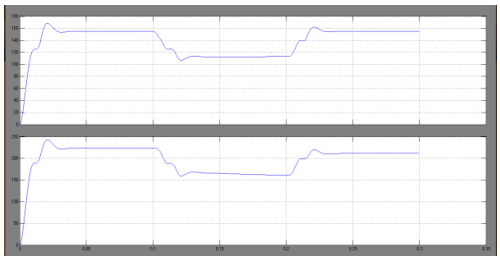

Fig 13 Simulation waveform for dc link voltages

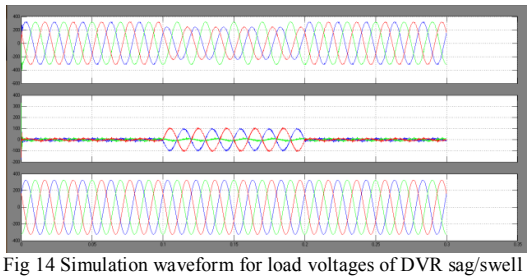

Fig 14 Simulation waveform for load voltages of DVR sag/swell compensation with fuzzy logic controller

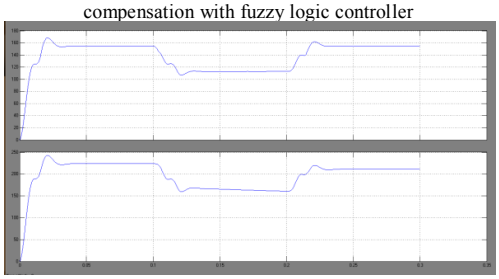

Fig 15 Simulation waveform for dc link voltages with fuzzy logic controller

VI CONCLUSION

In this paper, a new HUPQC topology is as an alternative solution to electrical power quality problems in distribution systems. In HUPQC, dc link connection of shunt hybrid APF and DVR are realized by isolated bidirectional DC-DC converter. The preferred DVR topology in the proposed HUPQC enables the compensation of unbalanced voltage sag and swells for the first time in literature within hybrid UPQC concept. The preferred shunt hybrid APF topology enables the reduction in the voltage rating of DC link capacitor and helps to reduce the cost and size of DC link and APF inverter. The dynamic response and performance of the DVR is improved with the DC-DC converter by keeping the DVR side DC link voltage stable during voltage sags and swells. DC-DC converter also provides isolation between DVR and hybrid APF inverters.

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