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A Novel Discrete cosine transforms & Distributed arithmetic

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Abstract

In this paper, first a comparative simulation study of PSNR is done for two quantization tables, one recommended byJPEG committee and another suitable for hardware Simplification. Simulation results indicate that quantization table suitable for hardware simplification can be used fordesigning JPEG baseline coder circuitry. Then we present asimple finite state machine (FSM) based VLSI architecture andits FPGA implementation from discrete cosine transform (DCT)to zig-zag ordering of transformed coefficients for JPEGbaseline coder. 1-D DCT implementation is done for thecompressed distributed arithmetic (DA) algorithm reported in previous literature with shifting performed by division operator. Quantizer using only shifter (no adder) and 2-D DCT a recombined in single step. Implementation is done on XC2VP30device on Xilinx Virtex-II Pro FPGA board.

Keywords: Discrete cosine transform (DCT), Distributed arithmetic (DA).

1. Introduction

A discrete cosine transform (DCT) expresses a sequence of finitely many data points in terms of a sum of cosine functions oscillating at different frequencies. DCTs are important to numerous applications in science and engineering, from lossy compression of audio and images (where small highfrequency components can be discarded), to spectral methods for the numerical solution of partial differential equations. The use of cosine rather than sine functions is critical in applications such as compression. The cosine functions are much more efficient where as for differential equations the cosines express a particular choice of boundary conditions. As like Fourier-related transform, DFT, discrete cosine transforms (DCTs) express a function or a signal in terms of a sum of sinusoids with different frequencies and amplitudes. And which operates on a function at a finite number of discrete data points. However, this visible difference is merely a consequence of a deeper distinction. A DCT implies different boundary conditions than the DFT or other related transforms. Frequency analysis of discrete time signals is most convenient in DCT. Discrete cosine transform is

the most popular transform technique for image compression and is adopted on various standardized coding schemes. Some applications require real-time manipulation of digital images. Because this, fast algorithms and specific circuits for DCT have been developed. Among the methods for two-dimensional DCT, the indirect method based on row-column decomposition is the best method for hardware implementation. The energy compaction property of the DCT is well suited for image compression since, as in most images, the energy is concentrated in the low to middle frequencies, and the human eye is more sensitive to the middle frequencies. A large majority of useful image contents change relatively slowly across images, i.e., it is unusual for intensity values to alter up and down several times in a small area, for example, within an 8 x 8 image block. Translate this into the spatial frequency domain; it says that, generally, lower spatial frequency components contain more information thanthe high frequency components which often correspond to less useful details and noises. The Discrete Cosine Transform transforms data into a format that can be easily compressed. The characteristics of the DCT make it ideally suited for image compression algorithms. These algorithms let you minimize the amount of data needed to recreate a digitized image. Reducing digitized images into the least amount of data possible has some advantages such as less memory required to store images, less time may be needed to analyze images, Channel bandwidth efficiency increased when transmitting images. Performing the DCT on a digitized image creates a data array that can be compressed by data compaction algorithms. Then, data can be stored or transmitted in its compacted form. The image quality depends on the amount of quantization used in the compaction algorithm. To reproduce the original image, the data is retrieved from memory, uncompacted, and an inverse DCT is performed. Some of today's most popular image data compression applications include, Teleconferencing using motion-compensated video codec's, ISDN multimedia communications including voice, video, text, and images, Video channel transmission using commercial geosynchronous tele communications satellites, Digital facsimile transmission using dedicated equipment and personal computers. Several image data compression algorithms use the DCT to remove spatial data redundancies in two-dimensional (2D) data. Images are subdivided into smaller, two-dimensional blocks. These blocks are then processed independently of the neighboring blocks. In general, the two dimensional, discrete cosine transform (2D DCT) transforms an (n x

n) data array into an (n x n) result array. First the DCT transforms the columns, and then it transforms the rows.

2. Related Work

2.1 DESIGN OF DA-BASED DCT STRUCTUREL:

Discrete cosine transform (DCT) is unitary of the major compression schemes owing to its near optimal performance and delivers energy compaction efficiency greater than any other transform. The transformation algorithm is presented in [6].

2.1.1 DCT ARCHITECTURE:

By using DCT architecture, then DWT is that there is higher throughput, lesser complexity and also no need to manipulate complex number. When computing 2D DCT, a greater number of multipliers and adders are required for enforcing the compression organization in harder, which shows the most timeconsuming process, it can be completely avoided in the proposed DA-based DCT architecture with Kogge_Stone_Adder. A minimum number of additions are used to the DCT based on the Distributed Arithmetic.

2.2 DA-BASED DCT

Distributed Arithmetic (DA) is an efficient method for computing inner products. It uses look up tables and replaced the accumulators instead of multipliers for computing inner products in DCT. DA-based DCT architecture is considerably known for VLSI implementation due to its reducing ROM size, by this area reduced [8]. DA-based DCT uses even-odd frequency decomposition of the DCT along with memory reduction. The 1D 8-point DCT are constructed using a DA-Butterfly-Matrix that has even and odd processing elements and Parallel Prefix Adder (Kogge_Stone_Adder) are show in Fig.1.

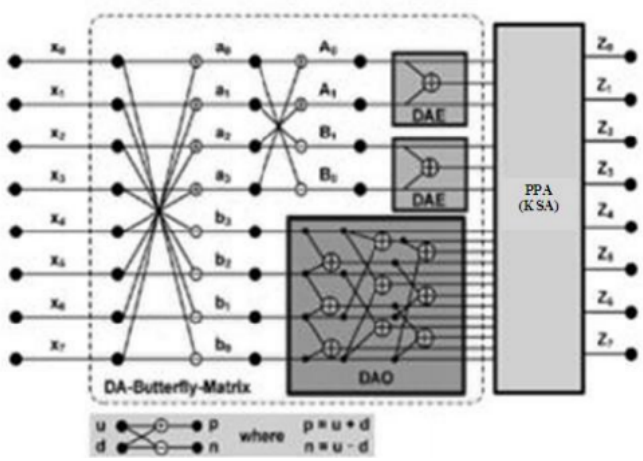

Fig.1. Architecture of 1D 8-point DA-DCT.

The 1D-DCT employs the DA-based architecture [6] and proposed Kogge_Stone_Adder to achieve a high-speed, small area and low power design. The 1D 8-point DCT can be expressed as follows in Eq. (1).

$$z_n = \frac{1}{2} k_n \sum_{m=0}^{7} x_m \times \cos\left(\frac{(2m+1)np}{16}\right) \qquad (1)$$

where, x_m denotes the input data;
z_n denotes the transform output;

$$k_n = \frac{1}{\sqrt{2}} \text{ for } n = 0;$$

$0 \le n \le 7$; $k_n = 1$ for other n values.

By neglecting the scaling factor ½, the 1D 8-point DCT in Eq. (1) can be divided into odd and even parts as presented in [7].

The DA-based DCT operation performs even, odd decomposition of input pixels and the representation of cosine basis in Canonical Sign Digit (CSD) [7]. Image compression operations are taking place as, the input image is broken into 8 × 8 block and they are multiplied by DCT matrix. After multiplication, addition process has taken place. For instance, take the input pixel value 120 is multiplied with the DCT fraction value 0.707 answers as 84.84, where the complexity is more and also delay increases due to the carry part. To overcome this complexity and delay state in this paper at DAbased DCT structure Canonical Sign Digit are used [6] by neglecting the unwanted LSB's this is accomplished by reproducing the input pixels with larger number as 210 are shown below.

$$2^{10} \times 0.707 = 723.968$$

By this proposed method the decimal values are completely carried away and complexity reduces largely by left shifting as described the cosine basis in [6].

3. Implementation

Distributed arithmetic is a bit level rearrangement of a multiply accumulate to hide the multiplications. It is a powerful technique for reducing the size of a parallel hardware multiply accumulates that is well suited to FPGA designs. It can also be extended to other sum functions such as complex multiplies, Fourier transforms. Distributed arithmetic (DA) is an effective method for computing inner products. It uses Look up Tables (LUT) and accumulators instead of multipliers.

Distributed arithmetic (DA) provides application in Very Large Scale Integration (VLSI) implementations of Digital Signal Processing (DSP) algorithms. Most of these applications, for example Discrete Cosine Transform (DCT) calculation, are arithmetic intensive with multiply/accumulate (MAC) being the predominant operation. The advantage of DA approach is that it alerts the basic assumption of using multipliers and adders for computing the DCT.

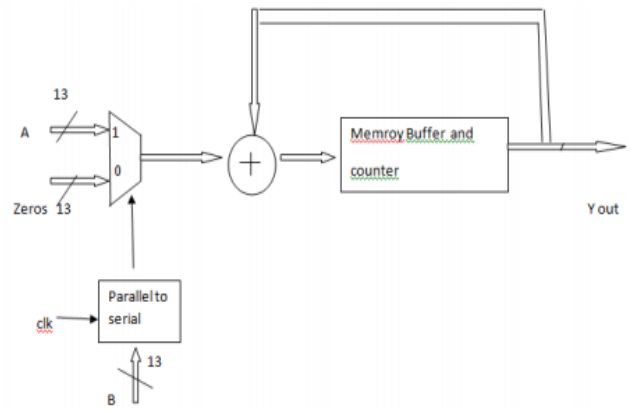

Figure 2. Distributed Arithmetic.

DCT is a computational intensive operation. It requires large number of adders and multipliers for direct implementation .Multipliers consume

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more power and hence distributed arithmetic (DA) is used to implement multiplication without multiplier.

The architecture of 1D-DCT

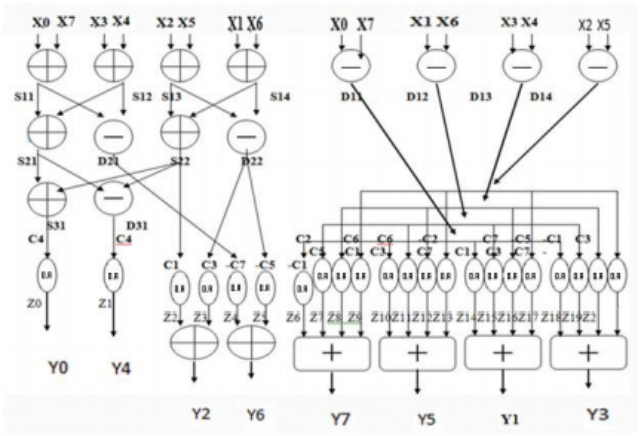

Figure 3. Overall architecture for DA base DCT.

4. Experimental Work

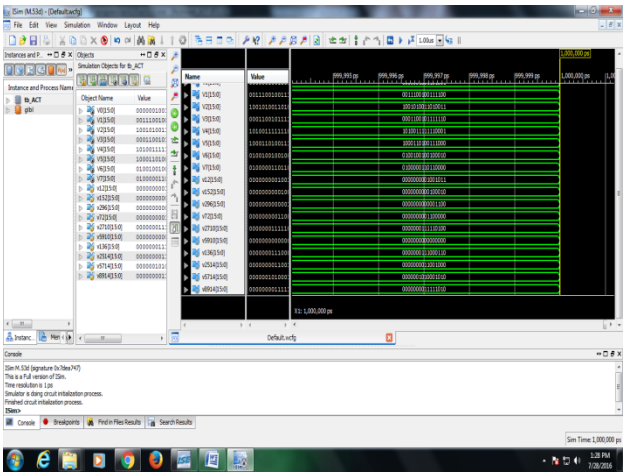

Figure (4): simulation results

Synthesis Results:

RTL schematic:

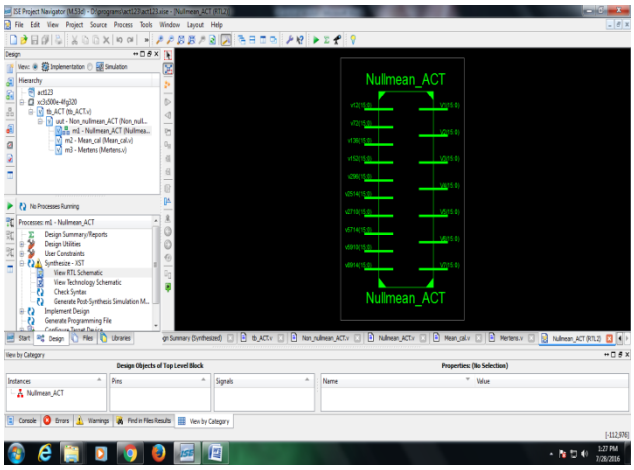

Figure (5): Null-mean Act schematic

Design Summary:

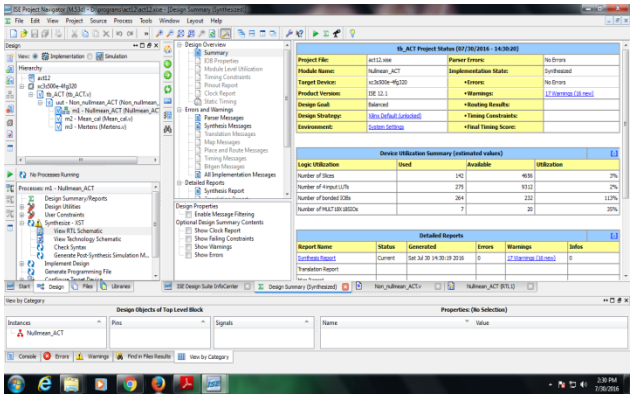

Figure (6): Design summary

5. Conclusion

In this paper, we have proposed an efficient VLSI architecture for the 2D-DWT to meet the requirements of real-time image and video processing. The advantages of the proposed architecture are saving embedded memories, fast computing time, low power consumption, and low control complexity. This hardware is designed to be used as part of a complete high performance and low power JPEG2000 encoder system for digital cinema applications. The proposed architecture has been correctly

verified by the VHDL Language. It routed in Altera Stratix III to work at 350 MHz and Cyclone II FPGA at 290 MHz's The FPGA implementation can code 48 frames (4096 x 2160) per second with 24 bpp. Moreover, it can be applied very well to the implementation of the coder used in real time video processing, such as MPEG-4.

6. References

[1] Vijay Kumar Sharma, K. K. Mahapatra and Umesh C. Pati,"An efficient distributed arithmetic based VLSI architecture for DCT" IEEE transaction on devices and communications 2011.

[2] T. Acharya and P. Tsai, "JPEG2000 Standard for ImageCompression: Concepts, Algorithms and VLSI Architectures" J. Wiley & sons. NJ, 2005.

[3] Gregory K. Wallace, "The JPEG Still Picture Compression Standard,"IEEE Transactions on Consumer Electronics, vol.38(I), Feb. 1992.

[4] R. C. Gonzalez, R. E. Woods, "Digital Image Processing,"2nd.Ed.,Prentice Hall, 2002.

[5] F.H.P. Fitzek, M. Reisslein, "MPEG-4 and H.263 Video Traces for Network Performance Evaluation,"IEEE Network, vol.15, no.6, pp.40-54, Nov/Dec 2001.

[6] Luciano Volcan Agostini, Ivan Saraiva Silva and Sergio Bampi,"Multiplierless and fully pipelined JPEG compression soft IP targeting FPGAs," Microprocessors and Microsystems, vol. 31(8), 3 pp.487-497,Dec. 2007.

[7] S. A. White, "Applications of distributed arithmetic to digital signal processing: a tutorial review," IEEE ASSP Magazine, vol.6, no.3, pp.4-19, Jul.1989.

[8] M.-T. Sun, T.-C. Chen, A.M. Gottlieb, VLSI Implementation of a 16x16 Discrete Cosine Transform," IEEE Transactions on Circuits and Systems, vol.36, no. 4, pp. 610 – 617, Apr.1989.

[9] A. Shams, A. Chidanandan, W. Pan, and M. Bayoumi, "NEDA: A low power high throughput DCT architecture," IEEE Transactions on Signal Processing, vol.54(3), Mar. 2006.

[10] Peng Chungan, Cao Xixin, Yu Dunshan, Zhang Xing, "A 250MHz optimized distributed architecture of 2D 8x8 DCT," 7th International Conference on ASIC, pp. 189 – 192, Oct. 2007.

[11] M. Kovac, N. Ranganathan, "JAGUAR: A Fully Pipelined VLSI Architecture for JPEG Image Compression Standard," Proceedings of the IEEE, vol.83, no.2, pp. 247- 258,Feb.1995.

[12] Yuan-Ho Chen, Tsin-Yuan Chang, Chung-Yi Li, "High Throughput DA Based DCT With High Accuracy Error-Compensated Adder Tree," IEEE Transactions on Very Large Scale Integration (VLSI) Systems, vol. PP, issue 99, pp. 1-5, Jan 2010.

[13] A. Kassem, M. Hamad, E. Haidamous, "Image Compression on FPGA using DCT,"

International Conference on Advances in Computational Tools for Engineering Applications, 2009, ACTEA '09, pp.320-323, 15-17 July 2009.

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