

A Novel OFDM using Radix 22 and FFT Algorithm

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Abstract

Several new generation wideband data communication systems nowadays, have adopted Orthogonal Frequency division Multiplexing technique. FFT/IFFT is one of the main kernel in the OFDM system, therefore, special attention needs to be given to optimize the FFT block. Hence, utilizing low power, area efficient as well as high speed multipliers and adders in Fast Fourier Transform will ensure enhanced performance and efficiency. Urdhva Tiryakbhyam is one of the age-old Indian Vedic sutra dealing with multiplication which enables parallel generation of partial products and completely eliminates unwanted multiplication steps. Multipliers implemented using Vedic mathematics is superior in terms of area efficiency. Carry Select Adders (CSLA) are one of the fastest adders used in several processors to perform fast and complex arithmetic functions. In this work, the Vedic multiplier which is developed using the Urdhva Tiryakbayam Sutra along with modified carry select adder is used to perform a Radix-22 pipeline Fast Fourier Transform. The Fast Fourier Transform (FFT) which is implemented using Vedic multiplier and modified adder is then compared with FFT implemented using traditional multipliers and adders and its performance is verified. Such an FFT will be most suitable to OFDM communication system. The coding of the FFT processor developed based on Vedic mathematics is done in VHDL (very high speed integrated circuit hardware description language) and synthesis is done using Xilinx ISE series.

Keywords:Radix 22 FFT, Algorithm, OFDM, Urdhava Tiryakbhyam, CSLA

1. Introduction

OFDM transmissions are emerging as a predominant multi-carrier modulation technique because of its capability of ensuring

high level robustness against interference. OFDM modulation technique is now extensively used in numerous high speed mobile and wireless communication systems as; fixed Wi-Fi system ,fixed WiMAX system (IEEE

802.16a standard), Asymmetric digital subscriber line (ADSL), mobile WiMAX system (IEEE 802.16e standard) and Wireless Local Area Network (WLAN). It provides high bandwidth efficiency because the carriers are orthogonal to each other and multiple carriers share the data among themselves. Fast Fourier Transform (FFT) is one of the key components in an OFDM system. Nowadays, several communication systems require higher points FFT and higher symbol rates. This requirement establishes challenges for low power and high speed FFT designs with large number of points. The FFT algorithm eliminates the redundant calculation which is needed in computing Discrete Fourier Transform (DFT) and is thus very suitable for efficient hardware implementation [13]. In addition to computing efficient DFT, the FFT is the core processing block in several widely used applications such as linear filtering, digital spectral analysis, image processing and correlation analysis. One of the major concerns for researchers is to meet this real-time processing requirement and to reduce the hardware complexity mainly with respect to area and power and to improve processing speed over the last decades. Hence, designing a pipeline FFT processor would provide optimum solution for speed, but it occupies more area for different stages used in the pipeline and also increases the

implementation complexity. Thus, utilizing a novel structure suitable for FPGA implementation along with reduced complexity of the FFT processor is necessary to ensure enhanced computational efficiency and improved performance. An efficient hardware oriented radix-2² algorithm is developed by integrating a twiddle factor decomposition technique. This is done by divide and conquers approach to form a spatially regular Signal Flow Graph (SFG). Mapping the proposed algorithm to the cascading delay feedback structure leads to the proposed architecture [11]. Vedic Mathematics is the ancient system of mathematics which has unique techniques of calculations based on 16 Sutras. All the Vedic formulae are claimed to be based on the natural principles on which the human mind works. The paper utilizes “Urdhva Tiryakbhyam” algorithm of ancient Indian Vedic Mathematics which is utilized for multiplication in complex twiddle multipliers. The next sections describes about the literature reviewed. The algorithms & also the design methodology towards developing an efficient FFT Core utilizing vedic mathematics which is aimed at increasing the performance of the OFDM system. Finally, we conclude with a comparison of the hardware requirement of our proposed FFT with conventional FFT.

2. Related Work

Satyendra Sharma and Unnati.C.Mehta in 2011 [17] presented a straightforward approach for pipeline implementation of radix-2 FFT algorithm called as Radix-2 single-path Delay Commentator (R2SDF) along with FIFO design for Mobile Wi-MAX. It was observed that at different stages of the design, the requirement of FIFO was different. The length of the FIFO depended on which stage of pipeline it was used. Width of the FIFO depends upon the word length used; this led to increased width for higher word length. The input sequence was broken into two parallel data stream flowing forward, with correct "distance" between data elements entering the butterfly scheduled by proper delays. This architecture required $\log_2 N$ radix-2 butterflies, as well as $\log_2 N - 2$ multipliers which were considered as the disadvantage of this architecture.

Bin Zhou, David Hwang and Yingning Peng in 2007[4] noticed most of the works related to Radix-4 Single-path Delay Commutator (R4SDC) and proposed an area-efficient algorithm. The R4SDC which was a Radix-4 version of Radix-2 Single-path Delay Feedback, employed CORDIC iterations for the pipelined processing of fast Fourier transform. A single data stream goes through the multiplier at every stage. The utilization of multipliers was increased to 75% due to the storage of three out of radix-4 butterfly outputs. The utilization of

the radix-4 butterfly was fairly complicated and contained at least 8 complex adders; hence it resulted in a very complex implementation of the processing elements (PEs). This design involved complex controller design which created a long critical path. It required $\log_4 N - 1$ multipliers, $\log_4 N$ full radix-4 butterflies and storage of size $N - 1$. Such architecture provided a lesser throughput per area.

Marti-Puig, Reig Bolano in 2009[14] derived two families of radix-4 factorizations for the FFT that have the property that both inputs and outputs are addressed in natural order. These families were obtained from another two families of radix-2 algorithms that have the same property. The algorithms obtained had the same number of multiplications and additions (mathematical complexity) as that of Radix-4 Cooley-Tukey algorithms but eliminated the input or output bit-reversal ordering applied in Cooley-Tukey algorithm. The hardware realization of Radix 4-FFT was done by multi-bank memory along with "in place" addressing strategy which reduces the memory access time and minimizes the hardware consumption. The main drawback was that, it suffered from low utilization of all components, which could be compensated only in certain special applications.

Angel M. Burón, Gustavo Ruiz, Jesús García and Juan A. Michell in 2007[3] explained the

realization of a Split Radix FFT (SRFFT) processor based on a pipeline architecture for signal and image processing application. This architecture focused on combining the higher parallelism of the Radix-4 FFTs and the possibility of processing sequences having length of any power of two. This architecture has as its basic building blocks a Complex Butterfly and a Delay Commutator. But the delay commutator had to be designed to be customized for even and odd SRFFT computation levels. The main drawback was the irregular structure compared to mixed radix and constant radix algorithms. Because of the irregular structure, this algorithm was not suitable for parameterization. It was most used with segmented arithmetic of any level of pipeline in order to speed up the operating frequency.

3. Implementation

In the proposed FFT architecture, Radix-2 2 DIF FFT algorithm derived in the previous section is mapped to the radix-2 Single delay feedback(SDF) architecture, and a new Radix 2 SDF architecture approach is obtained. Fig 2 outlines an implementation of the proposed

architecture for $N=64$, the similarity of the data-path to R2SDF and the reduced number of multipliers within the architecture can be noted. The implementation uses two kinds of butterflies; one identical to that in Radix2 SDF architecture, while the other also contains the logic to implement trivial twiddle factor multiplication, as shown below in Fig 3 and Fig 4 respectively. The proposed 64-point Radix- 2 fixed-point FFT consists of six Radix-2 butterflies designed using modified adders, feedback registers along with each butterfly, two complex vedic multipliers, two twiddle factor rom, and a controller module that provides the control signals to each of the butterflies. The feedback registers vary in length from 1 to 32-bits and are indicated below accordingly in the fig2. The twiddle values are generated by a Matlab program and the twiddle values are converted to fixed point and stored in the rom. Due to the spatial regularity of Radix-2 2 algorithm, the controller module of the processor is very simple. It serves two purposes: address counter for twiddle factor reading in each stage and also as a synchronization controller.

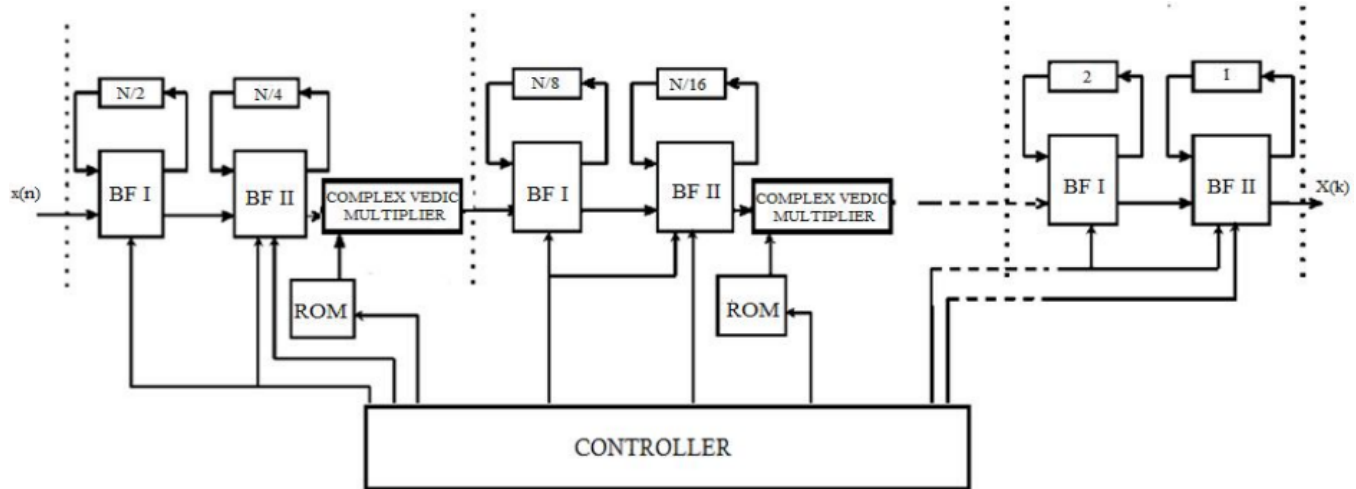


Fig2 Block Diagram of proposed N point Radix22 Vedic FFT Processor.

A. Butterfly Structures:

The scheduled operation of the pipelined Radix 22 Single- path delay feedback FFT processor in Fig 3 can be explained with the help of the butterfly structures shown below is as follows. Fig. 3 shows the Butterfly I structure(BF I), the inputs X_r , X_i of this butterfly comes from the FFT input data and in the succeeding stages this input comes from the previous component which is the twiddle factor multiplier. The output data Q_r , Q_i goes to the next stage which is normally the Butterfly II. The control signal (CNT1) has two options: when CNT1=0, the multiplexers direct the input data to the feedback registers until they are filled in the initial $N/2$ cycles. The other option is CNT1=1, in the next $N/2$ cycles, the multiplexers select the output of the adders and subtractors which is implemented by 2's complement modified adder in the proposed

design. This is the butterfly output i.e. a 2-point DFT computation with the incoming data and the data stored in the feedback registers.

$$\begin{aligned} Q(n) &= x(n) + x\left(n + \frac{N}{2}\right) \\ Q1\left(n + \frac{N}{2}\right) &= x(n) - x\left(n + \frac{N}{2}\right) \end{aligned} \quad (5)$$

The butterfly outputs $Q(n)$ and $Q1(n + N/2)$ are computed according to the equations given in eqn (5). $Q(n)$ is sent to the next stage and $Q1(n + N/2)$ is sent back to the feedback registers to be “multiplied” in the next $N/2$ cycles when the first half of the next frame of time sequence is loaded in. Operation of the second butterfly (BF II) is similar to that of the first one (BF I), except the “distance” of butterfly input sequence are just $N/4$. After $N-1$ clock cycles, the result of the complete DFT transform streams out to the last BFII structure. The next frame of

transform can be computed continuously without pausing due to the pipelined processing of each stage. The input data Q_r, Q_i comes from the previous component, Butterfly I. The output data from the Butterfly II are Y_r, Y_i , as well as the real and imaginary feedback signals. Feedback signals are fed to the next component, which is the twiddle factor multiplier. The multiplication by $-j$ involves swapping between real part and imaginary part and sign inversion.

Swap-MUX efficiently handles the swapping and the sign inversion is handled by switching between the adding and the subtracting operations performed by the adder/subtractor module. The control logic is activated when there is a need for multiplication by $-j$, therefore the real and imaginary data will swap and the adding and subtracting operations will be switched. Rounding off has been also applied to reduce the scaling error.

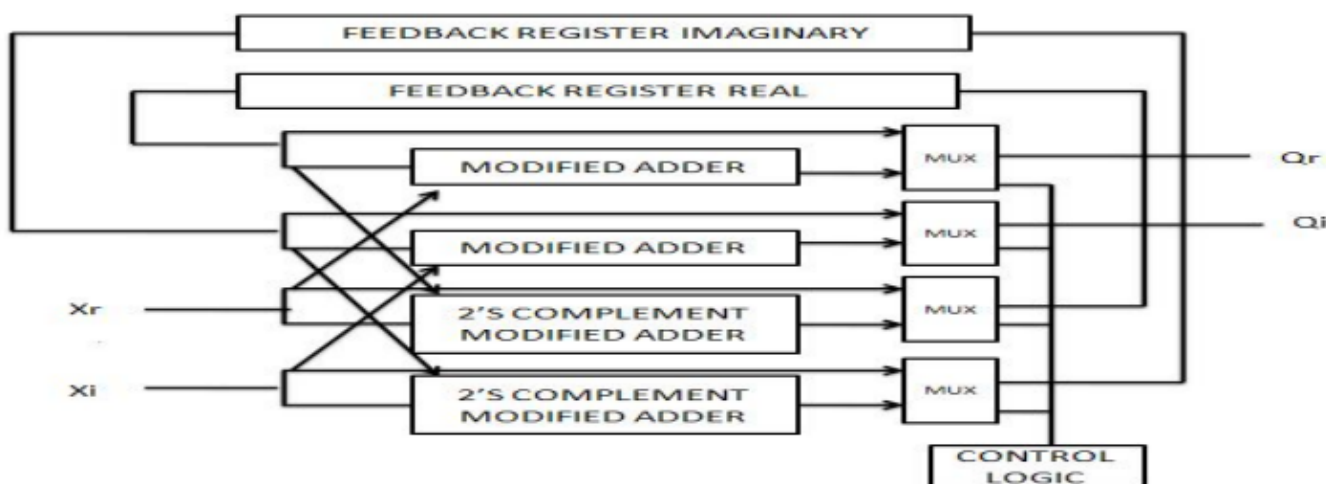


Fig 3 Butterfly structure (BFI) for Radix 22 FFT Processor.

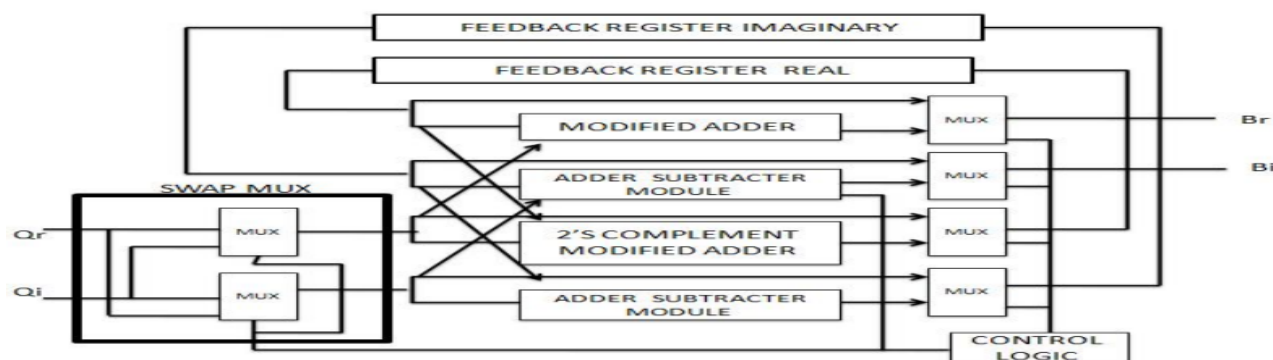


Fig.4 Butterfly structure (BFII) for Radix 22 FFT Processor.

4. Experimental Work

An efficient 64 point Radix-2 2 FFT module was designed using Vedic multipliers and modified adder and simulated using VHDL.FFT utilizing modified wallace multiplier and regular carry select adder was also simulated to compare the performances in terms of area and speed. Both the designs were implemented using the Sparten 3E and their synthesis reports were analyzed. Fig 5 shows the simulation of

the test bench which was developed to test and verify the 64 point FFT. The values were verified with Matlab output. Fig 6&7 show the simulation of the complex vedic multiplier and the modified adders utilized in the proposed processor. The 32 bit inputs are entered in both cases and the product and sum is verified respectively. The conclusion proves that our proposed system is better in terms of area and speed compared to the existing FFT processors.

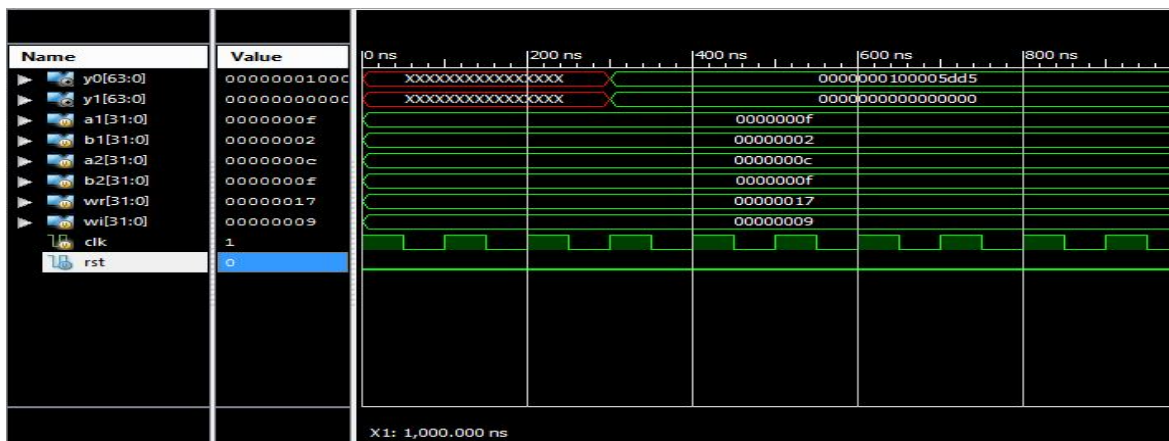


FIGURE.5: simulation result of 128 point FFT



FIGURE.6:Simulation result of 256 point FFT

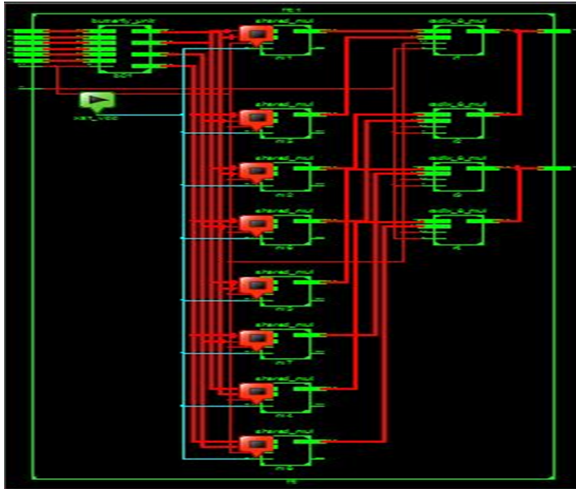


FIGURE 7: RTL schematic diagram of 128 point FFT.

5. Conclusion

In this paper, Vedic FFT processor with Radix 2 FFT algorithm is designed and implemented using Spartan 3E FPGA and is attractive to be used in real-time systems. Implementation results prove that the proposed FFT led to 26% area reduction and 29% speed improvement when compared with conventional FFT. This design had a maximum clock frequency of 95.2MHz. Such a 64-point FFT implemented using vedic concepts and modified adder was found to have a good balance between performance and hardware requirements and is therefore most suitable for use in OFDM. The results are a clear indication that the processing time of the proposed FFT is below the OFDM symbol period of 4 μ sec, which ensures an appropriate operation for the communication standard application requirements of mobile

WLAN(IEEE 802.11a), which uses OFDM modulated wireless communication system.

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