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VDigital signal processing Using filter truncated multipliers By VLSI design

Jaya Raju .Dara [1] & K Kameswar Reddy [2]

[1]M-Tech Dept of ECE, Geethanjali Engineering College NANNUR-V, KURNOOL-DIST

[2] Assistant Professor Dept ECE, Geethanjali Engineering College NANNUR-V, KURNOOL DIST Mail Id:- kamesh18@gmail.com

Abstract:- Low-cost finite impulse replication (FIR) designs are presented utilizing the concept of multipliers with the optimization of bit width and hardware resources without sacrificing the frequency replication and output signal precision. Non-uniform coefficient quantization with opportune filter order is proposed to minimize total area and cost. Multiple constant multiplication/accumulation in a direct FIR structure is implemented utilizing an amended version of Booth multipliers. In this proposed method a booth multiplier is implemented. In Booth multiplier to multiply the signed numbers is an integrated advantage. Comparisons with antecedent FIR design approaches show that the proposed designs achieve the best area and power results.

KEYWORDS: VDigital signal processing (DSP), faithful rounding, finite impulse response (FIR) filter, truncated multipliers, VLSI design

1. INTRODUCTION

Digital signal processing technology and its advancements have dramatically impacted our modern society everywhere. Without DSP, we would not have digital audio and verbalization, Digital telephone, Automobile industry, Electronic communications, Medical imaging equipment, Multimedia applications. The signals are conventionally processed in digital representation. , so verbalization processing can be regarded as a special case of digital signal processing the digital filter is the most consequential system in verbalization processing. It is utilized to reduce the noise in an information bearing signal. Predicated on the impulse replication filters are relegated as two.

Finite impulse replication filter (FIR)

Illimitable impulse replication (IIR).

FIR filter is designed utilizing finite number of impulse replication. IIR filter does not provide the stable output, So that here we have to design an efficient transposed FIR filter which engenders stable output.

The involution of the fir filter is dominated by the multiplication of the input samples with filter coefficients. Filters employ an immensely colossal number of multipliers that lead to exorbitant area and power consumption. But the filter coefficients are constant for a given filter, so that multiplications are implemented by a network of adders and sub tractors. Where the number of adders and subtractions are minimized by a constant multiplication scheme. In the transposed fir filter, the recent most input sample at any given clock period is multiplied with all the filter coefficients. A set of intermediate results are engendered in this case, and shared across all the multiplications in order to minimize the total number of integrations and subtractions utilizing multiple constant multiplication techniques. Each such intermediate results in an MCM process corresponds to one of the mundane sub-expressions of the set of constants to be multiplied. The prevalent sub expression elimination for MCM reveals that the number of operators used to compose the adder tree networks is very consequential. The number of operators on an adder tree is resolute by the number of input terms the coefficient uses from the network. For an N input adder tree, N-1 operators are required. Identify the resource minimization quandary in the scheduling of adder tree operations for the FIR MCM block. The area and power consumption of the filters MCM blocks can be calculated and apply the MIP predicated algorithm for exact bit level resource optimization.

2. RELETED WORK

The number of additaments used to implement the coefficient multiplications. It determines the intricacy of digital filters. Many approaches have been proposed in literature for reducing the number of adders in the multipliers of digital filters. Utilizing coefficient partitioning method to implement low intricacy digital filters with minimum number of full adders. While the optimization criterion in conventional low intricacy filter implementation method is the number of adders, the focus of this method is to minimize the number of full adders required for each adder. The coefficient partitioning algorithm is amalgamated with

the pseudo floating point coefficient coding scheme and applied to optimize the mundane sub expression elimination methods. The full adder reduction achieved utilizing this method is substantially higher for higher order filters. The number of adders and critical paths in a multiplier block of a multiple constant multiplication predicated implementation of a finite impulse replication filter can be minimized through mundane sub expression eliminate techniques. A two bit mundane sub expression can be located recursively in a non-canonic sign digit representation of the filter coefficients. To amend the elimination of a CS from the multiplier block of an FIR filter. It can be realized with fewer adders and logical depths as compared to the subsisting methods. This algorithm shows average logical operator with a comparative logic depth requisite. The two reconfigurable FIR filter architectures, namely Constant shift method (CSE) and Programmable sub expression elimination (PSE). Among these approaches, techniques the best hardware reduction since it deals with the multiplication of one variable (input signal) with several constants (coefficients).The CSE techniques fixate on eliminating redundant computations in multiplier blocks by employing the most mundane sub expressions consisting of two-nonzero bits. The PSM approach is predicated on the prevalent sub expression elimination algorithm utilized. Unlike the CSM method where constant shifts are utilized, the PSM employs programmable shifters. The advantage of PSM over CSM is that the former architecture always ascertains the minimum number of integrations and thus minimum power consumption. The latency of the adder tree increases by utilizing this approaches. An incipient algorithm for digit serial FIR filter utilizing CAD implement proposed in [2]. Little attention has been given to the digit-serial MCM design that offers alternative low involution MCM operations at the cost of an incremented delay. Designing digit-serial MCM operation with optimal area at the gate level by considering the implementation costs of digit-serial integration, subtraction, and shift operation. Since there are still instances with which the exact CSE algorithm cannot cope, the number of adders and logical operators still increases the latency and reduces the throughput of the multiple constant multiplication. The resource minimization quandary in the scheduling of adder tree

operations for the FIR multiple constant multiplication block and utilized the commixed integer programming predicated algorithm for exact bit level resource optimization. The puissance and area reduced in this approaches. After the quandary identification of all these implementations to surmount that only we have to implement an efficient FIR filter and proposed the high speed carry cull adder in the scheduling of adder tree MCM block for verbalization processing applications.

3. IMPLEMENTATION

Greedy Adder-Tree Scheduling

The coefficient of each CS terms is utilized for the treeheight minimization algorithm to engender an optimum height adder-tree. The minimization algorithm for tree height is utilized iteratively which collapses the dyad consisting of {Ti , Tj} with delays having most diminutive values. The most diminutive delays are calculated utilizing INTEGRATE/SUB to compose an incipient term with delay max(Di , Dj)+1 until a single term is reduced. The minimum delay value can be calculated by either a positive sign or a negative sign. When the positive sign is utilized then it determines the additament operation or when the negative sign is utilized then it determines the subtraction operation. With the avail of these designations, it can able to identify when the algorithm collapses a dyad of terms in the adder-tree. This is predicated on two rules. (1) If two input edges are of same sign then INTEGRATE is utilized otherwise it will be SUB. (2) The denotement of the output edge is always same as that of the left input edge. With the avail of these two rules the summation engendered from the final term may carry a negative sign. For an FIR filter, results from multiple adder-trees are accumulated by a structural adder-register line. So the negation can be eliminated by superseding the structural adder with a subtractor.

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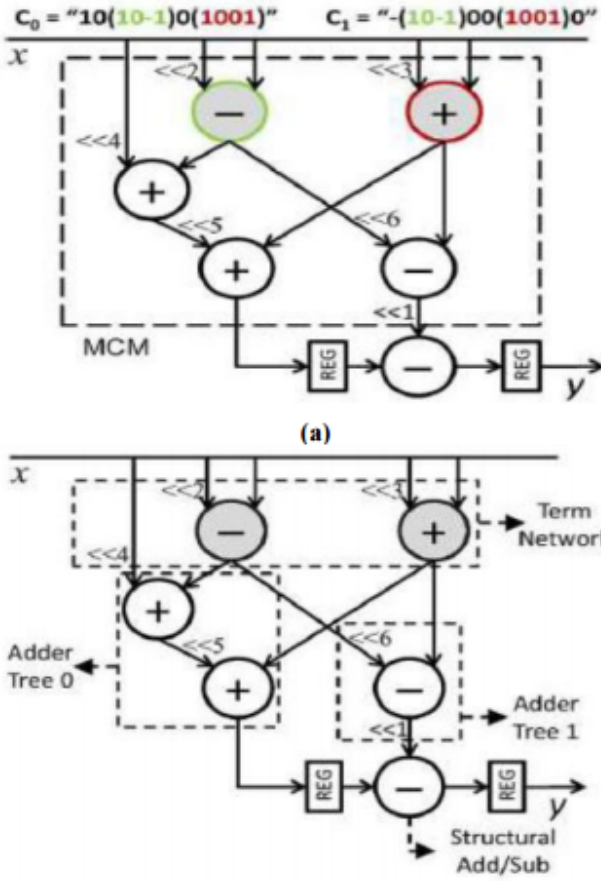

Fig.1 Composition of the MCM and Sub expression, (b) Term network and adder-trees for each Coefficient.

Cost Model

In order to reduce the hardware cost of the adder-tree the implementation of ripple carry is predicated on the cost of the INTEGRATE/SUB operations, which is most area efficient and will be picked up by the hardware compiler whenever the timing sanctions. The cost is calculated discretely by three bit segments. The cost calculation commences from the least paramount bit (LSB), 1st segment covers the bit positions not including the first bit of the shifted operand, 3rd segment covers the bits corresponding to the denotement extension bits of the denotement elongated operand and 2nd segment takes the rest of the bit positions. INTEGRATE operation is predicated on two cases are shown in . In both cases, the 2nd and 3rd segments are implemented by one Full Adder (FA) per bit, while the 1st segment cost is nothing but the wiring. SUB operation is predicated on four cases are shown in . In first two cases the shift operation takes place with the minuend. The first segment is implemented by full adders with the inverters in the minuend bits. The 1st segments for the last two cases are the wires, the 2nd segment for all the cases is implemented by a dyad of full adders and invertors and the 3rd segment when the designation extension bits emanate from the subtrahend, investors are not needed.

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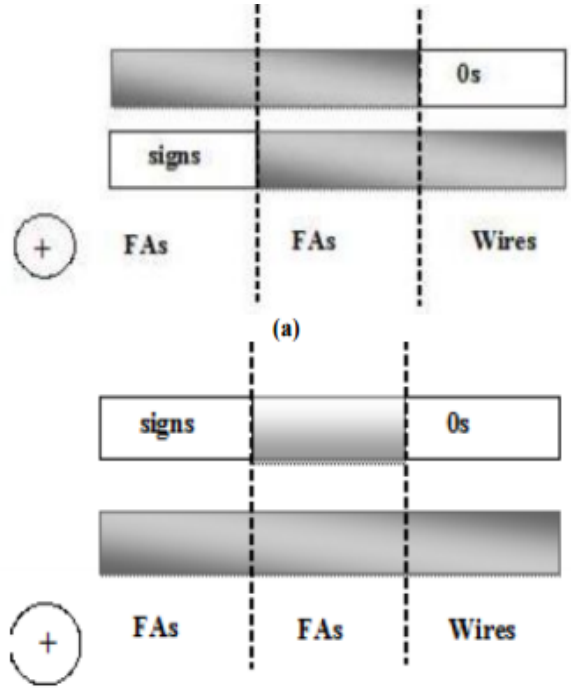

Fig.2 First case of ADD operation,

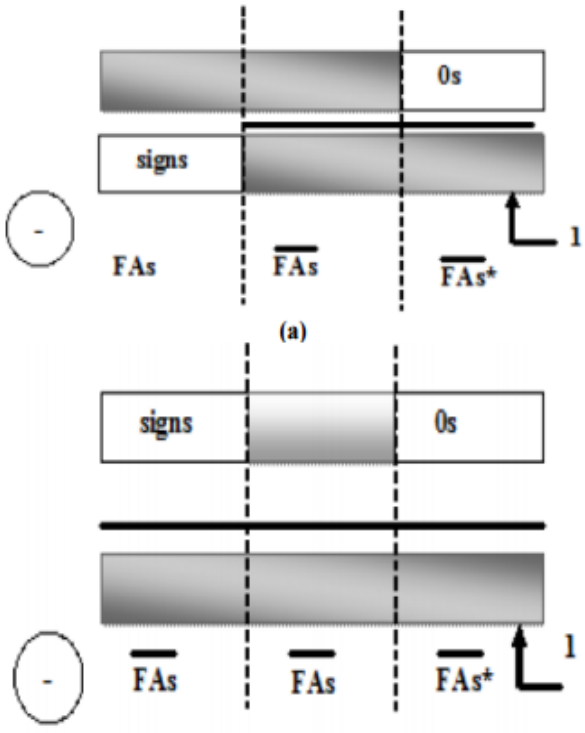

Fig:3 Second case of ADD operation

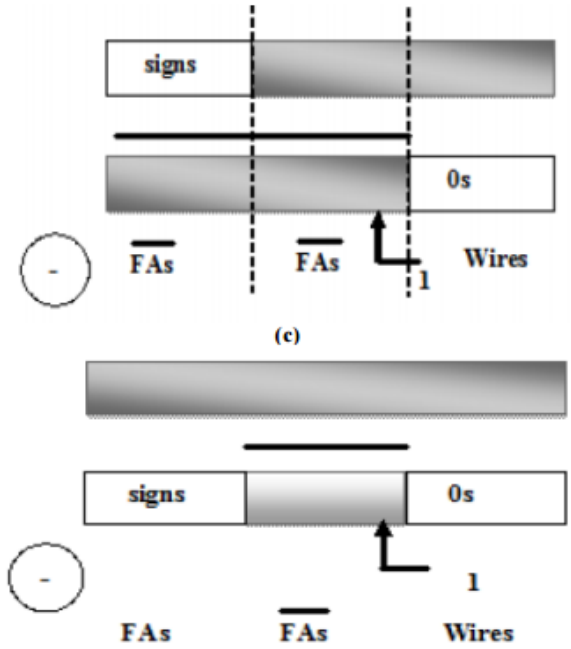

Fig. 4 First case of SUB operation

Pipelined Filter Implementation Using Mcm

To surmount the drawbacks of mundane sub expression elimination algorithm and digital recording algorithm, multiple constant multiplication is utilized which is predicated on the cupidinous scheduling algorithm. The proposed system verbalizes that to introduce the Cupidinous Scheduling algorithm is mainly utilized for the further reduction of area and delay. Pipelining with efficient MCM is introduced to increment the haste of the process which denotes that to reduce the delay. The pipelining architecture is constructed with MCM implementation. The

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Multiple Constant Multiplication is one of the hardware efficient techniques which greatly reduces the number of shifts and integrate operation. The pipelining architecture with MCM implementation with Nth order is illustrated in . In an N-level pipelined system, the number of delay elements in any path from input to output is (N-1) more preponderant than that in same path in the pristine sequential circuit. While pipelining reduces the critical path, it leads to a penalty in terms of an incrementation in latency. Latency is the difference in the availability of the first output data in the pipelined system and sequential system. For example if latency is 1 clock cycle then the kth output is available in (k+1) th clock cycle in a 1- stage pipelined system. The two main drawbacks of the pipelining are increase in the number of latches and in system latency

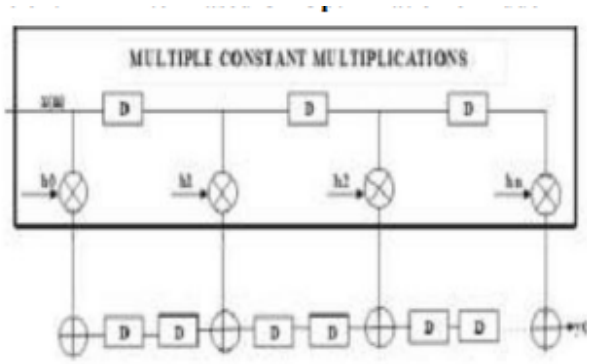

Fig:- 5 Second case of SUB operation

EXPERIMENTAL RESULTS

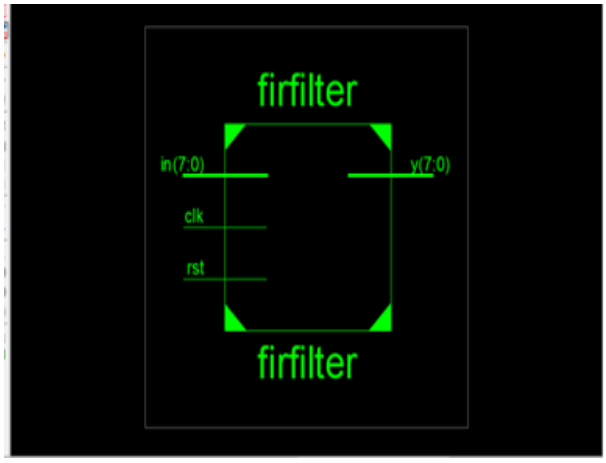

Fig:-6 Firfiter

Fig:-7 Simulater Results

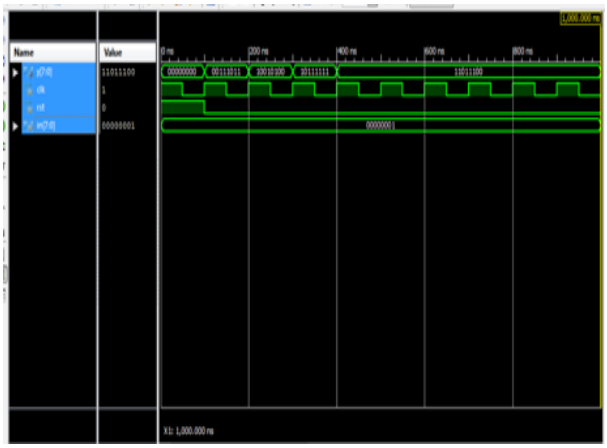

Fig:-8 Final Result

4. CONCLUSION

In this, the resource minimization formalization for designing digit-serial MCM operation with optimal area at the gate level by considering the implementation costs of digit-serial additament, subtraction, and shift operations was introduced. Since there are still instances with which the exact prevalent sub-expression algorithm cannot cope. But acquisitive scheduling algorithm that finds the best partial products in each iteration which yield the optimal gate level area in digit-serial MCM design was proposed. The experimental results denote that the sundry pipelined FIR filter, Parallel processing FIR filter implementation of Multiple Constant Multiplication. By utilizing MCM implementation with Acquisitive scheduling algorithm, we are achieved 30.55% area reduction and 4.5% delay reduction compared to subsisting algorithms. The future work will enhance to develop the Multiple Constant Multiplication (MCM) design by introducing the Commixed Integer Programming (MIP) algorithm. This algorithm is utilized to

5. REFERENCES

[1] Yu Pan and Pramod Kumar Meher, Senior Member, IEEE, ―Bit-Level Optimization of Adder-Trees for Multiple Constant Multiplications for Efficient FIR Filter Implementation‖, IEEE Transactions on Circuits and Systems—I: Regular Papers, Vol. 61, No. 2, February 2014.

[2] D. R. Bull and D. H. Horrocks, ―Primitive operator digital filter, IEE Proceedings-G, vol. 138, no. 3, pp. 401–412, Jun. 1991.

[3] A. G. Dempster and M. D. Macleod, ―Use of minimumadder multiplier blocks in FIR digital filters, IEEE Trans. Circuits Syst. II, Analod Digit. Signal Process, vol. 42, no. 9, pp. 569–577, 1995.

[4] S. D. S. M. Mehendale and G. Venkatesh, ―Synthesis of multiplier-less FIR filters with minimum number of additions, in Proc. IEEE ICCAD, 1995.

[5] I. C. Park and H. J. Kang, ―Digital filter synthesis based on minimal signed digit representation, in Proc. Design Autom. Conf. (DAC), 2001.

[6] Y. Voronenko and M. Püschel, ―Multiplier less multiple constant multiplication,‖ ACM Trans. Algorithms, vol. 3, no. 2, 2007.

[7] P. K. Meher and Y. Pan, ―Mcm-based implementation of block fir filters for high-speed and low-power applications, in Proc. VLSI and System-on-Chip (VLSI-SoC),

2011 IEEE/IFIP 19th Int. Conf., Oct. 2011, pp. 118–121.

[8] L. Aksoy, C. Lazzari, E. Costa, P. Flores, and J. Monteiro, ―Design of digit-serial FIR filters: Algorithms, architectures, and a CAD tool, IEEE Trans. Very Large Scale Integration (VLSI) Syst., vol. 21, no. 3, pp. 498–511, Mar. 2013.

[9] M. B. Gately, M. B. Yeary, and C. Y. Tang, ―Multiple real-constant multiplication with improved cost model and greedy and optimal searches in Proc. IEEE ISCAS, May 2012, pp. 588–591.

[10] M. Kumm, P. Zipf, M. Faust, and C.-H. Chang, ―Pipelined adder graph optimization for high speed multiple constant multiplication, in Proc. IEEE ISCAS, May 2012, pp. 49–52.