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MPEG encoders that optimizes power consumption with the goal of maintaining a particular PSNR

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Abstract:-

Image and video compression algorithms, such as JPEG, MPEG, and so on, are particularly attractive candidates for approximate computing which can be exploited to realize highly power-efficient implementations of these algorithms. However, existing approximate architectures typically fix the level of hardware approximation statically and are not adaptive to input data. For example, if a fixed approximate hardware configuration is used for an MPEG encoder the output quality varies greatly for different input videos. Architecture for MPEG encoders that optimizes power consumption with the goal of maintaining a particular Peak Signal-to-Noise Ratio (PSNR) threshold for any video. Toward this end, we design reconfigurable adder/sub tractor blocks (RABs), which have the ability to modulate their degree of approximation, and subsequently integrate these blocks in the motion estimation and discrete cosine transform modules of the MPEG encoder. We propose two heuristics for automatically tuning the approximation degree of the RABs in these two modules during runtime based on the Characteristics of each individual video. Note that although the proposed reconfigurable approximate architecture is presented for the specific case of an MPEG encoder, it can be easily extended to other DSP applications.

Key Words: - Approximate circuits, approximate, computing, low power design, quality configurable.

1. INTRODUCTION

Digital signal processing (DSP) blocks from the Backbone of various multimedia applications used in portable devices. Most of the DSP blocks implement image and video compression algorithms. Approximate computing architectures exploit the fact that a small relaxation in output correctness can result in significantly simpler and lower implementations. However, most approximate hardware architectures proposed so far suffer from the limitation

that, for widely varying input parameters, it becomes very hard to provide a quality bound on the output, and in some cases, the output quality may be severely degraded. The main reason for this output quality fluctuation is that the degree of approximation (DA) in the hardware architecture is fixed statically and cannot be customized for different inputs. This paper adopts a different approach to addressing this problem by dynamically reconfiguring the approximate hardware architecture depending on the inputs. Following contributions are 1) I demonstrate that, for a fixed level of hardware approximation in an MPEG encoder, the output quality varies widely across different videos, often going below acceptable limits. This shows that setting the level of hardware approximation statically is insufficient. 2) I investigate, for this paper, the use of dynamically reconfigurable approximate hardware architectures that vary the degree of approximation during run-time across multiple computational cycles, depending on the inputs. 3) Toward this end , I propose the design of reconfigurable adder/subtractor blocks for four commonly used adder architectures, viz, ripple carry adder , carry look ahead adder, carry bypass adder, and carry select adder, and subsequently integrate them into the MPEG encoder to enable quality configuration execution. 4) I propose a design methodology to adapt a degree of approximation dynamically based on the characteristics with the main aim of maintaining the output quality. 5) I have implemented the proposed architecture for an MPEG encoder on an Dual mode full adder (DMFA). My experimental results show that the proposed architecture results in power savings compare to a baseline approach that uses reconfigurable approximate architecture with the goal of maintaining a particular peak signal-to-noise ratio (PSNR) threshold for any video.

2. RELATED WORK

There has been a lot of effort in constructing energy-efficient video compression schemes. Different methods of power reduction include algorithmic modification[1],[2],voltage over scaling[3] and imprecise computation of metrics[4]. Approximate computing methods achieve a large amount of power savings by introducing a small amount of error or inaccuracy into the logic block. Different approaches for approximation include error introduction through voltage overcalling.[5],[6]. Intelligent logic

manipulation [7] and circuit simplification using don't care based optimization techniques[8]. The methods in [9] and [10] introduce imprecision by replacing adders with their approximate counterparts. There also exist instances of approximations introduced in the MPEG encoder. Most of them exploit the inherent error resilience of the motion estimation algorithm which results in minor quality degradation. For example use a bit width compression technique to reduce power consumption video frame memory and use bit truncation to introduce approximations in the ME block of the MPEG encoder. Note that, a preliminary version of this paper appeared in. Finally, we provide a comparative study of the power consumption of the different RAB s and also demonstrate how the DA is automatically regulated across different frames during runtime.

3. IMPLEMENTATION

Chip/Floor Plan

Level At this point, the power characteristics for the entire die are planned and power/delay budgets' are allocated. Vdd and Vth are determined based on performance goals. Power due to the assembly of macro blocks (interconnect and clock nets) is optimized, subject to delay and area/routability constraints. As macro blocks are instantiated, this high level information is updated and budgets may be adjusted to increase/decrease specifications on other sub-blocks.

Macro block Level

This stage comprises the assembly of gates into a basic function such as a block of control logic, or an arithmetic unit. In a standard cell design methodology, it is at this point that the implementer's intellectual property enters the design flow. As such, the various methods of implementing a particular function impact both power and delay. The number of power optimization techniques available at this level is numerous.

Gate/Circuit Level

This is lowest level stage visible to the designer, where transistors are assembled into basic gates. In a standard cell methodology, the fundamental gates used in macro block assembly are defined here. Power optimizations are very restricted at this level, as delay specification often dictates the power at which a device will operate. Emphasis is placed on reducing device parasitics and area while maximizing routability. A full custom approach may succeed in achieving lower powerthan a

standard cell approach, as individual transistor sizing may overcome certain obvious inefficiencies. More aggressive circuit families, such as dynamic logic, dual rail logic, or low-swing logic can be implemented at this stage, but these often require complicated design flows (e.g., through the introduction of clocks, noise sensitive nets, the need for level conversion, etc.) In our work, we focus on a standard cell CMOS methodology, as this is the most common Method for quickly and efficiently assembling a digital integrated circuit. As such, a number of clever and useful circuit techniques cannot be applied due to the complications which their use introduces in the design flow. Therefore, the performance of designs achievable by a standard cell based implementation is sub-optimal, but the ease of implementation of such a flow allows exploration of a wide range of designs.

Power Vs Energy

The distinction between the terms power and energy is important to this discussion. Note that energy is a measure of the total number of Joules dissipated by a circuit, whereas power refers to the number of Joules dissipated over a certain amount of time. Properly speaking, power reduction is a different goal than energy reduction. Power can be a problem primarily when heat removal is a concern. If too many Joules of energy areconverted into heat within a short amount of time, a package‘s heat sink may not be able to redistribute this heat quickly enough; the result will be a rise in temperature and subsequent thermal failure.

MPEG compression scheme

MPEG is mostly preferred for the video compression scheme in modern video devices and applications. MPEG- 2/MPEG-4 standards are used to squeezed to very small sizes. MPEG uses both Interframe and Intraframe encoding for video compression. Intraframe encoding involves encoding the entire frame of data, while Interframe encoding utilizes predictive and interpolative coding techniques as means of achieving compression. The interframe version exploits the high temporal redundancy between adjacent frames and only encodes the differences in information between the frames, thus resulting in great ratios. In this case, the encoding takes placed based upon the differences between the current frame and previous frame in the video sequence.

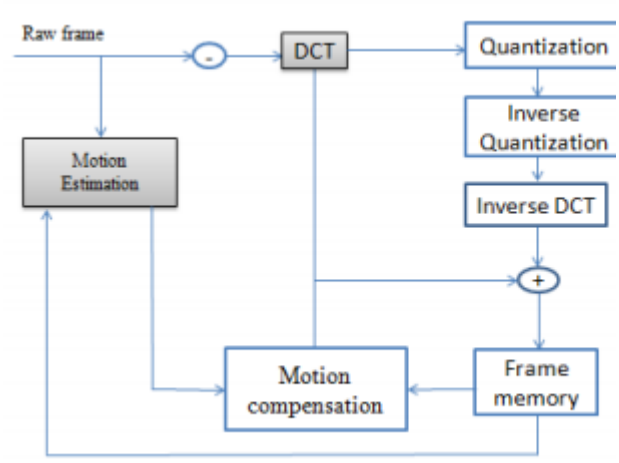

Fig:-1 MPEG encoder block diagram

There are three kinds of frames used in MPEG encoding: 1. I-frames means intraframe encoded. 2. P-frames means predictive encoded. 3. B-frames means bidirectional encoded. An I-frame is encoded as it is without any data loss and usually precedes each MPEG data stream. P-frames are constructed using the difference between the current frame and the immediately preceding I or P frame. B-frames are produced neighbor to the closest two I/P frames on either side of the current frame. The I, B and P frames are compressed when subjected to DCT. It is used to remove the existing frame. A significant portion of the inter frame encoding is spent in calculating motion vectors (MVs) from the computed differences. Every non encoded frame is divided into Macro blocks (MBs), such as 16 × 16 pixels. The Motion vectors (MVs) actually contain the information regarding the relative displacements of the Macro blocks (MBs) in the present frame in comparison with the reference.

4. EXPERIMENTAL RESULTS

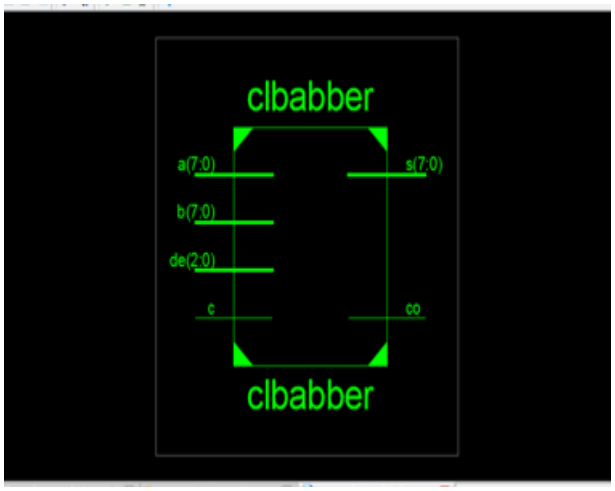

Fig:-2 Processer

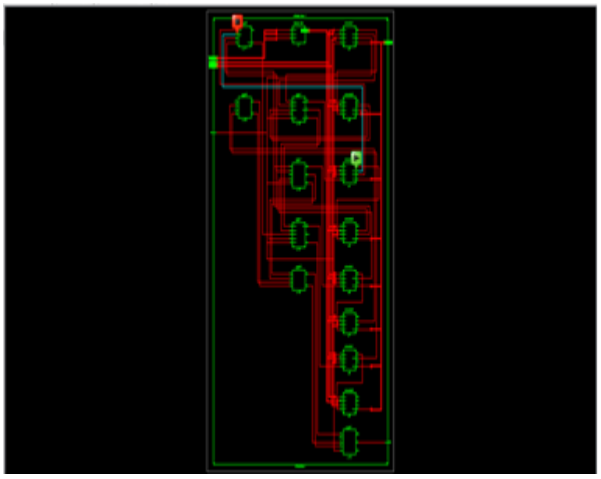

Fig:-3 Circuit

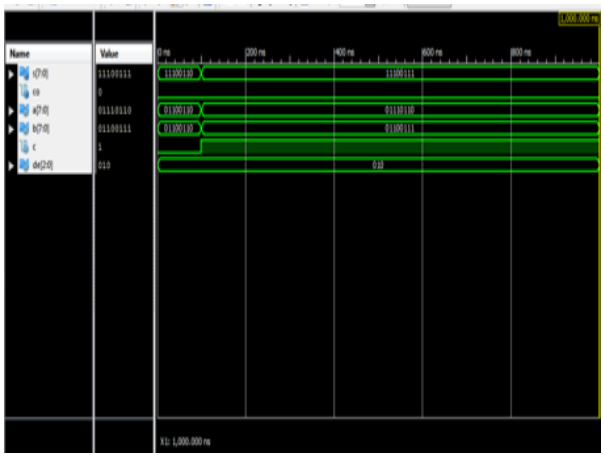

Fig: - 4 Simulation Results

5. CONCLUSION

This paper proposed a reconfigurable approximate architecture for the MPEG encoders that optimize power consumption while maintain a output quality across different input videos. The proposed architecture is based on the input characteristics. It requires the user to specify only the overall minimum quality for videos instead of having to decide the level of hardware approximation. Our experimental results show that the proposed architecture results in power savings equivalent to a baseline approach that uses fixed approximate hardware while respecting quality constraints across different videos. Future work includes the incorporation of other approximation techniques and extending the approximations to other arithmetic and functional blocks.

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