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New scheme to protect parallel FFT using cardiac commonly in modern signal processing circuits

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Abstract: - The uses of FFTs are unavoidable in communication systems. As most of the information may be analog in this world and as transmission of information in digital form is more acceptable and efficient, FFTs plays an important role in present communication scenario. For a reliable communication the information that we transmit should be reached at the destination as such. But due to many factors the information that we transmits get altered. One of the main problems in communication system is soft error. Even though soft error doesn't make any physical damage to the communication system it is dangerous. It has the ability to alter the values stored in the system. It may alter the transmitted message. A lot of techniques are available to detect the soft error and correct it. Those include TMR, ECC, parity SOS, and parity-SOS-ECC. All these assume that there can only be a single error in the circuit. The proposed system known as reduced precision redundancy considers Instead of using two full precision FFTs it uses two half precision FFTs as redundant FFTs. It limits the error, reduces area and power consumption.

Keywords: - Reduced Precision Redundancy, Fast Fourier transforms (FFTs), Soft errors

1. INTRODUCTION

Error correction code (ECC) techniques have been widely used to correct transient errors and improve the reliability of memories. ECC words in memories consist of data bits and additional check bits because the ECCs used in memories are typically from a class of linear block codes. During the write operations of memories, data bits are written in data bit arrays, and check bits are concurrently produced using the data bits and stored in check bit arrays. The check bit arrays, just like the data bit arrays, should be tested prudently for the same fault models if reliable error correction is to be insured[1]. Fast Fourier transform is used to convert a signal from time domain to frequency & this is needed so that you can

view the frequency components present in a signals. If you know the frequency components present in a signals you can play with the signals :) Let's say, u want to design a low pass filter and want to decide on the cut off frequency of the filter. If you have the frequency domain details for a signals u can clearly identify the frequency components which u want to retain & the ones which u want to take out[2]. Environmental interference and physical defects in the communication medium can cause random bit errors during data transmission. Error coding is a method of detecting and correcting these errors to ensure information is transferred intact from its source to its destination. Error coding is used for fault tolerant computing in computer memory, magnetic and optical data storage media, satellite and deep space commu nications, network communications, cellular telephone networks, and almost any other form of digital data communication. Error coding uses mathematical formulas to encode data bits at the source into longer bit words for transmission. The "code word" can then be decoded at the destination to retrieve the infor mation. The extra bits in the code word provide redundancy that, according to the coding scheme used, will allow the destination to use the decoding process to determine if the communication medium introduced errors and in some cases correct them so that the data need not be retransmitted. Different error coding schemes are chosen depending on the types of errors expected, the communication medium's expected error rate, and whether or not data retransmission is possible. Faster processors and better communications technology make more complex coding schemes, with better error detecting and correcting capabilities, possible for smaller embedded systems, allowing for more robust communications. However, tradeoffs between bandwidth and coding overhead, coding complexity and allowable coding delay between transmissions, must be considered for each application. Transient errors can often upset more than one bit producing multi-bit errors with a very high probability of error occurrence in neighboring memory cells . Bit interleaving is one technique to remedy multi-bit errors in neighboring memory cells as physically adjacent bits in memory array are assigned to different logical words [5],[6]. The single-error-correction, doubleerror-detection, and double-adjacent-error-correction (SEC-DED-DAEC) codes have previously been

presented to correct adjacent double bit errors [4]-[7]. The required number of check bits for the SEC-DEDDAEC codes is the same as that for the SEC-DED codes

2. RELATED WORK

Existing System

This work starts with the protection scheme based on the use of parity-SOS for digital filters. In the first technique, original module consist of 4 FFTs. Input is given to each FFTs separately as x1,x, x3, x4. Here the idea is that each filter can be the equivalent of a bit in an ECC and parity check bits can be computed using addition. Each FFT consist of a SOS check in parallel to detect the error in the FFT. The output of the Parseval check is represented as P1, P2, P3, and P4. If there is any error in the FFT then the Pi will set to 1

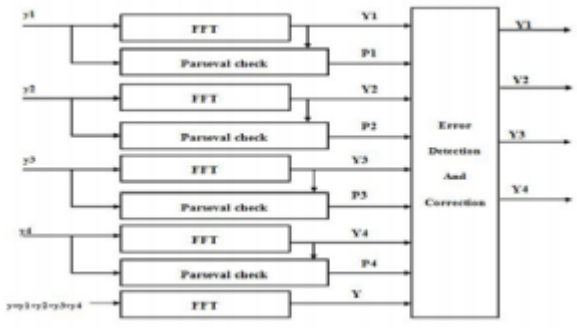

Fig:- 1 Parity-SOS

The output of the FFT and the Pi outputs are given to error detection and correction block. If there is any error in the FFT output then the additional FFT which is given parallel to the FFT module will correct the error. This Parseval check can only detect the errors in the FFT. It can't correct it by its own. For that an additional FFT is used. We can correct the error using its output. The SOS check can be combined with the ECC approach to reduce the protection overhead in first technique for parallel FFTs. Since the SOS check can only detect errors, the ECC part should be able to implement the correction. This is done using the equivalent of a simple parity bit for all the FFTs. The SOS check is used on each FFT to detect errors. When an error is detected then the output of the parity FFT can be used to correct the error. Instead of using an SOS check per FFT we can use an ECC for the SOS checks

Proposed System

This project is detecting multiple errors and corrects it with less over heads. It's better than the traditional method known as triple modular redundancy. A less expensive hardware mitigation strategy for arithmetic circuits called reduced-precision redundancy (RPR) is the proposed project. RPR is designed to protect against large magnitude errors. It is used mainly in arithmetic circuits with the help of redundant, lower precision arithmetic circuits and comparing their

results. Using of Reduced Precision Redundancy may introduce low precision errors but still its area reduction make it an attractive alternative for protecting FFTs, transient and soft data errors. There are some conditions to be satisfied while designing a RPR module. These choices include the reduced precision and threshold. RPR is implemented by creating two identical reduced-precision (RP) module of the original full precision FFTs. The outputs of the two RP modules are used to determine if there is any error in the FP module than a preset threshold, Th, the FP module is assumed to be in error. When the FP module is found to be in error, then it will discard the FP output and use RP output with 000's appended at the LSB part. If the FP output differs from the RP outputs by less than Th, then it is considered as the error free output and the final output will be FP output. The arithmetic circuits protected by RPR may be of any size. The circuit used may be of basic arithmetic operation such as an adder or a more complex combination of operators and logics such as an infinite impulse response filters, finite impulse response (FIR) filter etc. This paper refers to the combination of FP module and RP module. There are two parameters to be considered before implementing RPR on a module. They are the bit width of the reduced precision module (Br) and the decision threshold (Th). The two values are linked and together greatly affect the cost and performance of RPR.

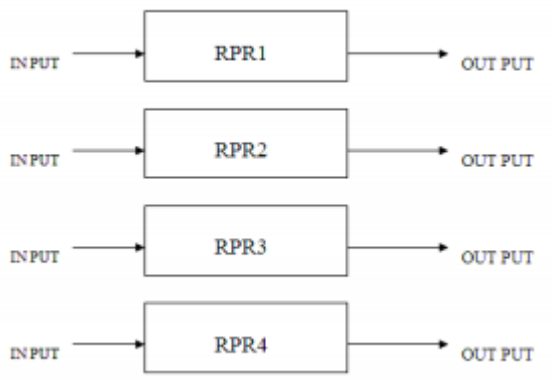

Fig:-2 Block diagram of RPR technique

It is used to detect and correct errors in the parallel FFTs. Input given to this block consist of 4 inputs with each input six bit long. Each block is having the same function. Only the input will be different.

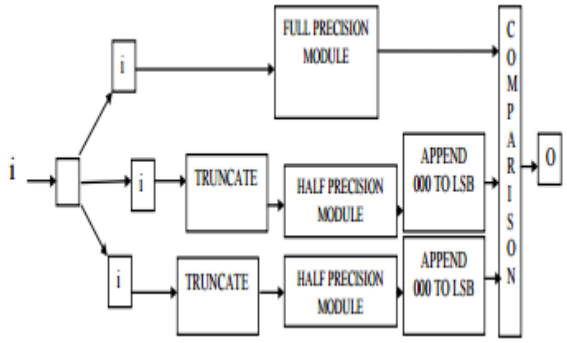

Fig: - 3 A single RPR module

A single RPR module. Same input is given to all these three section. First part is known as full precision module because it computes

the FFT output as such i.e. the input of the FFT module is same as the input that we give at the starting section. Second and third part is known as reduced precision module because it uses the truncated input as the input to the FFT. Both full precision module and reduced precision module use four point FFT. Since this project is mainly intended to find out the error and correct it we are not giving much importance to FFT design. We are considering a simple radix 4 DIF FFT.

RPR module consists of three parallel paths. One consists of full precision module. Other two consist of half precision module. First input is given. Input is four points. i.e. there will be 4 inputs and each input will be six bit long. In the first part these four inputs are given as such to full precision module. Full precision module will give a four point DIF FFT output which is six bit long. In the second and third part also same six bit input is given. Then it is given to truncation block. Truncation block will truncate the six bit input to three bit input. Truncation is done by removing 3 bits from the LSB part. So the input to half precision module is 3bit inputs and output will be 3 bit output which is four point DIF FFT output. Then output of full precision module is given to the comparison block directly. But in the case of half precision module the output of the FFT is given to another block before giving to comparison. Here in this block three bits 000 is appended at the LSB part of the FFT output to make the output as six bit output. All these six bit outputs are given to comparison block. In the comparison block comparison of each output is done. There will be four outputs from each block. If the output of the full precision is less than a particular threshold value, then that output is taken as the final output. If the output of the full precision module is greater than the threshold and if the output of both the half precision modules are equal then that value is taken as the final output. Threshold value is set by doing a lot of computation. We are not comparing the outputs of all the modules directly. Instead we are comparing it with the help of a threshold value. It's mainly because truncated output is used in two half precision modules. Thus the output will be with less error. The full and half precision module we use is four point DIF FFT. Since this project is mainly for error detection and correction the FFT design is not having much importance. So we are using a simple FFT. The FFT used here is radix 4 DIF FFT.

3. EXPERIMENTAL RESULTS

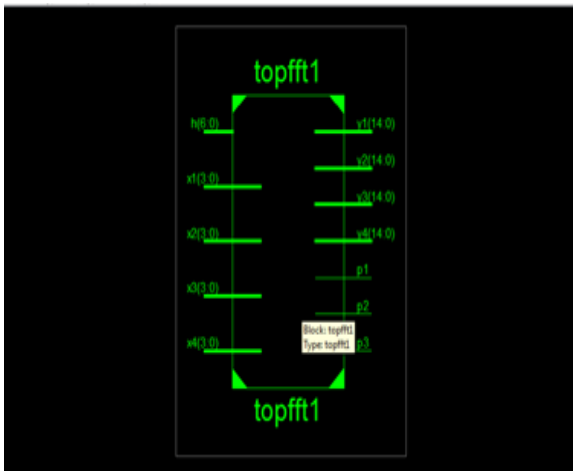

Fig:-4 Processer

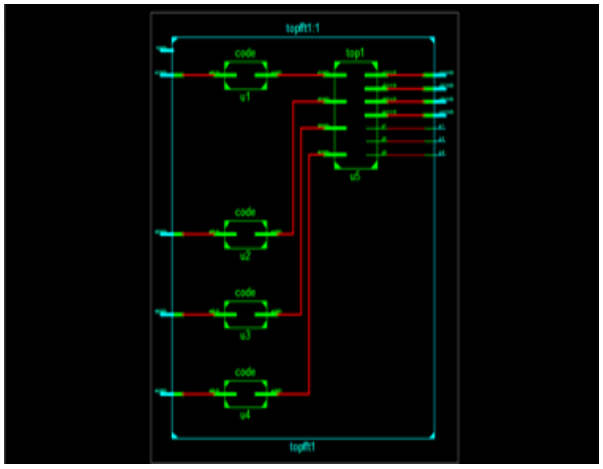

Fig:-5 Circuit

Fig:-6 Simulation Results

4. CONCLUSION

Detecting and correcting errors such as critical reliability are difficult in signal processing which increases the use of fault tolerant implementation. In modern signal processing circuits, it is common to find several filters operating in parallel. Proposed is an area efficient technique to detect and correct single errors. This brief has presented a new scheme to protect parallel FFT using cordic that is commonly found in modern signal processing circuits. The approach is based on applying SOS-ECC check to the parallel FFT outputs to detect and correct errors. The SOS checks are used to detect and locate the errors and a simple parity FFT is used for correction. The 8 point FFT with the input bit length 32 is protected using the proposed technique. . The detection and location of the errors can be done using an SOS check per FFT or alternatively using a set of SOS checks that form an ECC. This technique can detect and correct only single bit error and it reduces area results in high speed compared to existing techniques.

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