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Design Pulse-Triggered Flip-Flop Based on Signal Feed-Through Scheme with Low-Power

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Abstract:
Practically, clocking system like flip-flop (FF) consumes large portion of total chip power. In this paper, a novel low-power pulse-triggered flip-flop (FF) design is presented. Pulse-triggered FF (P-FF) has been considered as a popular alternative to the conventional master –slave based FF in the applications of high speed. First, a simple two-transistor AND gate design is used to reduce the circuit complexity. Second, a conditional pulse-enhancement technique is devised to speed up the discharge along the critical path only when needed. As a result, transistor sizes in delay inverter and pulse-generation circuit can be reduced for power saving. The maximum power saving against rival designs is up to 39.4%.Compared with the conventional transmission gate-based FF design; the average leakage power consumption is also reduced by a factor of 3.52.

Index Terms *– Flip-flop, low power, pulse-triggered*

I. INTRODUCTION

Flip-flops (FFs) are the basic storage elements used extensively in all kinds of digital designs. In particular, digital designs now-a-days often adopt intensive pipelining techniques and employ many FF-rich modules. It is also estimated that the power consumption of the clock system, which consists of clock distribution networks and storage elements, is as high as 20%–45% of the total system power. Traditional master-slave flip-flops are made up of two stages, one master and one slave and they are characterized by their hard-edge property. Alternatively, pulse-triggered flip-flops reduce the two stages into one stage and are characterized by the soft edge property. Pulse-triggered FF (P-FF) has been considered a popular alternative to the conventional master–slave based FF in the applications of high-speed operations. Besides the speed advantage, its circuits simplicity are also beneficial to lowering the power consumption of the clock tree system. The circuit complexity of a P-FF is simplified since only one latch, as opposed to two used in conventional master–slave configuration, is needed. P-FFs also allow time borrowing across clock cycle boundaries and feature a zero or even negative setup time. Depending on the method of pulse generation, P-FF designs can be classified as implicit or explicit. In an implicit-type P-FF, the pulse generator is a built-in logic of the latch design and no explicit pulse

signals are generated. In an explicit-type PFF, the designs of pulse generator and latch are separate. Implicit pulse generation is often considered to be more power efficient than explicit pulse generation. In this paper, we will present a novel low-power implicit-type P-FF design featuring a conditional pulse-enhancement scheme. Three additional transistors are employed to support this feature. In spite of a slight increase in total transistor count, transistors of the pulse generation logic benefit from significant size reductions and the overall layout area is even slightly reduced.

II. IMPLICIT-TYPE P-FF DESIGN WITH PULSE CONTROL SCHEME

A.Conventional Implicit-Type P-FF Designs

1)ip-DCO: ip-DCO is known as the implicit data close to output. It is an implicit type flip-flop. In this method the pulse is generated inside the flip-flop. A state-of-the-art P-FF design, named ip-DCO, is given in Fig.1. It contains an AND logic-based pulse generator and a semi-dynamic structured latch design. Semi-Dynamic Flip-Flop is a high performance flip-flop because of its small delay and simple topology. It is measured to be one of fastest flip-flops today.

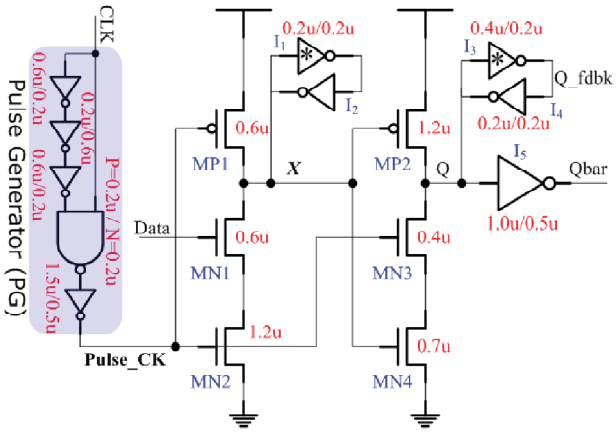

Figure1. ep-DCO

Inverters I5 and I6 are used to latch data and inverters I7 and I8 are used to hold the internal node X. The pulse generator takes complementary and delay skewed clock signals to generate a transparent window equal in size to the delay by inverters I1-I3. Two practical problems exist in this design. First, during the rising edge, nMOS transistors N2 and N3 are turned on. If data remains high, node X will be discharged on every rising edge of the clock. This leads to a large switching power.

2)MHLFF: The modified hybrid latch flip-flop is known as MHLFF and this is an type of implicit type flip-flop. MHLFF shows an improved P-FF design in fig.2. It employs a static latch structure. A static latch can remember as long as gate power is

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on the charge on a capacitor. Node X is no longer precharged periodically by the clock signal. A weak pull-up transistor P1 controlled by the FF output signal Q is used to maintain the node level at high when Q is zero.

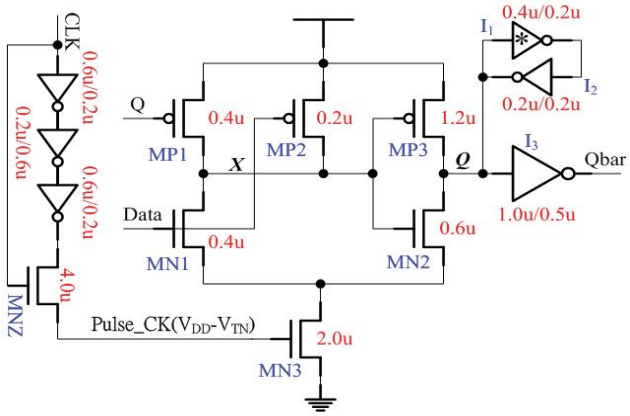

Figure2. MHLFF

This design eliminates the unnecessary discharging problem at node. However, it encounters a longer Data-to-Q (D-to-Q) delay during "0" ,"1" transition because node is not pre-discharged. Larger transistors N3 and N4 are required to enhance the discharging capability. Another drawback of this design is that node becomes floating when output Q and input Data both equal to "1". Extra DC power emerges if node X is drifted from an intact"1".

3)SCCER: SCCER is known as the single ended conditional capturing energy recovery P-FF. It is a refined low power P-FF design using a conditional discharged technique. This technique is also used to present a new flip-flop Conditional Discharge flip-flop (CDFF). CDFF use a pulse generator which is suitable for double edge sampling. CDFF has two stages. First is responsible for capturing the Low-to-High transition and second stage captures the High-to-Low input transition. In this SCCER design, the keeper logic is replaced by a weak pull up transistor P1 in conjunction with an inverter I2 to reduce the load capacitance of node. The discharge path contains nMOS transistors N2 and N1 connected in series. In

order to eliminate superfluous switching at node, an extra nMOS transistor N3 is employed. Since N3 is controlled by Q_fdbk, no discharge occurs if input data remains high.

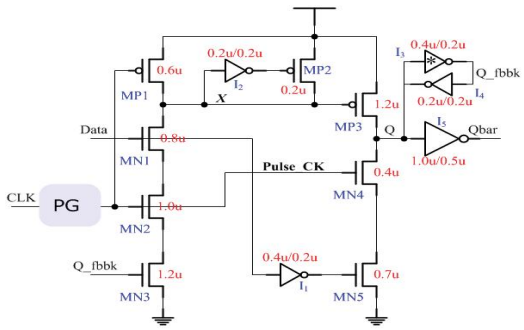

Figure3.Static-CDFF

The worst case timing of this design occurs when input data is "1" and node is discharged through four transistors in series, i.e., N1 through N4, while combating with the pull up transistor P1. A powerful pull-down circuitry is thus needed to ensure node can be properly discharged. This implies wider N1 and N2 transistors and a longer delay from the delay inverter I1 to widen the discharge pulse width.

III. PROPOSED P-FF DESIGN

Fig. 4 shows the proposed design. The proposed design, adopts two measures to overcome the problems associated with existing P-FF designs. The first one is reducing the number of nMOS transistors stacked in the discharging path. The second one is supporting a mechanism to conditionally enhance the pull down strength when the input data is "1." As opposed to the transistor stacking design in Fig. 1 and Fig. 3, transistor N2 is removed from the discharging path. Transistor N2, in conjunction with an additional transistor N3, forms a two-input pass transistor logic (PTL)-based AND gate to control the discharge of transistor N1. Pass transistors require lower switching energy to charge up a node, due to the reduced voltage swing.

In SCCER design, the discharge control signal is driven by a single transistor. Parallel conduction of two nMOS transistors (N2and N3) speeds up the operations of pulse generation. Thus the number of stacked transistors along the discharging path is reduced. To enhance the discharging condition, transistor P3 is added. When the FF output Q changes from 0 to 1 the conditional pulse enhancement technique effectively takes place. Thus this leads to the better power performance compared to the indiscriminate pulse enhancement approach.

The post layout simulations on various P-FF were conducted to obtain the performance figure of the proposed design. These designs include three flip-flops namely ip-DCO, MHLFF and

SCCER. And those designs are discussed above. The target technology is the UMC 90-nm CMOS process. The operating condition used in simulations is 500 MHz/1.0V.

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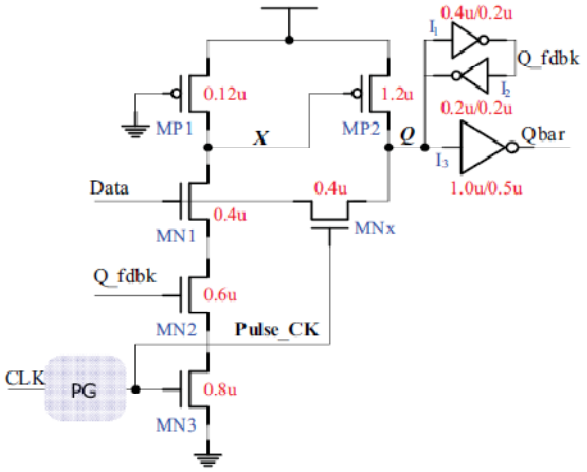

Figure4.Schematic of the proposed P-FF design.

with gate connected to the ground is used in the first stage of the TSPC latch. This gives rise to a pseudo-nMOS logic style design, and the charge keeper circuit for the internal node *X* can be saved. In addition to the circuit simplicity, this approach also reduces the load capacitance of node *X* [20], [21]. Second, a pass transistor MNx controlled by the pulse clock is included so that input data can drive node Q of the latch directly (the signal feed-through scheme). Along with the pull-up transistor MP2 at the second stage inverter of the TSPC latch, this extra passage facilitates auxiliary signal driving from the input source to node Q. The node level can thus be quickly pulled up to shorten the data transition delay. Third, the pull-down network of the second stage inverter is completely removed. Instead, the newly employed pass transistor MNx provides a discharging path. The role played by MNx is thus twofold, i.e., providing extra driving

to node Q during 0 to 1 data transitions, and discharging node Q during —1‖ to —0‖ data transitions. Compared with the latch structure

used in SCDFF design, the circuit savings of the proposed design include a charge keeper (two inverters), a pull-down network (two nMOS transistors), and a control inverter. The only extra component introduced is an nMOS pass transistor to support signal feed through. This scheme actually improves the —0‖ to —1‖ delay and thus reduces the disparity between the rise time and the fall time delays. In comparison with other P-FF designs such as ep-DCO, CDFF, and SCDFF, the proposed design shows the most balanced delay behaviors. The principles of FF operations of the proposed design are explained as follows. When a clock pulse arrives, if no data transition occurs, i.e., the input data and node Q are at the same level, on current passes through the pass transistor MNx, which keeps the input stage of the FF from any driving effort. At the same time, the input data and the output feedback Q_fdbk assume complementary signal levels and the pull-down path of node *X* is off. Therefore, no signal switching occurs in any internal nodes. On the other hand, if a —0‖ to —1‖ data transition occurs, node *X* is discharged to turn on transistor MP2, which then pulls node Q high. Referring

operations as the discharging path conducts only for a pulse duration. However, with the signal feed through scheme, a boost can be obtained from the input source via the pass transistor MNx and the delay can be greatly shortened. Although this seems to burden the input source with direct charging/discharging responsibility, which is a common pitfall of all pass transistor logic, the scenario is different in this case because MNx conducts only for a very short period. Referring to Fig. 2(c), when a —1‖ to —0‖ data transition occurs, transistor MNx is likewise turned on by the clock pulse and node Q is discharged by the input stage through this route. Unlike the case of —0‖ to —1‖ data transition, the input source bears the sole discharging responsibility. Since MNx is turned on for only a short time slot, the loading effect to the input source is not significant. In particular, this discharging does not correspond to the critical path delay and calls for no transistor size tweaking to enhance the speed. In addition, since a keeper logic is placed at node Q, the discharging duty of the input source is lifted once the state of the keeper logic is inverted.

IV. SIMULATION RESULTS

The performance of the proposed P-FF design is evaluated against existing designs through post-layout simulations. The compared designs include four explicit type P-FF designs shown in Fig.1, an implicit type P-FF design named SDFF, a TG latch based P-FF design ep-SFF, plus two non-P-FF designs. One of them is a conventional TG master–slave-based FF (TGFF) and the other one is an adaptive-coupling-configured FF design (ACFF) . A conventional CMOS NAND-logic-based pulse generator design with a three-stage inverter chain is used for all P-FF designs except the MHLFF design, which employs its own pulse generation circuitry as specified in Fig. The target technology is the TSMC 90-nm CMOS process.

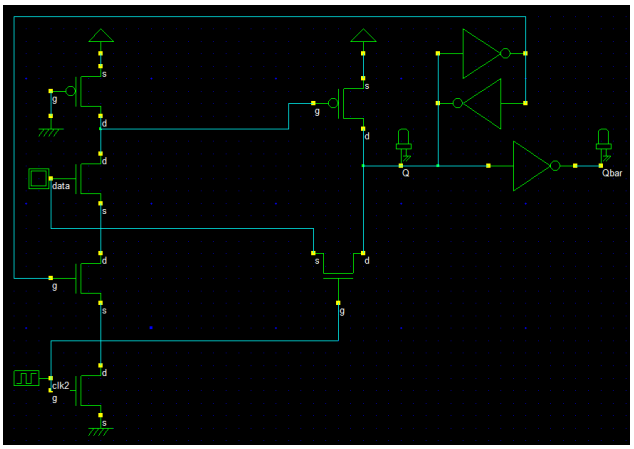

Figure 5. Schematic of the proposed flipflop.

Since pulse width design is crucial to the correctness of data capture as well as the power consumption, the transistors of the pulse generator logic are sized for a design spec of 120 ps in pulse width in the TT case. The sizing also ensures that the pulse generators can function properly in all process corners. With regard to the latch structures, each P-FF design is individually optimized subject to the product of power and D-to-Q delay. To mimic the signal rise and fall time delays, input

signals are generated through buffers. Since the proposed design

comparisons the power consumption of the data input buffer (an inverter) is included. The output of the FF is loaded with a 20-fF capacitor. An extra loading capacitance of 3-fF is also placed at the output of the clock buffer. The operating condition used in simulations is 500 MHz/1.0 V. Six test patterns, each representing a different data switching probability, are applied in simulations. Five of them are deterministic patterns, with 0% (all-0 or all-1), 12.5%, 25%, 50%, and 100% data transition probabilities, respectively.

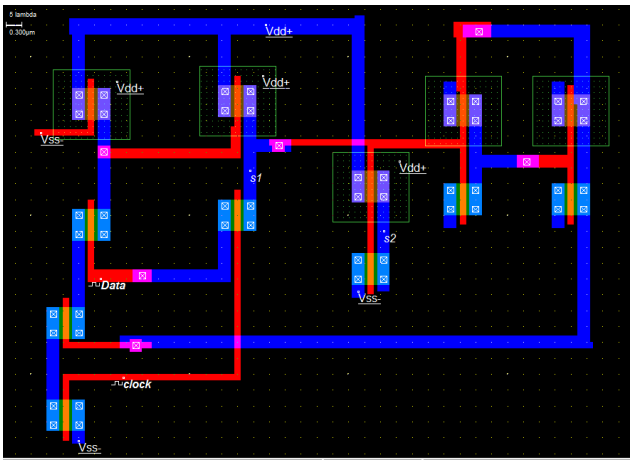

Figure 7. Layout of the proposed Flipflop

V. CONCLUSION

In this brief, we presented a novel P-FF design by employing a modified TSPC latch structure incorporating a mixed design style consisting of a pass transistor and a pseudo-nMOS logic. The key idea was to design in various performance aspects provide a signal feed through from input source to the internal node of the latch, which would facilitate extra driving to shorten the transition time and enhance both power and speed performance. The design was intelligently achieved by employing a simple pass transistor. Extensive simulations were conducted, and the results did support the claims of the proposed.

REFERENCES

[1] H. Kawaguchi and T. Sakurai, "A reduced clock-swing flip-flop (RCSFF) for 63% power reduction," *IEEE J. Solid-State Circuits*, vol. 33, no. 5,pp. 807–811, May 1998.

[2] K. Chen, "A 77% energy saving 22-transistor single phase Clocking D-flip-flop with adoptive-coupling configuration in 40 nm CMOS," in*Proc. IEEE Int. Solid-State Circuits Conf.*, Nov. 2011, pp. 338–339.

[3] E. Consoli, M. Alioto, G. Palumbo, and J. Rabaey, "Conditional pushpull pulsed latch with 726 fJops energy delay product in 65 nm CMOS," in *Proc. IEEE Int. Solid State Circuits Conf.*, Feb. 2012, pp. 482–483.

[4] H. Partovi, R. Burd, U. Salim, F.Weber, L. DiGregorio, And D. Draper, "Flow-through latch and edge-triggered flip-flop hybrid elements," in *Proc. IEEE Int. Solid-State Circuits Conf.*, Feb. 1996, pp. 138–139.

[5] F. Klass, C. Amir, A. Das, K. Aingaran, C. Truong, semi-dynamic and dynamic flip-flops with embedded logic for high-performance processors," *IEEE J. Solid-State Circuits*, vol. 34, no. 5, pp. 712–716, May 1999.

[6] V. Stojanovic and V. Oklobdzija, "Comparative analysis of Masterslave latches and flip-flops for high-performance and low-power systems,"*IEEE J. Solid-State Circuits*, vol. 34, no. 4, pp. 536–548, Apr. 1999.

[7] J. Tschanz, S. Narendra, Z. Chen, S. Borkar, M. Sachdev, and V. De,"Comparative delay and energy of single edge-triggered and dual edge triggered pulsed flip-flops for high-performance microprocessors," in *Proc. ISPLED*, 2001, pp. 207–212.

[8] S. D. Naffziger, G. Colon-Bonet, T. Fischer, R. Riedlinger, T. J. Sullivan, and T. Grutkowski, "The implementation of The Itanium 2 microprocessor," *IEEE J. Solid-State Circuits*, vol. 37, no. 11, pp. 1448–1460, Nov. 2002.

[9] S. Sadrossadat, H. Mostafa, and M. Anis, "Statistical design Framework of sub-micron flip-flop circuits considering die-to-die and within-die variations," *IEEE Trans. Semicond. Manuf.*, vol. 24, no. 2, pp. 69–79, Feb. 2011.

[10] M. Alioto, E. Consoli, and G. Palumbo, "General strategies to design nanometer flip-flops in the energy-delay space," *IEEE Trans. Circuits Syst.*, vol. 57, no. 7, pp. 1583–1596, Jul. 2010.

[11] M. Alioto, E. Consoli, and G. Palumbo, "Flip-flop energy/performance versus Clock Slope and impact on the clock network design," *IEEE Trans. Circuits Syst.*, vol. 57, no. 6, pp. 1273–1286, Jun. 2010.

[12] M. Alioto, E. Consoli, and G. Palumbo, "Analysis and comparison in the energy-delay-area domain of nanometer CMOS flip-flops: Part I-methodology and design strategies," *IEEE Trans. Very Large Scale Integr. (VLSI) Syst.*, vol. 19, no. 5, pp. 725–736, May 2011.

[13] M. Alioto, E. Consoli and G. Palumbo, "Analysis and comparison in the energy-delay-area domain of nanometer CMOS flip-flops: Part II - results and figures of merit," *IEEE Trans. Very Large Scale Integr. (VLSI) Syst.*, vol. 19, no. 5, pp. 737–750, May 2011.

[14] B. Kong, S. Kim, and Y. Jun, "Conditional-capture flip-flop for statistical power reduction," *IEEE J. Solid-State Circuits*, vol. 36, no. 8, pp. 1263–1271, Aug. 2001

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