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Application of Reversible Logic in Implement of High Speed Low Power Combinational and Sequential Circuits

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Abstract - Reversible logic has conferred itself as a distinguished technology that plays an essential role in Quantum Computing. Quantum computing devices in theory operate at immoderate high speed and consume infinitesimally less power. analysis tired this paper aims to utilize the thought of reversible logic to interrupt the traditional speed-power trade-off, thereby obtaining a step nearer to grasp Quantum computing devices. To demonstrate this analysis, numerous combinable and serial circuits are enforced like a 4-bit Ripple-carry Adder, (8- bit X 8-bit) Wallace Tree number, and also the management Unit of associate degree 8-bit GCD processor victimization Reversible gates. the ability and speed parameters for the circuits are indicated, and compared with their typical non-reversible counterparts. The comparative applied mathematics study proves that circuits using Reversible logic so are quicker and power economical. The styles conferred during this paper were simulated victimization Xilinx fourteen.4 software.

Key Words: grasp Quantum computing, GCD processor

1.INTRODUCTION

Reversible logic is wide employed in low power VLSI. Reversible circuits are capable of back-computation and reduction in dissipated power, as there's no loss of knowledge [1]. Basic reversible gates are used to realize the specified practicality of a reversible circuit. the individuality of reversible logic is that, there's no loss of knowledge since there's matched correspondence between inputs and outputs. this allows the system to run backwards and whereas doing thus, any intermediate style stage is completely examined. The fan-out of every block within the circuit must be one. This analysis paper focuses on implementation of reversible logic circuits within which main aim is to optimize speed of the look. A Reversible adder is intended victimization basic reversible gates. victimization this adder, associate degree 8-bit reversible ripple-carry adder is devised then compared with the traditional 8-bit adder in terms of speed, vital ways, hardware used. Then victimization a similar reversible adder, a Wallace tree number has been enforced, and compared with the traditional Wallace tree number. With the illustrious indisputable fact that serial circuits are the center of digital planning, the look for the management unit of a reversible GCD processor has been projected victimization Reversible logic gates.

1.1 Reversible logic

Reversible logic is one in every of the promlsmg fields for future low power style technologies. Since one in every of the necessities of all DSP processors and alternative handheld devices is to reduce power dissipation multipliers with high speed and lower dissipations are vital. This paper proposes associate degree

implementation of Reversible Urdhva Tiryakbhayam number that consists of 2 cardinal options. One is that the quick multiplication feature derived from religious writing formula Urdhva Tiryakbhayam and another is that the reduced chilling by the virtue of implementing the circuit victimization reversible logic gates. The paper is divided into six sections. Section eleven offers literature survey, Section 111 deals with reversible logic. Section IV explains the Urdhva Tiryakbhayam formula. Section V elaborates on the look aspects of Reversible Urdhva Tiryakbhayam number. Section VI introduces a replacement parameter named Total Reversible Logic Implementation price (TRLIC) to the literature victimization that our projected style is compared. Conc1usions and references follow.

2. LITERATURE REVIEW

Energy loss is a vital thought in digital circuit style. a district of this downside arises from the technological non quality of switches and materials. the opposite a part of the matter arises from Landauer's principle that there's no resolution. Landauer's Principle [3] states that logical computations that don't seem to be reversible essentially generate k*T*ln(2) joules of warmth energy, wherever k is that the constant k=1.38xlO-23 J/K, T is that the temperature at

which the computation is performed. though this quantity of warmth seems to be little, Moore's Law predicts exponential growth of warmth generated attributable to data lost, which is able to be a clear quantity of warmth loss in next decade.

Also by second law of natural philosophy any method that's reversible won't amendment its entropy. On thermo high-octane grounds, the erasure of 1 little bit of data from the mechanical degrees of a system should be amid the thermalization of associate degree quantity of k*T*ln (2) joules of energy. the knowledge entropy H is calculated for any chance distribution. equally the natural philosophy entropy S refers to natural philosophy possibilities specifically. so gain in entropy forever suggests that loss of knowledge, and zilch a lot of.

Design that doesn't lead to data loss is termed reversible. It naturally takes care of warmth generated attributable to data loss. Bennett [4] showed that zero energy dissipation would be attainable given that the network consists of reversible logic gates, so changeableness can become a vital property in future circuit style technologies.

3.REVERSIBLE LOGIC

Reversible logic may be a promising computing style paradigm that presents a way for constructing computers that manufacture no chilling. Reversible computing emerged as a results of the applying of quantum physics principles towards the event of a universal computer. Specifically, the basics of reversible computing are supported the link between entropy, heat transfer between molecules during a system, the chance of a quantum particle occupying a specific state at any given time, and also the quantum field theory between electrons once they are in dose proximity. the essential principle of reversible computing is that a bijective device with an even range of input and output lines can manufacture a computing surroundings wherever the electrodynamics of the system allow prediction of all future states supported illustrious past states, and

also the system reaches each attainable state, leading to no chilling .

3.1APPLICATIONS OF REVERSIBLE LOGIC GATES

3.1.1Reversible 4- bit full adder

The gate used in implementing a reversible ripple-carry full adder is the HNG gate. The HNG gate functions like a full adder. A reversible ripple-carry adder is faster than the non-reversible adder, since the computation of carry in a reversible adder does not require the computation of previous stage carry (as indicated in the critical paths).

When previous stage carry is being forwarded in the reversible adder, the computation of previous stage carry and computation regarding sum is done simultaneously whereas in an irreversible adder the next stage carry cannot start any computation till previous stage carry is fully generated. The critical paths of 4bit reversible and irreversible ripple-carry adders are as shown in fig.2.7 and fig.2.8

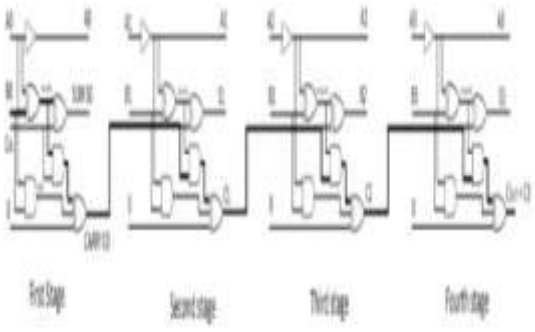

Fig1.Critical Path of 4-bit reversible adder

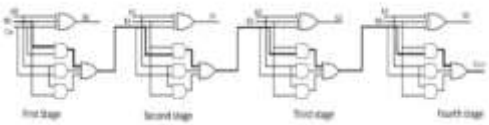

Fig2. Critical Path of 4 bit irreversible adder

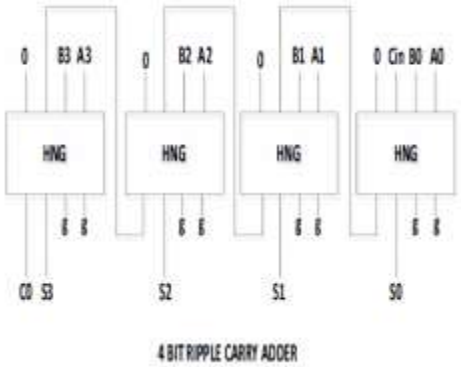

Fig3:4 Bit Ripple Carry Adder

4.WALLACE TREE MULTIPLIER

A Wallace tree is an efficient hardwired implementation of a digital circuit that multiplies two integers. The Wallace tree has three steps:

- Every bit of the multiplicand is multiplied (i.e. AND) by every bit of multiplier, thus yielding n^2 results (for n X n multiplication). Depending on position of the multiplied bits, the wires carry different weights, i.e. weight of bit carrying result of a5b6 is 65.
- The number of partial products is reduced to 2 by layers of full and half adders.
- The wires are grouped in two numbers, and added using a conventional adder.
- The circuit diagram of Wallace tree multiplier using reversible gates is shown in fig. 2.12

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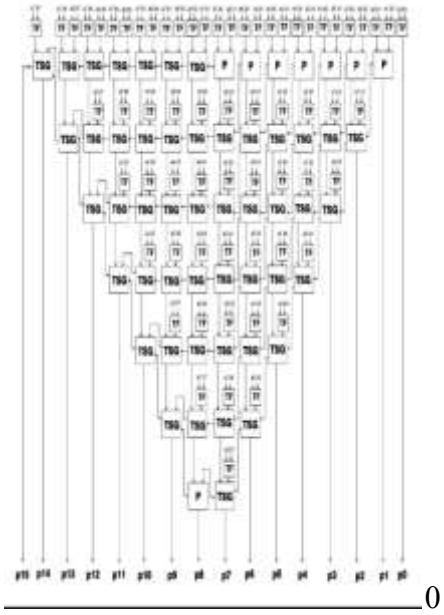

Fig4. 2.12 8X8 reversible Wallace tree Multiplier

Implementation of reversible and irreversible 8bit X 8bit Wallace tree multipliers were done and the comparison is as shown in table 2.2.

4.1 CONTROL UNIT FOR GCD PROCESSOR

To illustrate the classical and reversible approaches to the Sequential Control Unit Design, reversible logic is employed for a special purpose processor that computes the GCD of two numbers. This GCD processor incorporates standard Euclid's Algorithm involving Subtract-Compare-Swap operation of two numbers. The basic principle is to subtract smaller of the two numbers repeatedly from the other number until we get the number that divides another.

4.2Control Unit:

Control unit of GCD processor generates the control signals to manipulate the operations in Data-path.

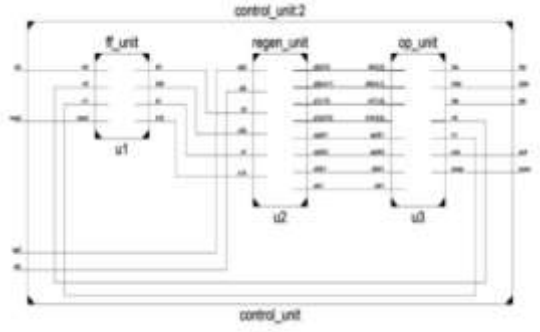

Fig. 4.1: Block diagram of GCD Control Unit

5. FLOW CHART

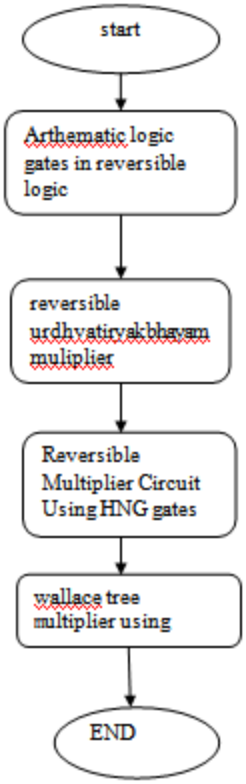

Fig 5: Flowchart of design

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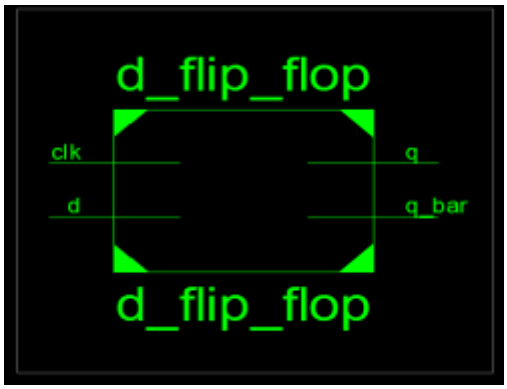
6.RESULTS AND ANALYSIS



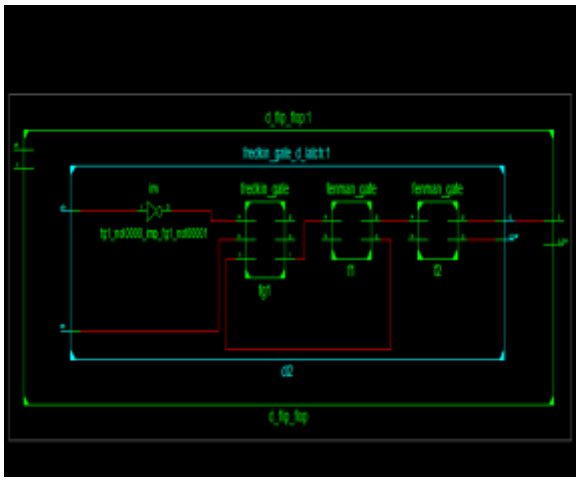
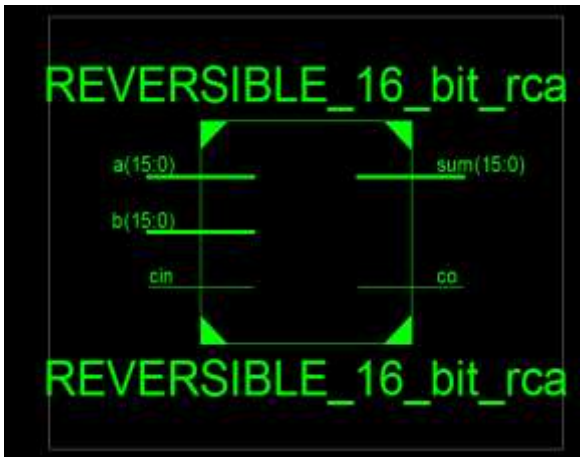


Fig 6 RTL of D-Flip flop using Reversible logic

Fig 7 Output wave form of D-Flip flop using Reversible logic



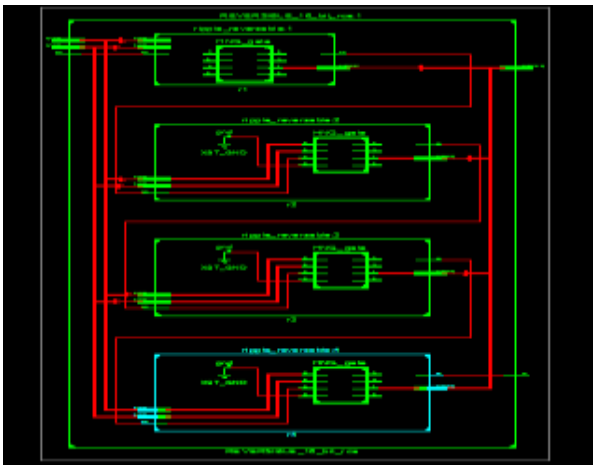


Fig 8 RTL of 16- bit adder using Reversible logic

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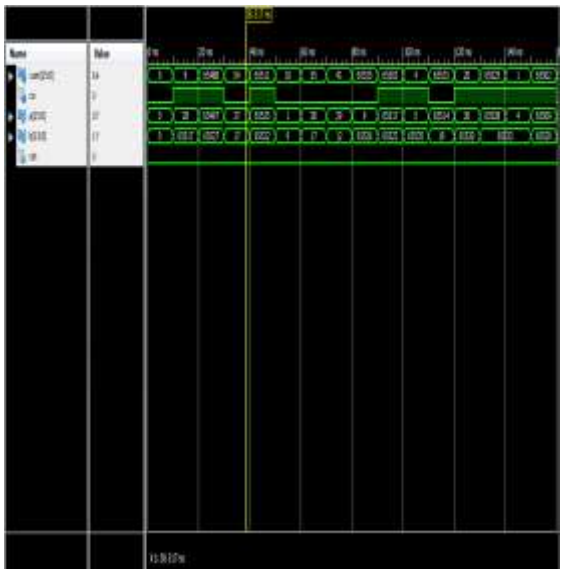
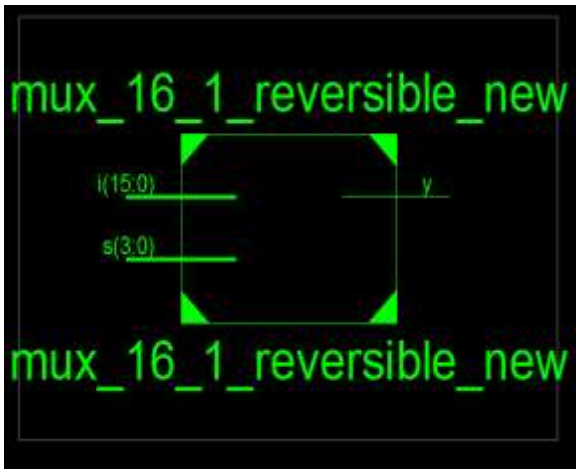


Fig 9 Output wave form of 16- bit adder using Reversible logic



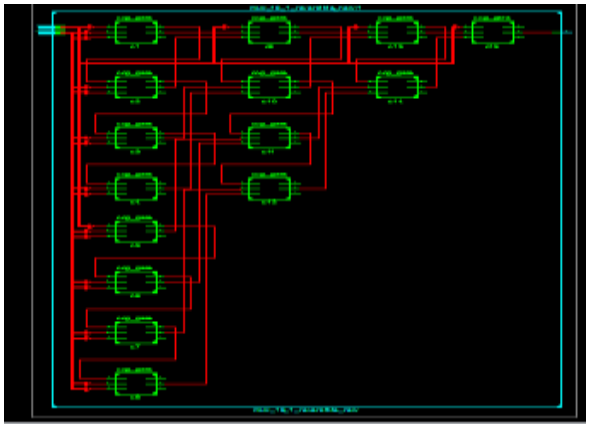
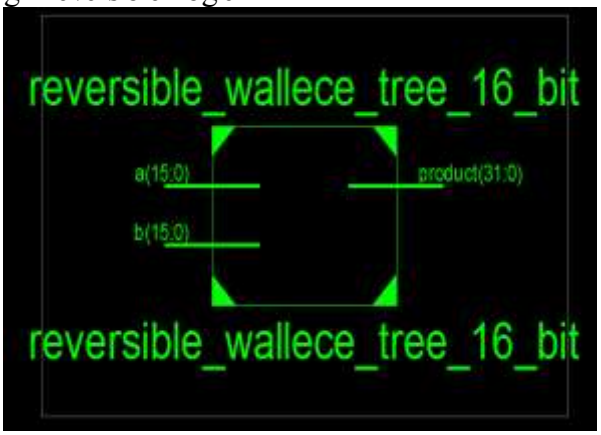


Fig 10 RTL of 16- bit MUX using Reversible logic

Fig 11 Output wave forms of 16- bit MUX using Reversible logic



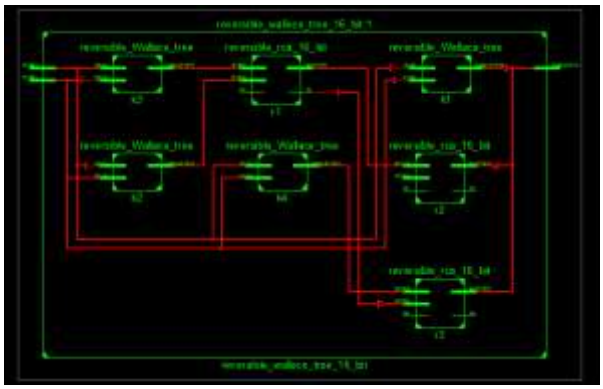


Fig 12 RTL of 16- bit Multiplier using Reversible logic

Fig 13. Output waveform of 16- bit Multiplier using Reversible logic

7.CONLUSION

The performance of digital circuits can be enhanced using reversible gates and have compared 4-bit ripple carry reversible adder with an irreversible adder in terms of speed and power; thereby concluding that reversible designs are faster and power efficient. Furthermore, this concept is extended to combinational circuits such as a Wallace tree multiplier using reversible gates, which were simulated and respective results validate prior inferences. Then a reversible sequential control unit of a GCD processor was designed. Thus, all the designs implemented were compared with their irreversible counterparts, and the speed and power parameters for the reversible designs were observed to have improved significantly.

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