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A Study ofModified Three-Phase Four-Wire UPQC Topology

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ABSTRACT: The unified power quality conditioner (UPQC) is a custom power device, which mitigatesvoltage and current-related PQ issues in the power distribution systems. In this paper, a UPQC topologyfor applications with non-stiff source is proposed. The proposed topology enables UPQC to have areduced dc-link voltage without compromising its compensation capability. This proposed topology alsohelps to match the dc-link voltage requirement of the shunt and series active filters of the UPQC. Thetopology uses a capacitor in series with the interfacing inductor of the shunt active filter, and the systemneutral is connected to the negative terminal of the dc-link voltage to avoid the requirement of the fourthleg in the voltage source inverter (VSI) of the shunt active filter. The average switching frequency of theswitches in the VSI also reduces; consequently the switching losses in the inverters reduce. Detaileddesign aspects of the series capacitor and VSI parameters have been discussed in the paper.

KEYWORDS-Average switching frequency, dc-link voltage, hybrid topology, non-stiff source, unifiedpower quality conditioner (UPQC).

I. INTRODUCTION

Power Quality (PQ) has become an importantissue since many loads at various distribution ends likeadjustable speed drives, process industries, printers,domestic utilities, computers, microprocessor basedequipments etc. have become intolerant to voltagefluctuations, harmonic content and interruptions.Power Quality (PQ) mainly deals with issues likemaintaining a fixed voltage at the Point of CommonCoupling (PCC) for various distribution voltage levelsirrespective of voltage fluctuations, maintaining near unitypower factor power drawn from the supply, blocking ofvoltage and current unbalance from passing upwards fromvarious distribution levels, reduction of voltage and currentharmonics in the system and suppression of excessivesupply neutral current.. Unified PQ conditioner (UPQC) is aversatile custom power device which consists of twoinverters connected back-to-back and deals with both loadcurrent and supply voltage imperfections. UPQC cansimultaneously act as shunt and series active power filters.

The series part of the UPQC is known as dynamic voltagerestorer (DVR). It is used to maintain balanced, distortionfree nominal voltage at the load. The shunt part of theUPQC is known as distribution static compensator(DSTATCOM), and it is used to compensate load reactivepower, harmonics and balance the load currents therebymaking the source current balanced and distortion free withunity power factor. Voltage rating of dc-link capacitorlargely influences the compensation performance of anactive filter . In general, the dc-link voltage for the shuntactive filter has much higher value than the peak value ofthe line-to-neutral voltage. This is done in order to ensure aproper compensation at the peak of the source voltage. In,the authors mentioned about the current distortion limit andloss of control limit, which states that the dc-link voltageshould be greater than or equal to $\sqrt{6}$ times the phase voltageof the system for distortion free compensation. When the dclink voltage is less than this limit, there is insufficientresultant voltage to drive the currents through theinductances so as to track the reference currents. Theprimary condition for reactive power compensation is thatthe magnitude of reference dc-bus capacitor voltage shouldbe higher than the peak

voltage at the point of commoncoupling (PCC). Due to the aforementioned criteria, manyresearchers have used a higher value of dc capacitor voltagebased on applications. Similarly, for series active filter, thedc-link voltage is maintained at a value equal to the peak ofthe line-to-line voltage of the system for propercompensation . In case of the UPQC, the dc-link voltagerequirement for the shunt and series active filters is not thesame. Thus, it is a challenging task to have a common dclink of appropriate rating in order to achieve satisfactoryshunt and series compensation. The shunt active filterrequires higher dc-link voltage when compared to the seriesactive filter for proper compensation. In order to have aproper compensation for both series and shunt active filter,the researchers are left with no choice rather than to selectcommon dc-link voltage based on shunt active filterrequirement. This will result in over rating of the seriesactive filter as it requires less dc-link voltage compared toshunt active filter. Due to this criterion, in literature, ahigher dc link voltage based on the UPQC topology hasbeen suggested. With the high value of dc-link capacitor, thevoltage source inverters (VSIs) become bulky, and theswitches used in the VSI also need to be rated for highervalue of voltage and current. This in turn increases the entirecost and size of the VSI. To reduce the dc-link voltagestorage capacity, few attempts were made in literature. In ahybrid filter has been discussed for motor drive applications.The filter is connected in parallel with diode rectifier andtuned at seventh harmonic frequency. Although an elegantwork, the design is specific to the motor drive application,and the reactive power compensation is not considered,which is an important aspect in UPQC applications.

In caseof the three-phase four-wire system, neutral-clampedtopology is used for UPQC. This topology enables theindependent control of each leg of both the shunt and seriesinverters, but it requires capacitor voltage balancing. Infour-leg VSI topology for shunt active filter has beenproposed for three-phase four-wire system. This topologyavoids the voltage balancing of the capacitor, but theindependent control of the inverter legs is not possible. Toovercome the problems associated with the four-legtopology, in the authors proposed a T-connected transformerand three-phase VSC based DSTATCOM. However, thistopology increases the cost and bulkiness of the UPQCbecause of the presence of extra transformer. In this paper, aUPQC topology with reduced dc-link voltage is proposed.

II. PROPOSEDCONTROL STRATEGY

Fig.1 represents the equivalent circuit of the proposed VSI topology for UPQC compensated system.In this topology, the system neutral has been connected to the negative terminal of the dc bus along with thecapacitor Cf in series with the interfacing inductance of the shunt active filter. This topology is referred to asmodified topology. The passive capacitor Cf has the capability to supply a part of the reactive power required bythe load, and the active filter will compensate the balance reactive power and the harmonics present in the load.The addition of capacitor in series with the interfacing inductor of the shunt active filter will significantly reducethe dc-link voltage requirement and consequently reduces the average switching frequency of the switches.

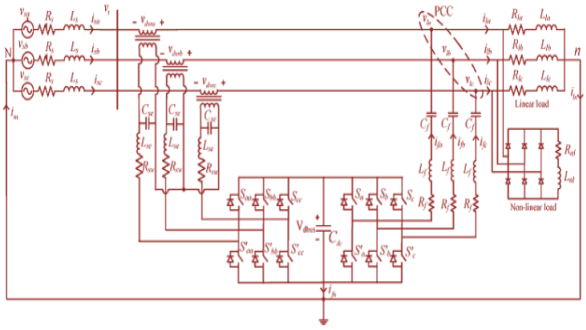

Fig. 1. Equivalent circuit of proposed VSI topology for UPQC compensated system (modified topology).

Thisconcept will be illustrated with analytic description in the following sectionthe dc-link voltage requirement of the shunt active filter enables us to the match the dc-link voltage requirementwith the series active filter. This topology avoids the over rating of the series active filter of the UPQCcompensation system. The design of the series capacitor Cf and the other VSI parameters have significant effecton the performance of the compensator. These are given in the next section. This topology uses a single dccapacitor unlike the neutral-clamped topology and consequently avoids the need of balancing the dc-linkvoltages. Each leg of

the inverter can be controlled independently in shunt active filter. Unlike the topologies mentioned in the literature, this topology does not require the fourth leg in the shunt activefilter for three-phase four-wire system.

A. Design of VSI parameters

The parameters of the VSI need to be designed carefully for better tracking performance. Theimportant parameters that need to be taken into consideration while designing conventional VSI are Vdc, Cdc, Lf ,Lse, Cse, and switching frequency (fsw). The design details of the VSI parameters for the shunt and series activefilter are given.

Design of Shunt Active Filter VSI Parameters: Consider the active filter is connected to an XkVA system and deals with 0.5X kVA and 2X kVA handlingcapability under transient conditions for n cycles. During transient, with an increase in system kVA load, thevoltage across each dc-link capacitor (Vdc) decreases and vice versa.

Design of Series Active Filter VSI Parameters: In order to make the series active filter system a first-order system, a resistor is added in series with thefilter capacitor, referred as switching band resistor (Rsw).The rms value of the capacitor current can be expressed as Ise =√ (I^2inv− I^2l). Iinv is the series inverter currentrating and Il is the load current. The capacitor branch current is divided into two components—a fundamentalcurrent Ise1, corresponding to the fundamental reference voltage (Vref1) and a switching frequency current Isw,corresponding to the band voltage (Vsw).

A design example is illustrated for a rated voltage of 230V line to neutral and the dc-link voltagereference (Vdcref) of the conventional VSI topology has been taken as 1.6 Vm for each capacitor. Thehysteresis band (h1) is taken as 0.5 A. From (5), the interfacing inductance (Lf) is computed to be 26mH. Thebase kVA rating of the system is taken as 5 kVA. Using (3), Cdc is computed and found to be 2200 F. The ratedseries VSI voltage is chosen as 50% of the rated voltage, i.e., the maximun injection capacity of the series activefilter is 115 V. The hysteresis band (h2) for series active filter is taken as 3% of the rated voltage, i.e., 6.9 V. Themaximum switching frequency of the IGBT-based inverter is taken as 10 kHz. The series active filter currentrating is choosen as 8 A and the rated load current as 7 A. Using the (7)–(9), the filter capaciotr Cse, the bandresistor Rsw and interfacing inductance Lse are calculated to be 80μF, 1.5 Ω, and 5mH, respectively. The systemparameters are given in Table I for the conventional VSI topology.

Design of Cf for the Proposed VSI Topology: The design of the Cf depends upon the value to which the dc-link voltage is reduced. In general, loads withonly nonlinear components of currents are very rare, and most of the electrical loads are combination of thelinear inductive and nonlinear loads. Under these conditions, the proposed topology will work efficiently. Thedesign of the value of Cf is carried out at the maximum load current, i.e., with the minimum load impedance toensure that the designed Cf will perform satisfactorily at all other loading conditions. If Smax is the maximumkVA rating of a system and V_{base} is the base voltage of the system, then the minimum impedance in the system.

In the modified topology along with the series capacitor in the shunt active filter, the system neutral isconnected to the negative terminal of the dc bus capacitor. This will introduce a positive dc voltage componentin the inverter output voltage. This is because, when the top switch is ―ON, +Vdbus appears at the inverteroutput, and 0 V appears when the bottom switch is ―ON. Thus, the inverter output voltage will have dc voltagecomponent along with the ac voltage. The dc voltage is blocked by the series capacitor, and thus the voltageacross the series capacitor will be having two components, one is the ac component, which will be in phaseopposition to the PCC voltage, and the other is the dc component. Whereas, in case of the conventionaltopology, the inverter output voltage varies between +Vdc when top switch is ―ON and −Vdc when the bottomswitch ―ON. Similarly, when a four-leg topology is used for shunt active filter with a single dc capacitor, theinverter output voltage varies between +Vdbus and −Vdbus. Therefore, these topologies does not contain any dccomponent in the inverter output voltage.

III. GENERATION OF REFERENCE COMPENSATORCURRENTS

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In this work, the load currents are unbalanced anddistorted, these currents flow through the feeder impedanceand make the voltage at terminal unbalanced and distorted.The series active filter makes the voltages at PCC balancedand sinusoidal. However, the voltages still contain switchingfrequency components and they contain some distortions. Ifthese terminal voltages are used for generating the shuntfilter current references, the shunt algorithm results inerroneous compensation. To remove this limitation of thealgorithm, fundamental positive sequence voltages v+la1(t),v+lb1(t), and v+lc1(t) of the PCC voltages are extractedand are used in control algorithm for shunt active filter. Theexpressions for reference compensator currents are given. In this equation, Plavg is the average load power,Ploss denotes the switching losses and ohmic losses inactual compensator, and it is generated using a capacitorvoltage ANN controller.

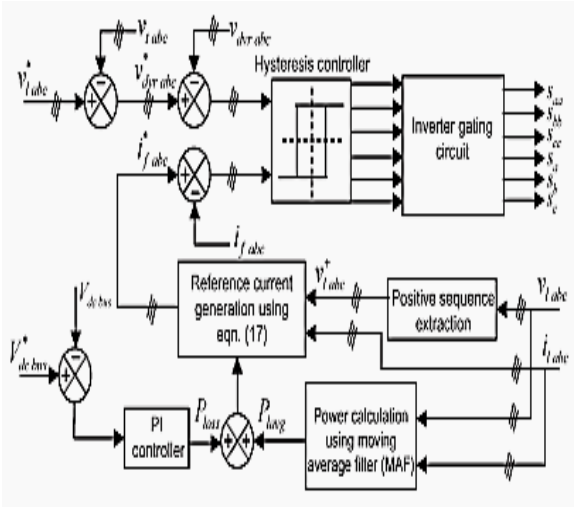

Fig. 2. Control block diagram for UPQC.

IV. SIMULATION AND EXPERIMENTAL RESULTS

In order to validate the proposed topology,simulation is carried out using MATLAB. The same systemparameters which are given Table I with additional Cf for adesired dc-link voltage are used to carry out simulationstudies. The simulation results for both the conventionaltopology and the proposed modified topology are presentedin this section for better understanding and comparisonbetween both the topologies.

Table I System parameters

System Quantities	Values
System voltages	230 V (line to neutral), 50 Hz
Feeder impedance	$Z_s = 1 + j3.141\ \Omega$
Linear Load	$Z_{la} = 34 + j47.5\ \Omega$, $Z_{lb} = 81 + j39.6\ \Omega$, $Z_{lc} = 31.5 + j70.9\ \Omega$
Non-linear Load	three-phase full bridge rectifier load feeding a R-L load of 150 Ω-300 mH
Shunt VSI parameters	$C_{dc} = 2200\ \mu F$, $L_f = 26$ mH, $R_f = 1\ \Omega$ $V_{dbus} = 2 \times V_{dc} = 1040$ V (Conventional), $V_{dbus} = 560$ V(Proposed)
Series VSI parameters	C_{se}=80 μF, L_{se}= 5 mH $R_{sw} = 1.5\ \Omega$
Series interfacing transformer	1:1, 100 V and 700 VA
PI controller gains	$K_p = 6$, $K_i = 5.5$
Hysteresis band	$h_1 = \pm 0.5$ A, $h_2 = \pm 6.9$ V

V. CONCLUSION

A modified UPQC topology for three-phase four-wiresystem using ANN controller has been suggested in thispaper, which has the proficiency to compensate the load at alower dc-link voltage under non stiff source. Design of thefilter parameters for the series and shunt active filters isexplained in detail. The proposed method is validatedthrough simulation and experimental studies in a threephase distribution system with neutral-clamped UPQCtopology (conventional). The proposed modified topologygives the advantages of both the conventional neutralclamped topology and the four-leg topology.

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