International Journal of Research
Available at https://edupediapublications.org/journals
p-ISSN: 2348-6848
e-ISSN: 2348-795X
Volume 03 Issue 14
October 2016

A Novel Efficient Distributed Arithmetic &Finite Impulse Response on Look-up-table

Vontikommu Bhargavi[1] & Mrs.Pabbaraju Padmaja[2]

[1]M-Tech Dept of ECE, Khammam Institute Of Technology & Sciences, Khammam

[2]Associate Professor, Dept of ECE, Khammam Institute of Technology & Sciences, Khammam

ABSTRACT

In this paper, critical path of multiple constant multiplication (MCM) blocks is analyzed precisely and optimized for high-speed and low-intricacy implementation. A delay model predicated on signal propagation path is proposed for more precise estimation of critical path delay of MCM blocks than the conventional adder depth and the number of cascaded full adders. A dual objective configuration optimization (DOCO) algorithm is developed to optimize the shift-integrate network configuration to derive high-speed and low-intricacy implementation of the MCM block for a given fundamental set along with a corresponding adscititious fundamental set. A genetic algorithm (GA)-predicated technique is further proposed to probe for optimum supplemental fundamentals. In the evolution process of GA, the DOCO is applied to each probed adscititious fundamental set to optimize the configuration of the corresponding shift-integrate network. Experimental results show that the proposed GA-predicated technique reduces the critical path delay,Area, power consumption, area delay product and power delay product by 32.8%, 4.2%, 5.8%, 38.3%, and 41.0%, respectively, over other subsisting optimization methods.

Keywords: Efficient Distributed Arithmetic (DA), Finite Impulse Response (FIR), Look-up-table (LUT).

1. INTRODUCTION

Finite impulse replication (FIR) filters are of great paramountcy in digital signal processing (DSP) systems since their characteristics in linear-phase and victual-forward implementations make them very utilizable for building stable high-performance filters. Albeit both architectures have kindred intricacy in hardware, the transposed form is generally preferred because of its higher performance and power efficiency. The multiplier block of the digital FIR filter in its transposed where the multiplication of filter coefficients with the filter input is realized, has consequential impact on the intricacy and performance of the design because a sizably voluminous number of constant multiplications are required. That is often often called the multiple constant

multiplications (MCM) operation and can be a consequential operation and performance bottleneck in many other DSP programs equipollent to expeditious Fourier transforms, discrete cosine transforms (DCTs), and blunder redressing codes. Even though field-, delay-, and energy-efficient multiplier architectures, corresponding to Wallace and modified sales space multipliers, had been proposed, the whole flexibility of a multiplier is just not imperative for the steady multiplications, given that filter coefficients are fine-tuned and determined beforehand by the DSP algorithms. Hence, the multiplication of filter coefficients with the input data is generally implemented under a shift integration architecture where each constant multiplication is realized utilizing integration/subtraction and shift operations in an MCM operation For the shift-integrates implementation of constant multiplications, a straightforward method, generally kenned as digit predicated run at the gate level. In this paper, we initially determine the gate-level implementation costs of digit-serial additament, subtraction, and left shift operations utilized in the shift integrates design of digit-serial MCM operations. Then, we introduce the exact CSE algorithm that formalizes the gate-level area optimization quandary as a 0–1 integer linear programming (ILP) quandary when constants are defined under a particular number representation. We additionally present an incipient optimization model that reduces the 0–1 ILP quandary size significantly and, consequently, the runtime of a generic 0–1 ILP solver. Since there are still instances which the exact CSE algorithm cannot handle, we describe the approximate GB algorithm that iteratively finds the “best” partial product which leads to the optimal area in digit-serial MCM design at the gate level. The CSE technique primarily searches for the most frequently occurred mundane sub expressions which could be maximally shared across the multipliers in the MCM block. Potkonjak et al. and Hartley pioneers to explore the redundancy in MCM blocks utilizing CSE technique. Potkonjak et al. represented coefficients in signed digit (SD) form and utilized a recursive bipartite matching algorithm to identify the maximally-shared mundane subexpressions. Hartley expressed the coefficients in canonical signed digit (CSD) form and arranged them in a two-dimensional array to probe for identical bit patterns in horizontal (intra-coefficient), vertical and oblique (inter-coefficient) directions. Thereafter, more CSE algorithms with different mundane subexpression identification strategies are proposed to

reduce the logical operators (LOs) and logic depth (LD). However, the disadvantage of CSE algorithms is that the performance of these algorithms depends on the number representation. The conception of representing multiplier blocks with directed acyclic graphs (DAGs) was introduced. vertices (or nodes) in the graph correspond to additaments. Values assigned to vertices representing the results of additaments are referred to as fundamentals. Edges in the graph correspond to shift operations, i.e., multiplications by a potency-of-two term. Minimized adder graph (MAG) for single constant multiplications are engendered by an exhaustive search of all possible graph topologies and further utilized in the heuristic part of -dimensional reduced adder graph (RAG-) algorithm However, due to the high computation intricacy of exhaustive search, the MAG lookup table (LUT) utilized in RAG- contains constants only up to 12-bit. Thereafter, several heuristic algorithms with different supplemental fundamental cull strategies have been proposed to surmount the circumscription of the MAG LUT. The GD algorithms share the same optimal part and use different criteria to determine adscititious fundamentals. While the earlier GD algorithms fixate on reducing the number of supplemental fundamentals (i.e., word-level adders), in some recent works , the bit-level information of word-level adders has been taken into consideration to minimize the number of full adders.

2. RELATED WORK

Subsisting System

Multiple constant multiplications (MCM) Constitutes a typical fine-tuned-point arithmetic operation in digital signal Processing. It is the focus of a plethora of research on high-speed and low power contrivances in communication systems and signal processing systems. In multiplier less MCM, multipliers are superseded by simpler components such as adders and hard-wired shifts (adders in our paper include withal sub tractors as their hardware costs are kindred). By utilizing the Negative digits (sub rector in circuit) in their signed digit Representations, coefficients may be synthesized with fewer adders; ergo the area and power Consumption of the circuit can be reduced. An example of a multiplier-predicated and a multiplier less predicated MCM implementations respectively, wherein 4 multiplications are superseded by 6 adders and 6 hardwired shifts. Such Multiplier less MCMs are utilized, for example, in the design of finite-impulse replication Filters.

Proposed system

The optimization of gate-level area quandary in digit-serial MCM design is an NP-consummate quandary due to the NP-plenariness of the MCM quandary. Thus, naturally, there will be always 0–1 ILP quandaries engendered by the exact CSE algorithm that current 0–1 ILP solvers find arduous to handle. Hence, the GB heuristic algorithms, which obtain a good solution utilizing less computational resources, are indispensable. In our approximate algorithm called MINAS-DS, as done in algorithms designed for the MCM quandary given in Definition 1, we find the fewest number of intermediate constants such that all the target and intermediate constants are synthesized utilizing a single operation. However, while culling an intermediate constant for the implementation of the not yet synthesized target constants in each iteration, we favor the one among the possible intermediate constants that can be synthesized utilizing the least hardware and will enable us to implement the not-yet synthesized target constants in a more minute area with the available constants. After the set of target and intermediate constants that realizes the MCM operation is found, each constant is synthesized utilizing an A-operation that yields the minimum area in the digit-serial MCM design. The area of the digit-serial MCM operation is resolute as the total gate-level implementation cost of each digit-serial advisement, subtraction, and shift operation under the digit size parameter d as described in Section II-D. The preprocessing phase of the algorithm is equipollent to that of the exact CSE algorithm, and its main part and routines are given. The right shift of an A-operation is postulated to be zero

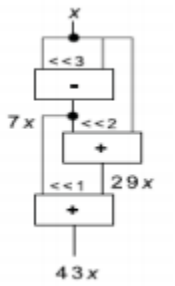

Fig:-1 Project Flow

3. IMPLEMENTATION

While the area intricacy is estimated at bit-level, the CPD in our paper is estimated predicated on the signal propagation path, because in a 1-bit full adder, the delays for different paths may be different. For this reason, a fine-grained signal propagation path predicated delay model is proposed for the analysis of critical path of MCM blocks. Thereafter, a shift-integrate network configuration optimization scheme is developed for reducing CPD as well as hardware intricacy.

Signal Propagation Path Predicated Critical Path Analysis:

In the bit-level delay model proposed in the computation time of the sum and carry-out of a full adder is surmised to be identically tantamount. However, a more proximate optically canvass the full adder reveals that this is not the true case in authentic digital circuits. Let us take the full adder in as an example. From the implementation perspective of a full adder, the input signals from and to the outputs and peregrinate through different paths. This results different intrinsic delays for different signal paths. Furthermore, the loads driven by the outputs of a full adder impact the delays as well. Thus, in lieu of postulating the computation time of the sum and carry out to be equipollent, we treat the delays of different signal paths in a full/half adder individually. Predicated on the input-output path delay information the propagation delay of each path in the MCM block is estimated by integrating all the delay components along the signal path. Which shows the integration of three 4-bit numbers, and Ripple carry adder (RCA) is utilized in most of the works for the implementation of MCM blocks due to their conventional implementation pattern. Thus, it is additionally considered to implement MCM blocks throughout this work. (However, the conception of signal propagation path predicated critical path analysis studied in this work can be applied to other adder structures) Six bits are needed to represent the result of this integration and sign extensions.

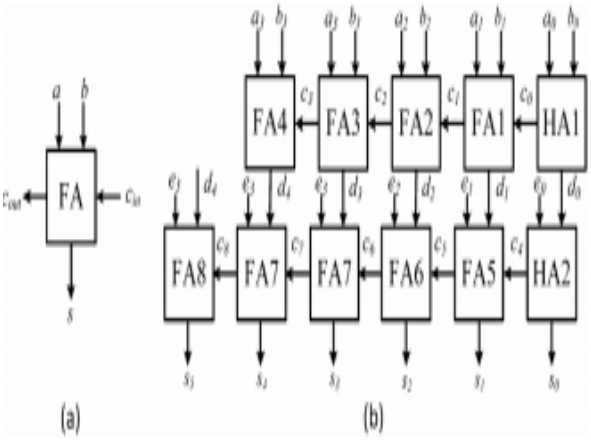

Fig:-2 Full adder &two consecutive additions

Optimization of Shift-Add Network Configuration for Reduction of CPD:

For a given fundamental set and a corresponding supplemental fundamental set, different configurations of the shift-integrate network result in not only different hardware intricacy as shown in Section II-C, but additionally different CPD. Let us take the same four different implementations of the multiplication of a 8-bit input with the coefficient set {3, 13} in as an example. Utilizing the delay information in Table I, the CPD for scenarios (a), (b), (c), and (d) are estimated to be 13.2 u.t., 12.2 u.t., 11.2

u.t., and 10.3 u.t., respectively. This implicatively insinuates that the configuration of a shift-integrate network could be optimized to reduce the CPD. The following shift-integrate network configuration optimization algorithm, designated avaricious reduced critical path delay configuration (GRCPDC) algorithm, is proposed to optimize the con- figuration of the shift-integrate network for reducing the CPD.

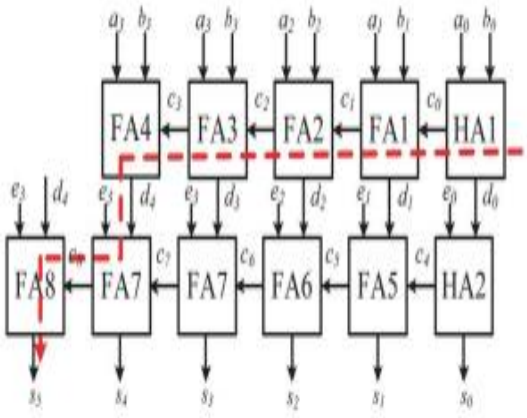

Fig:-3 Critical path of two consecutive additions

1) During the construction of the DAG, each time only one fundamental (no matter if it is a given or additional fundamental) which results in the lowest CPD among all the fundamentals that can be obtained from the previously realized fundamentals is realized. If there are more than one fundamental that result in the same lowest CPD, the fundamental with the smallest value is selected.

2) Repeat step 1 until all fundamentals have been realized.

Reduction of CPD and Hardware Intricacy:

In this section, a dual-objective configuration optimization (DOCO) algorithm is proposed to optimize both CPD and of the MCM block for a given fundamental set with a corresponding adscititious fundamental set. The proposed DOCO algorithm is a hybrid algorithm predicated on three rudimentary cupidinous optimization techniques: GRCPDC, RFA and the optimal part of RAG- , referred to as ORAG- . Here, GRCPDC engenders MCM blocks with lowest CPD .While RFA and ORAG fixate on reducing and the number of adders, respectively. The key conception of DOCO is to reduce the of GRCPDC without incrementing CPD by introducing solutions of RFA and ORAG- . Let be the given fundamental set and be the corresponding supplemental fundamental set

The DOCO algorithm is described as follows:

1) Apply GRCPDC, RFA, and ORAG- on and get three different shifts-integrate networks. For each shift-integrate network, record the shift-integrate configuration of each coefficient of.

2) Merge the configuration recordings of the three shifts-integrate networks. If there are

identical configurations for the same coefficient, keep one and abstract the others. Compute the number of full adders needed for each configuration.

3) Solve the coalescence quandary of culling one configuration for each coefficient of from the merged configuration set. If the amalgamation number is less than , go to step 4. Otherwise, go to step 5. The size of the coalescence quandary increase exponentially with the number of coefficients. Thus, the algorithm uses as a threshold to determine either optimal (step 4) or heuristic (step 5–7) method to be utilized in the following steps. The default value of in our design is 25 000.

4) Traverse through all the cumulations and test to find if for every cumulation there subsists a feasible solution. If affirmative, compute the of this solution. Cull the coalescence with the most diminutive and terminate the optimization.

5) Utilize the shift-integrate network engendered by GRCPDC as a base solution and compute its . For each coefficient, abstract the configurations in the merged configuration set that need more number of full adders than the corresponding configuration in the base solution.

6) For each fundamental, cull one configuration from the merged configuration set to supersede the configuration in the base solution and engender an incipient solution. Test the newsolution: if the incipient solution is a feasible one and its is more minuscule than the base solution, update the base solution with the incipient solution and expunge the configuration in the merged configuration set; otherwise, keep the pristine base solution

7) Reiterate step 6 until no configuration left in the merged con- figuration set.

In DOCO, two different optimization strategies are utilized according to the size of the amalgamation quandary. In step 4, when the combnation quandary size is less than , exhaustive search is utilized to test all potential solutions to get an optimal solution while steps 5–7 start with a base solution of GRCPDC and amend it gradually with cupidinous supersession. is utilized as a threshold to determine which strategy to utilize. In the rest of the paper, we utilize DOCO to represent the value of the shift-integrate network of after DOCO optimization.

4. EXPERIMENTAL RESULTS

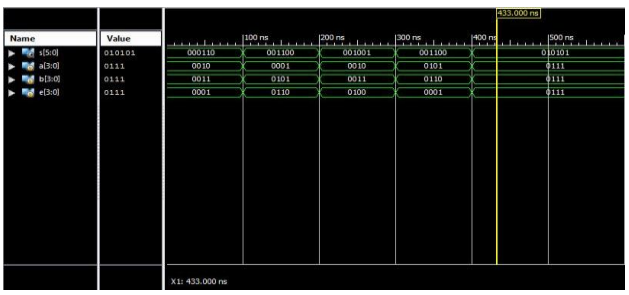

Fig: - 4 Simulation result

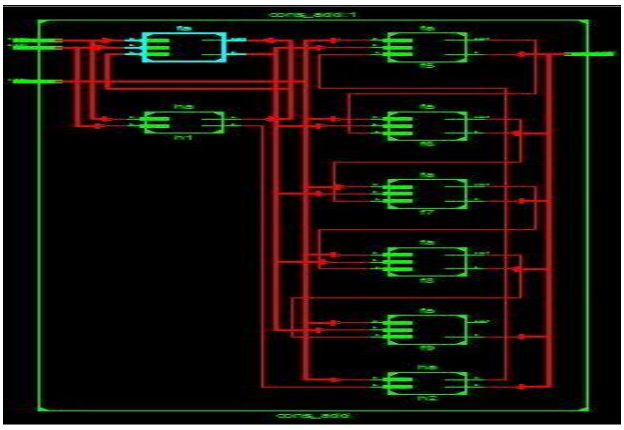

Fig: - 5 Synthesis results

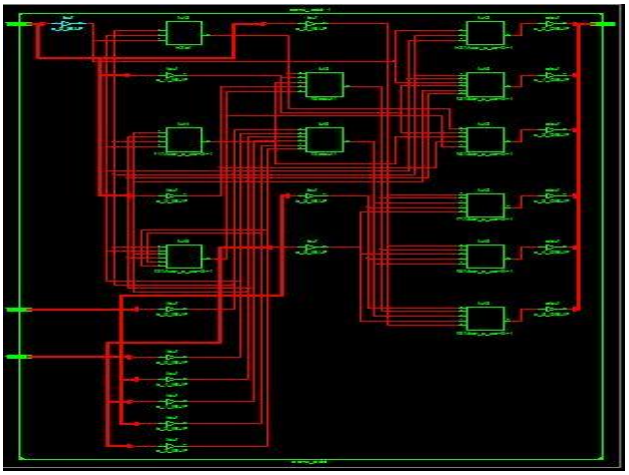

Fig: - 6 TTL schematic diagram

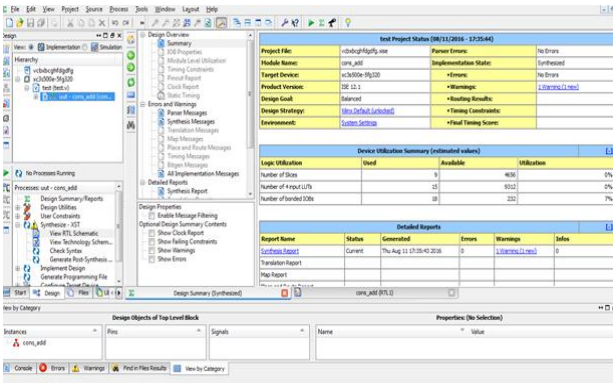

Fig:- 7 Design summary

5. CONCLUSION

In this project, the critical path of MCM blocks are analyzed predicated on the signal path and a fine grained delay model for CPD estimation is proposed. Predicated on this precise estimate of path, we proposed an algorithm designated DOCO to optimize the shift-integrate network configuration of MCM blocks for the reduction of CPD and hardware intricacy subject to a supplemental fundamental set. In this order to find the optimum supplemental fundamentals for a given fundamental set, a GA-predicated search method is proposed. The DOCO algorithm is adopted in the proposed GA-predicated technique to optimize the shift integrate network configurations. Experimental results show that solutions engendered by the proposed GAbased technique outperform subsisting algorithms in terms of CPD, area, power consumption, ADP and PDP. The CPD, area, potency, ADP, and PDP are reduced by 32.8%, 4.2%, 5.8%, 38.3%, and 41.0%, respectively, in average over the subsisting algorithms.

6. REFERENCES

[1] Y. Voronenko and M. Püschel, "Multiplierlessmultiple constant multiplication," ACM Trans.Algorithms, vol. 3, no. 2, p. 11, Sep. 2007.

[2] R. Pasko, P. Schaumont, V. Derudder, S.Vernalde, and D. Durackova, "A new algorithm for

elimination of common subexpressions," IEEE Trans.Comput.-Aided Design Integr. Circuit Syst., vol. 18,no. 1, pp. 58–68, Jan. 1999.

[3] M. M. Peiro, E. I. Boemo, and L. Wanhammar,"Design of high-speed multiplierless filters using anonrecursive signed common subexpressionalgorithm," IEEE Trans. Circuits Syst. II, AnalogDigit. Signal Process., vol. 49, no. 3, pp. 196–203,Mar. 2002.

[4] F. Xu, C. H. Chang, and C. C. Jong, "Contentionresolution algorithm for common subexpressionelimination in digital filter design," IEEE Trans.Circuits Syst. II, Exp. Briefs, vol. 52, no. 10, pp.695–700, Oct. 2005.

[5] F. Xu, C. H. Chang, and C. C. Jong, "Contentionresolution algorithm for common subexpressionelimination in digital filter design," IEEE Trans.Circuits Syst. II, Exp. Briefs, vol. 52, no. 10, pp.695–700, Oct. 2005.

[6] O. Gustafsson and L. Wanhammar, "Ilpmodelling of the common subexpression sharing
problem," in Proc. IEEE 9th Int. Conf. Electron.,Circuits Syst., Sep. 2002, vol. 3, pp. 1171–1174.

[7] A. Yurdakul and G. Dundar, "Multiplierlessrealization of linear DSP transforms by using
common two-term expressions," J. VLSI SignalProcess., vol. 22, pp. 163–172, Sep. 1999.

[8] L. Aksoy, E. da Costa, P. Flores, and J. Monteiro,"Exact and approximate algorithms for the
optimization of area and delay in multiple constantmultiplications," IEEE Trans. Comput.-Aided DesignIntegr. Circuit Syst., vol. 27, no. 6, pp. 1013–1026,Jan. 2008.

Authors Profile

VONTIKOMMU BHARGAVI, completed B-Tech in Khammam Institute Of Technology And Sciences located in khammam in 2014 with the branch Electronics and Communication Engineering (ECE) with 76% of marks. Now persuing M-Tech in Khammam Institute Of Technology And Sciences,Khammam with Very Large Scale Integration System Design(VLSISD)

Mrs. PABBARAJU PADMAJA completed her M-Tech with the branch Electronics and Communication Engineering(ECE) from JNTU, Hyderabad and Presently working as Associate Professor in Khammam Institute Of Technology And Sciences, Khammam