International Journal of Research
Available at https://edupediapublications.org/journals
p-ISSN: 2348-6848
e-ISSN: 2348-795X
Volume 03 Issue 14
October 2016

An Processors With High speed OFDM & FFT size greater than 512 points with Low power consumption standards

Vagaboina Jyothi [1], Ms. V.Krupa Devi[2] & Mr. Kothapalli Saidulu[3]

[1]M-Tech Dept of ECE, Bomma Institute of Technology and Science, Khammam.

[2]Associate Professor, Dept of ECE, Bomma Institute of Technology and Science, Khammam.

[3]HOD, Associate professor, Dept of ECE, Bomma Institute of Technology and Science, Khammam.

Abstract

This paper proposes a shared multiplier scheduling scheme (SMSS) for area-efficient expeditious Fourier transform (FFT)/ inverse FFT processors. SMSS can significantly reduce the total number of involute multipliers up to 28%. The proposed commixed-radix multipath delay commutator processors can fortify 128/256 and 256/512-point FFTs utilizing SMSS. The proposed processors have been designed and implemented with 90-nm CMOS technology, which can reduce the total hardware intricacy by 20%. The proposed processors having eight-parallel data paths can achieve a high throughput rate up to 27.5 GS/s at 430 MHz. In integration, the proposed processors can fortify any FFT size utilizing adscititious stages. Lesser delay With High speed & Low power consumption

Keywords:- FFT (Fast Fourier Transform), reconfigurable FFT, Vedic multiplier, MRMDC (mixed radix multipath delay Commutator), OFDM (Orthogonal Frequency Division Multiplexing).

1. INTRODUCTION

ORTHOGONAL frequency-divisionmultiplexing (OFDM) has emerged as the leading modulation technology for wireless and wireline communications and has been incorporated into many communication standards, such as IEEE 802.11n/ac/ad, IEEE 802.15.3.c, IEEE 802.16e , DAB , DVB-T/H , ultrawideband (UWB) , and optical OFDM (O-OFDM). High-speed OFDM systems, such as wireless personal area networks (WPANs), ecumenical interoperability for microwave access, UWB, and O-OFDM require a high-speed expeditious Fourier transform (FFT) and its inverse FFT (IFFT) implementation to meet perpetuating demands for higher data rates. In additament, the FFT computation of authentic input samples has been researched, which capitalizes on the symmetry property of FFT to reduce the

computational involution for medical applications, such as electrocardiography or electroencephalography OFDM transceivers involve FFT computation; however, implementing low-power and high-speed FFT processors is one of the most arduous tasks in the entelechy of OFDM modems, as its hardware is intricate. Consequently, sundry FFT processors have been proposed to meet authentic-time processing requisites and to reduce the hardware involution . To achieve a more minute area, recollection-predicated architectures have been proposed. In additament, application-concrete injuctive authorization-set processors have additionally been proposed to meet the flexibility for FFT computation. However, they cannot meet the highspeed requisites. By employing SMSS that can reduce the number of involute multipliers by moving the multipliers from the second stage to the first stage for 128/256-point FFT/IFFT architecture, the proposed FFT/IFFT processors decrease the hardware involution when compared with the subsisting MRMDC. In integration, the processor can achieve a high throughput utilizing eight-parallel data paths. Consequently, the proposed Type III architecture can be utilized for the high-speed FFT applications. Along with the 128/256-point processor, we withal propose a 256/512-point FFT processor utilizing SMSS to meet the requisites of 802.11ad and IEEE 802.15.3.c.

2. RELETED WORK

we show the subsisting 128/256-point MRMDC FFT/IFFT processor to derive kenned FFT architectures in general. shows the eight-parallel 128/256-point FFT/IFFT architecture, which consists of BUs, delay commutators, and twiddle factor multipliers. The input sequence of the ith OFDM symbol is split in eight-parallel data paths, where j stands for the OFDM symbol index. In the first stage, the radix-2/4 BU can perform one radix-4 or two radix-2 operations to compute the 128- and 256-point FFTs. The second and third stages employ a modified radix-8 BU proposed in which is opportune for the pipelined structure.

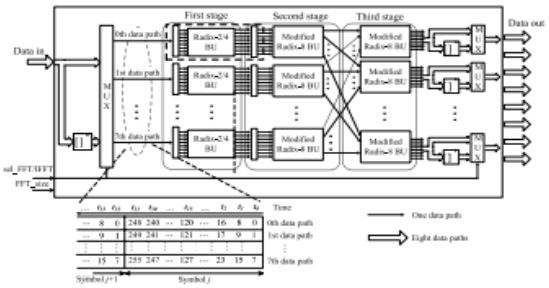


Fig:- 1 Eight-parallel 128/256-point MRMDC FFT/IFFT processor

The operation of the FFT or IFFT is culled by the control signal, sel_FFT/IFFT. To perform the IFFT computation, the designations of the imaginary components in the input and output sequences are

transmuted utilizing intricate conjugate operations

3. IMPLEMENTATION

First Stage for 256-Point FFT:

Even though Rabiner and Gold did not show the MRMDC architecture, the architecture shown in Fig. 2 can be inferred from the MDC architecture. Fig. 2 shows the first and second stages of the subsisting 256-point MRMDC architecture,which are represented by the dotted box shown in Fig. 1. The first and second stages consist of the input buffer, radix- 2/4 BU, modified radix-8 BU in and commutator. The subsisting radix-8 BU in consists of seven phases and requires a long critical path because the involute multipliers are located in two phases; hence, it has the long critical path delay that is 2tmul + 3tadd, where tmul and tadd are the delays of the intricate multiplier and adder, respectively. To reduce the critical path, the modified radix-8 BU proposed in is more felicitous for efficient implementation. Reference has incorporated twiddle factors and adder tree matrices into a single phase of calculation. In the modified radix-8 BU in the first phase has 11 intricate multipliers, and the other three phases consist of adder trees, and thus, the modified radix-8 BU can have the critical path delay of tmul + 3tadd. Ergo, the modified radix-8 BU can reduce the critical path delay by tmul. The FFT/IFFT processor withal utilizes the modified radix-8 BUs utilized in to implement high-speed FFT processors. In the subsisting MRMDC architecture the input sequence of the zeroth data path is split into eight data streams from A to H. The four input sequences of the upper BU include streams A, C, E, and G, and those of the lower BU include streams B, D, F, and H. indexed input samples in the horizontal arrive at the same stream at different time instants, whereas input samples in the vertical arrive at the same time from different streams. All the data streams are delayed by the delay elements, Di, to maintain the felicitous cycles, where i is the size of the delay element. For the first four cycles from t0 to t3, the input stream A of the zeroth data path, x(0), x(8), x(16), and x(24), is victualed and stored in D28. The input stream B is victualed and stored in D24 for the next four cycles. Every four cycles, the input sequence is switched to the next stream. The input samples in the vertical arrived at the same time from different streams in the upper and lower Bus

First Stage for 128-Point FFT

the first stage of the subsisting 128-point MRMDC architecture, which is represented by the dotted box The processor can fortify the 128-point FFT/IFFT in a kindred manner to compute the 256-point FFT n the

subsisting MRMDC, the input sequence of the eightparallel data paths is split into eight data streams. Further, each data stream is delayed by the delay elements. The subsequences in the vertical arrived at the same time from different streams in the upper and lower Bus where m is 0 or 1. in1,u(m) and in1,l(m) are the input samples in the upper and lower BUs, respectively. In contrast to the 256-point FFT the number of delay elements for input reordering in the 128-point FFT decreases by a moiety. To reorder the input sequences for the first stage, the subsisting structure in takes 14 cycles utilizing D2, D4, D6, D8, D10, D12, and D14 during the idle period and two cycles during the computation period when the FFT size is 128. Consequently, the first stage of the subsisting processor requires 16 cycles. This section proposes novel eight-parallel MRMDC FFT/IFFT processors that offer a high throughput and low hardware involution utilizing SMSS. In contrast with the subsisting processor, the first stage utilizes the shared multipliers and the second stage requires the modified radix-8 BUs without intricate multipliers (w/o mul),

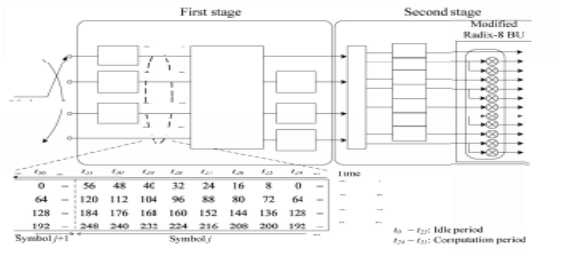
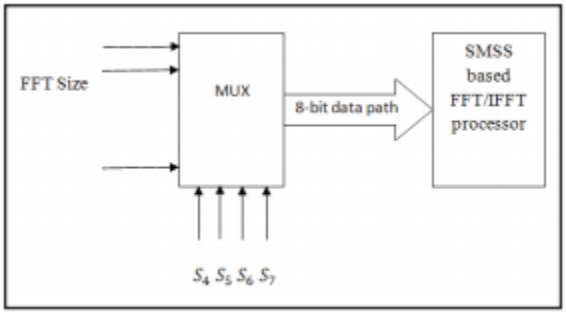


Fig:-2 256 point fft processor

VLSI Architecture of SMSS for Reconfigurable FFT/ IFFT Processor

The subsisting SMSS predicated FFT/IFFT processor [9] can fortify 128/256 point FFT size at a time only. Variable size FFT processor is required to fortify multiple FFT sizes. Reconfigurable FFT/ IFFT processor provides such a flexibility of culling any FFT sizes on single processor design without going to each FFT size processor. The subsisting work can be elongated to fortify sundry FFT sizes (2, 4, 8, 16, 32, 64, 128 and 256) lengths utilizing reconfigurable FFT processor. The reconfigurable feature is integrated to the subsisting categorical size FFT processor utilizing multiplexer as



The re-configurability for the SMSS predicated FFT/IFFT processor reduces the hardware intricacy. The multipliers utilized in the SMSS predicated FFT/IFFT processors are superseded with Vedic multipliers, so as to ameliorate performance .Vedic multipliers follows antediluvian set of rules, so that the multiplication operations

are efficient in time. Vedic multipliers [10] are predicated on sixteen sutras. Of these URDHVA TRIYAKBHYAM (vertically and crosswise) is sutra that fortifies all types of multiplications. So that the haste of calculation is further ameliorated utilizing Vedic multipliers.The implementation and synthesis report gives the performance details of proposed processor

4. EXPERMENTAL RESULTS

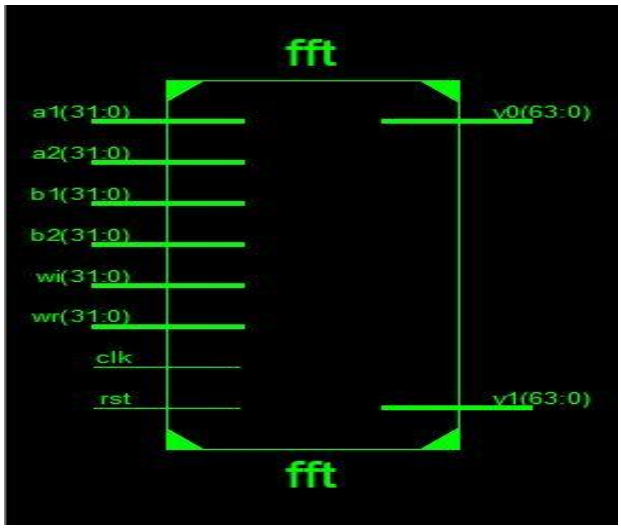


Fig:-3 Block diagram of fft

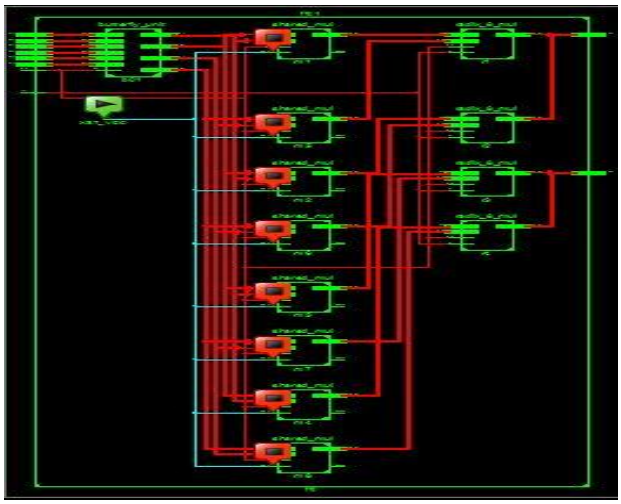


Fig:-4 RTL Results

Fig:-5 simulation result for fft

5. CONCLUSION

This paper proposed high speed and low hardware intricacy SMSS predicated reconfigurable FFT/IFFT processor. The reconfigurable FFT processor can reduce the hardware involution when compared with the subsisting 256-point SMSS predicated FFT processor. The proposed Vedic multiplier ameliorates the computation celerity. The performance results shows that the proposed reconfigurable FFT processor gives less hardware involution i.e. area reduced by 17% and celerity is incremented by 11% with a throughput rate of 8.036GS/s. In additament the proposed architecture can apply any FFT size more preponderant than 256 point utilizing adscititious stages.

6. REFERENCES

[1] S.-J. Huang, S.-G. Chen,"A green FFT processor with 2.5- GS/s for IEEE 802.15.3c (WPANs)," In Proc. Int. Conf. Green Circuits Syst., Jun. 2010, pp. 9–13.

[2] P.-Y. Tsai, T.-H. Lee, T.-D. Chiueh,"Power-efficient continuous flow memory-based FFT processor for WiMax OFDM mode," In Proc. Int. Symp. Intell. Signal Process. commun. Syst., Dec. 2006, pp. 622–625.

[3] X. Guan, Y. Fei, H. Lin,"Hierarchical design of an application specific instruction set processor for high-throughput and scalable FFT processing," IEEE Trans. Very Large Scale Integr. (VLSI) Syst., Vol. 20, No. 3, pp. 551–563, Mar. 2012.

[4] S. He, M. Torkelson,"Designing pipeline FFT processor for OFDM (de)modulation," In Proc. Int. Symp. Signals, Syst., Electron., Sep. 1998, pp. 257–262.

[5] C.-H. Yang,T.-H.Yu, D.Markovic,"Power and area optimization of reconfigurable FFT processors:A 3Gpp-LTE example,'' IEEE Trans. Very Large Scale Integr. (VLSI) Syst., Vol. 47, No. 3, pp. 757–768, Mar. 2012.

[6] T. Cho, H. Lee,"A high-speed low-complexity modified radix- FFT processor for high rate WPAN applications," IEEE Trans. Very Large Scale Integr. (VLSI) Syst., Vol. 21, No. 1, pp. 187–191, Jan. 2013.

[7] C. Chung, S. Wang, C. Li,"Area-efficient architectural design of radix-4 pipeline fast Fourier transform processor," In Proc. Workshop Consum. Electron. Signal Process., Nov. 2004, pp. 1–4.

[8] E. J. Kim, M. H. Sunwoo,"High speed eight-parallel mixedradix FFT processor for OFDM systems," In Proc. IEEE Int. Symp. Circuits Syst., May 2011, pp. 1684–1687.

[9] Eun Ji Kum, Jea Hack Le e, Myuang Hoon Sunwoo, "Novel Shared Multiplier Scheduling Scheme for Area-Efficient FT/IFFT Processors", IEEE Trans. Very Large Scale Integr. (VLSI) Syst., Vol. 23, No.9, pp. 1689–1699, sep. 2015.

[10] Harpreet Singh Dhillon, AbhijitMitra,"A Digital Multiplier Architecture using Urdhva Tiryakbhyam Sutra of Vedic Mathematics", IIT-G , pp. 1-4, 2010.

Authors Profile

VAGABOINA JYOTHI

B-Tech in SARADA INSTITUTE OF TECHNOLIGY AND SCINCE, Khammam, and percentage is 66.19%, year of completed April 2014. M-Tech Electronics And Communication Engineering

Bomma Institute of Technology and Science (BITS), Khammam.

Mail id: chandubfa@gmail.com

MS. V.KRUPA DEVI
Experience: 2 years.
Qualification: M.Tech from JNTU, Hyderabad.
Designation: Associate Professor.
Working: V.KRUPADEVI received the B.Tech degree in Electronics andCommunication Engineering from BITS, JNTUH, KMM, TS, INDIAin2012andM.Techfrom VLSI from BITS, KMM, TS, INDIA in 2015. Presently,sheisworkingas Asst.Prof in BITS,KMM,TS,INDIA. Bomma Institute of Technology and Science (BITS), Khammam.
Email-d: krupa.vudharu@gmail.com

Mr. Kothapalli. Saidulu.
Working: Head of the Department, Associate professor ECE, Bomma Institute of Technology and Science (BITS), Khammam. He obtained B.Tech degree from REC, Warangal and M.Tech degree from JNTUH, Hyderabad. Now he is pursuing Ph.D. in Computer Science and Engineering from JNTUH, Hyderabad. His research areas include Cryptography & Network Security, Computer Networks, Unix Internals, Computer Graphics and Operating Systems.