A New Highly Efficient Three-Phase Transformer-Less Hbzvr for Grid Operating System.

Uppala Naresh
M-tech Scholar
Department of Electrical & Electronics Engineering,
Anurag College of Engineering , Aushapur(Vi),Ghatkesar(Md);
Ranga Reddy (Dt); Telangana, India.
Email:uppalanaresh214@gmail.com

Sarala Sandolu
Assistant Professor
Department of Electrical & Electronics Engineering,
Anurag College of Engineering , Aushapur(Vi),Ghatkesar(Md);
Ranga Reddy (Dt); Telangana, India.
Email:saralajcyp@gmail.com

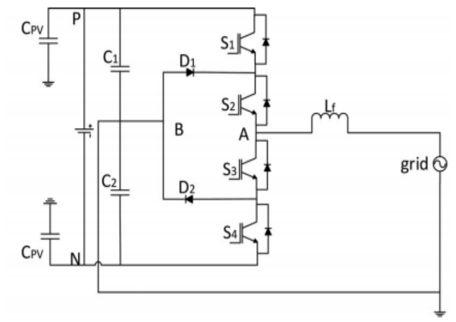
***Abstract*: ABSTRACT-Single-phase transformer less inverter is widely used in low-power grid-connected systems due to its small size, high efficiency and low cost. The galvanic isolation can be achieved via dc-decoupling or ac-decoupling, for isolation on the dc- or ac-side of the inverter, respectively. It has been shown that the latter provides lower losses due to the reduced switch count in conduction path. Common-mode voltage (CMV) appears in motor drives due to working principles of the pulse width modulation (PWM) inverters. This voltage is the main source of many unwanted problems in AC drive systems. In this Project, several recently proposed transformers less inverters with different galvanic isolation methods and CMV clamping technique are analyzed and compared. A simple modified H-bridge zero-voltage state rectifier is also proposed, to combine the benefits of the low-loss ac-decoupling method and the complete leakage current elimination of the CMV clamping method. The performances of different topologies, in terms of CMV, leakage current, total harmonic distortion, losses and efficiencies are compared. The proposed concept is further connected to three-phase system and is implemented using HBZVR concept. A safety issue is the main concern for the transformer less systems due to high leakage current. Without galvanic isolation, a direct path can be formed for the leakage current to flow from the source to the grid by In extension the proposed concept can be implemented for three-phase configuration by using MATLAB/SIMULATION software**.

Keywords: Brushless DC Motor (BLDC), Anti-windup PI Controller, Fuzzy controller, Hybrid controller, speed control, PWM inverter

I. INTRODUCTION

Today, the energy demand is increasing due to the rapid increase of the human population and fast-growing industries. Hence, renewable energy plays an important role to replace traditional natural resources such as fuel and coal. Photovoltaic (PV) energy has recently become a common interest of research because it is free, green, and inexhaustible [1]–[3]. Furthermore, PV systems are now more affordable due to government incentives, advancement of power electronics and semiconductor technology and cost reduction in PV modules [2], [3]. Generally, there are two types of grid-connected PV systems, i.e., those with transformer and without transformer. The transformer used can be high frequency (HF) transformer on the dc side or low frequency transformer on the ac side [4]. Besides stepping up the voltage, it plays an important role in safety purpose by providing galvanic isolation, and thus eliminating leakage current and avoiding dc current injection into the grid. Nevertheless, the transformers are bulky, heavy, and expensive. Even though significant size and weight reduction can be achieved with HF transformer, the use of transformer still reduces the efficiency of the entire PV system [9]. Hence, transformers less PV systems are introduced to overcome these issues. They are smaller, lighter, lower in cost, and highly efficient [4]. However, safety issue is the main concern for the transformer less PV systems due to high leakage current. Without galvanic isolation, a direct path can be formed for the leakage current to flow from the PV to the grid. At the same time, the fluctuating potential, also known as common-mode voltage (CMV), charges and discharges the stray capacitance which generates high leakage current. Besides safety issue, this leakage current increases grid current ripples, system losses, and electromagnetic interference. In order to reduce the leakage current to meet the standard in , conventional half bridge inverter or full-bridge inverter with bipolar modulation technique are used in transformer less PV systems to generate constant CMV to reduce the leakage current. However, a 700-V dc-link voltage is required for the half bridge and diode-clamped topologies. For full-bridge bipolar modulation, high losses and reduced efficiency are observed due to two-level bipolar output voltage. As a result, the voltage stress across the inductors is doubled and current ripples increase. Larger filter inductors are required, increasing the cost and size of the PV systems. Hence, many research works have been proposed recently to eliminate the leakage current via galvanic isolation and CMV clamping techniques. Galvanic isolation topologies such as H5, H6 family and HERIC introduce dc-decoupling and ac-decoupling to disconnect the PV and the grid. It is found that ac-decoupling provides lower losses due to reduced switch count in the conduction path. Nevertheless, the galvanic isolation alone cannot completely eliminate the leakage current due to the influence of switches' junction capacitances and parasitic parameters. Therefore, CMV clamping has been used in oH5, and H-bridge zero-voltage

International Journal of Research
Available at https://edupediapublications.org/journals
p-ISSN: 2348-6848
e-ISSN: 2348-795X
Volume 03 Issue 14
October 2016



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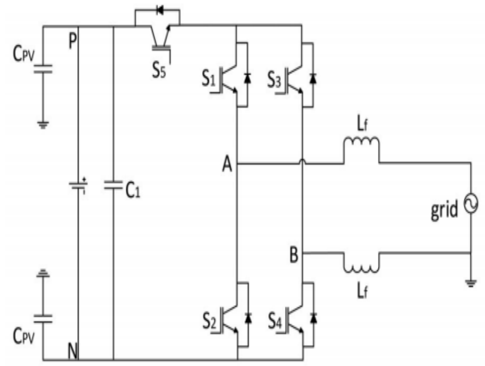

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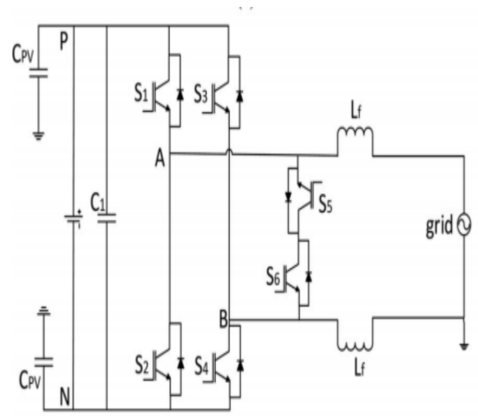

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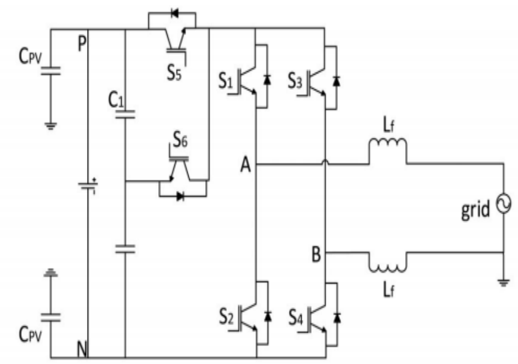

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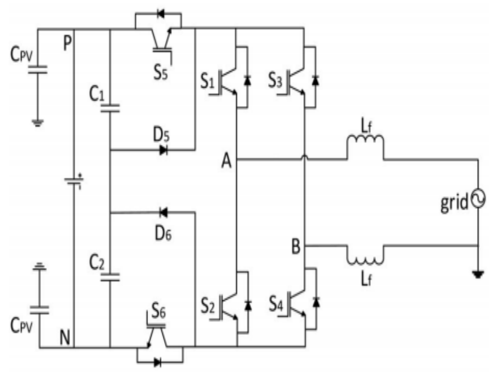

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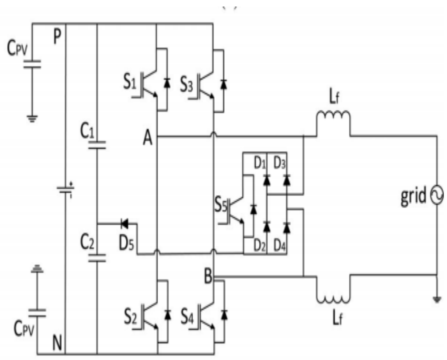


(f)

Fig. 1. Recently proposed transformer less topologies. (a) Diode-clamped topology. (b) H5 topology. (c) HERIC topology. (d) oH5 topology. (e) H6 topology. (f) HBZVR topology.

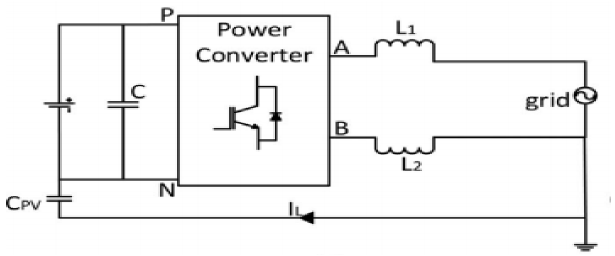
state rectifier (HBZVR), as shown in Fig. 1(d)–(f), to completely eliminate the leakage current. However, the clamping branch of HBZVR does not perform optimally. It is shown in the later section that the leakage current is as high as those of galvanic isolation topologies. In this paper, several recently proposed transformer less PV inverters with different galvanic isolation methods and CMV clamping techniques, as shown in Fig. 1, are analyzed and compared. A simple modified HBZVR-D is also proposed, to combine the benefits of the low-loss ac-decoupling method and the complete leakage current elimination of the CMV clamping method. Performance of HBZVR-D is compared to other existing topologies in terms of CMV, leakage current, total harmonic distortion (THD), losses analysis, and efficiency. Discussions are done based on MATLAB/Simulink simulations and further validated through experimental tests. It is proven that HBZVRD topology gives the best overall performance and is suitable for transformer less PV applications. This paper is organized as follows: Leakage current reduction methods via galvanic isolation and CMV clamping is discussed and analyzed in Section II. Proposed topology with its conversion structure and operation principles is presented in Section III.

p-ISSN: 2348-6848
e-ISSN: 2348-795X
Volume 03 Issue 14
October 2016

Simulation and experimental results are shown in Section IV and Section V, respectively, to validate and discuss the performance of various topologies. Finally, conclusion is made in Section VI to summarize the findings and results.

II. COMMON-MODE BEHAVIOR AND LEAKAGE CURRENT REDUCTION METHODS

When the transformer is removed from the inverter, a resonant circuit is formed as shown in Fig. 2(a). This resonant circuit includes stray capacitance (C_{PV}), the filter inductors ($L1$ and $L2$), and leakage current (I_L). Here, the power converter is represented by a block with four terminals to allow a general representation of various converter topologies. On the dc side, P and N are connected to the positive and negative rail of the dc-link, respectively; while on the ac side, terminals A and B are connected to the single-phase grid via filter inductors. From the view point of the grid, the power converter block shown



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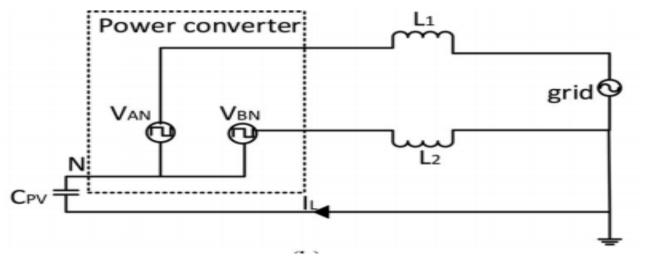

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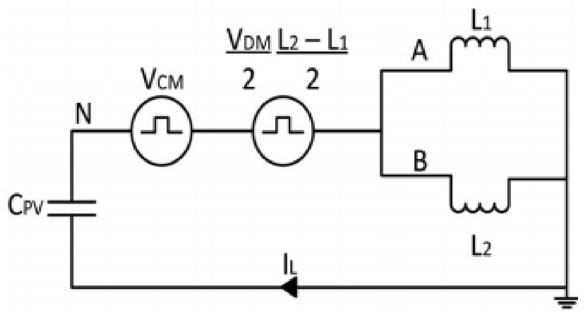

(c)

Fig. 2. Common-mode model for single-phase grid-connected inverter. (a) Full model. (b) Simplified model. (c) Simplified common-mode model.

in Fig. 2(a) can be considered as voltage sources, generating voltage V_{AN} and V_{BN} . Hence, regardless of the conversion structure, this power converter block can be simplified into the equivalent circuit which consists of V_{AN} and V_{BN} as shown in Fig. 2(b) . The leakage current is thus a function of V_{AN}, V_{BN} , grid voltage, filter inductance, and stray capacitance. The CMV V_{CM} and differential-mode voltage V_{DM} can be defined as

$$V_{CM} = \frac{V_{AN} + V_{BN}}{2} \quad (1)$$

$$V_{DM} = V_{AN} - V_{BN}. \quad (2)$$

Rearranging (1) and (2), the output voltages can be expressed in terms of V_{CM} and V_{DM} as

$$V_{AN} = V_{CM} + \frac{V_{DM}}{2} \quad (3)$$

$$V_{BN} = V_{CM} - \frac{V_{DM}}{2}. \quad (4)$$

Using (3)–(4) and considering only the common-mode components of the circuit, a simplified common-mode model can be obtained as in , following the steps in and The equivalent CMV (V_{ECM}) is defined as

$$V_{ECM} = V_{CM} + \frac{V_{DM}}{2}\frac{L2 - L1}{L1 + L2}. \quad (5)$$

Since identical filter inductors ($L1 = L2$) are used in this paper, the V_{ECM} is equal to V_{CM}

$$V_{ECM} = V_{CM} = \frac{V_{AN} + V_{BN}}{2}. \quad (6)$$

From the model, it can be concluded that the leakage current is very much dependent of the CMV. Thus, converter structure and the modulation technique must

p-ISSN: 2348-6848
e-ISSN: 2348-795X
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October 2016

be designed to generate constant CMV in order to eliminate the leakage current. It is worth highlighting that the model in Fig. 2(c) has been commonly used for describing the common-mode behaviour of the conventional full-bridge (H4) topology. However, due to the generality of the model, it is obvious that the model is valid for other topologies discussed here, apart from H4. As a matter of fact, the same model has been used to analyze the common-mode behaviour of various transformers less converter topologies. However, since different topology has different ***VAN*** and ***VBN*** , the expressions for ***VC M*** and ***VDM*** will differ from one another, which yield different common-mode behaviour.

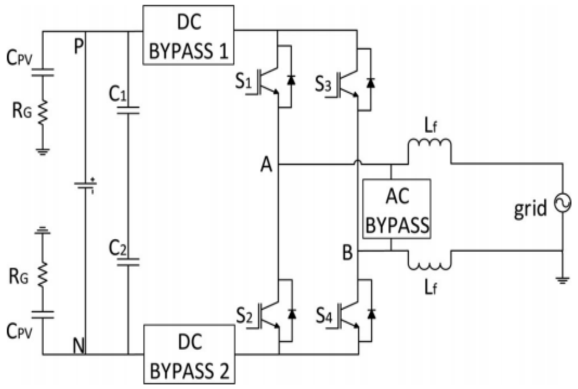
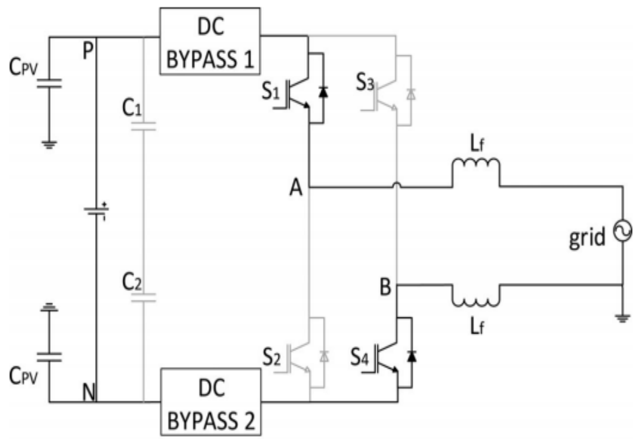


Fig. 3. Universal transformerless topologies.

Hence, to evaluate the common mode behaviour of a particular topology, *VAN* and *VBN* under different switching condition need to be evaluated, as will be shown later.

A. Galvanic Isolation In transformer less PV inverters, the galvanic connection between the PV and the grid allows leakage current to flow. Hence, in topologies such as H5 and HERIC, galvanic isolation is provided to reduce the leakage current. The galvanic isolation can basically be categorized into dc-decoupling and ac-decoupling methods. For dc-decoupling method, dc-bypass switches are added on the dc side of the inverter to disconnect the PV arrays from the grid during the freewheeling period. However, the dc-bypass branch, which consists of switches or diodes, is included in the conduction path as shown in Fig. 3. For H6, output current flows through two switches and the two dc-bypass branches during the conduction period. Hence, the conduction losses increase due to the increased number of semiconductors in the conduction path. On the other hand, bypass branch can also be provided on the ac side of the inverter (i.e., ac-decoupling method) such as seen in HERIC. This ac-bypass branch functions as a freewheeling path which is completely isolated from the conduction path, as shown in Fig. 3. As a result, the output current flows through only two switches during the conduction period. Therefore, topologies employing ac-decoupling techniques are found to be higher in efficiency as compared to dc-decoupling topologies. One setback of galvanic isolation is that there is no way of controlling the CMV by PWM during the freewheeling period. Fig. 4 shows operation modes of galvanic isolation which



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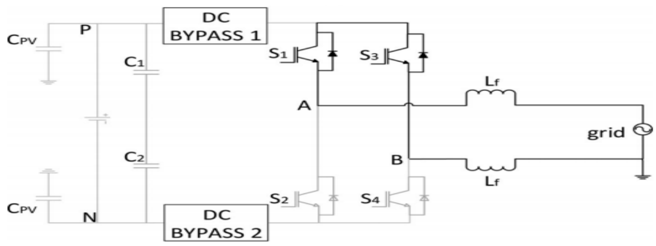

(b)

Fig. 4. Operation modes of dc-decoupling topology. (a) Conduction mode and (b) freewheeling mode

employs dc-decoupling method. As shown in Fig. 4(a), during the conduction period, *S*1 and *S*4 conduct to generate the desired output voltage. At the same time, ***VA*** is directly connected to ***VDC*** and ***VB*** is connected to the negative terminal (*N*) of the dc-link. Hence, the CMV becomes

$$V_{CM} = \frac{V_{AN} + V_{BN}}{2} = \frac{1}{2}(V_{DC} + 0) = \frac{V_{DC}}{2}. \quad (7)$$

Nevertheless, during the freewheeling period, the dc-bypass switches disconnect the dc-link from the grid. Therefore, point *A* and point *B* are isolated from the dc-link, and ***VA*** and ***VB*** are floating with respect to the dc-link as shown in Fig. 4(b). The CMV during this period of time is not determined by the switching state, but

p-ISSN: 2348-6848
e-ISSN: 2348-795X
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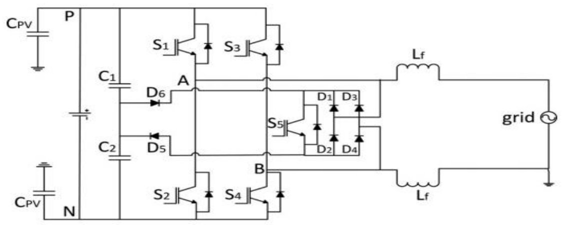
instead, is oscillating with amplitude depending on the parasitic parameters and the switches' junction capacitances of the corresponding topology. As a result, leakage current can still flow during freewheeling period. The same is the case for converters using ac decoupling method

B. CMV Clamping As mentioned earlier, CMV is one of the main causes for leakage current. H5 and HERIC focus only on providing galvanic isolation while neglecting the effect of the CMV. Unlike conventional topologies, the CMV in these topologies cannot be manipulated via PWM, due to the use of galvanic isolation as explained previously. In order to generate constant CMV, clamping branch is introduced in oH5 [see Fig. 1(d)] and H6 [see Fig. 1(e)].



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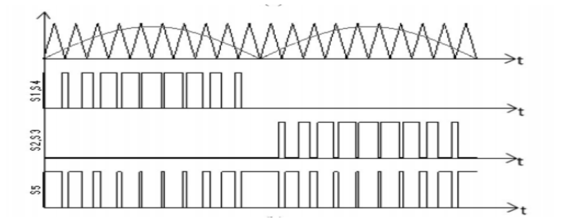


(b)

Fig. 5. Proposed HBZVR-D topology. (a) Converter structure. (b) Switching waveforms

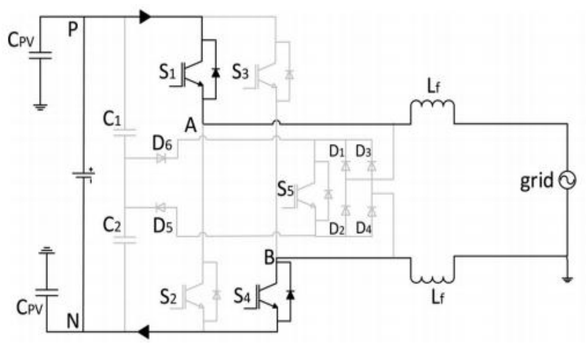
Generally, the clamping branch consists of diodes or switches and a capacitor divider which ensures the freewheeling path is clamped to the half of the input voltage. With the combined effect of galvanic isolation and CMV clamping, leakage current is completely eliminated. Nevertheless, both H6 and oH5 uses dc-decoupling method, which suffers from lower efficiency. HBZVR also employs CMV clamping technique but it is found that the clamping branch does not function optimally. It is shown in both the simulation and experimental results that the CMV and the leakage current in HBZVR are as high as those in the topologies which use only galvanic isolation.

III. OPERATION PRINCIPLES OF PROPOSED TOPOLOGY

A. Structure of Proposed HBZVR-D

Based on the analysis above, a simple modified HBZVR-D is proposed to combine the benefits of the low-loss ac-decoupling method and the complete leakage current elimination of the CMV clamping method. HBZVR-D is modified by adding a fast-recovery diode, *D*6, to the existing HBZVR as shown in Fig. 5(a). The voltage divider is made up of *C*1 and *C*2. *S*1−*S*4 are the switches for full-bridge inverter. The anti parallel diodes, *D*1−*D*4, as well as *S*5 provide a freewheeling path for the current to flow during the freewheeling period. Diodes *D*5 and *D*6 form the clamping branches of the freewheeling path.

B. Operation Modes and Analysis In this section, the operation modes and the CMV of the proposed topology is discussed. Fig. 5(b) illustrates the switching



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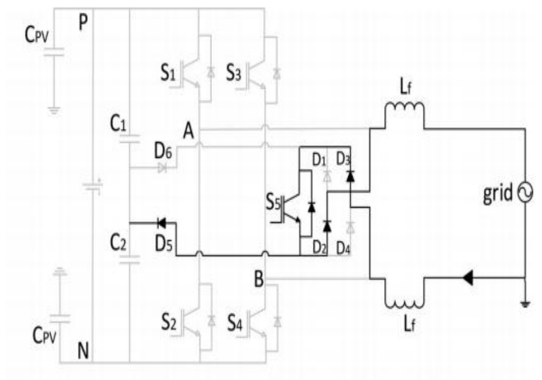

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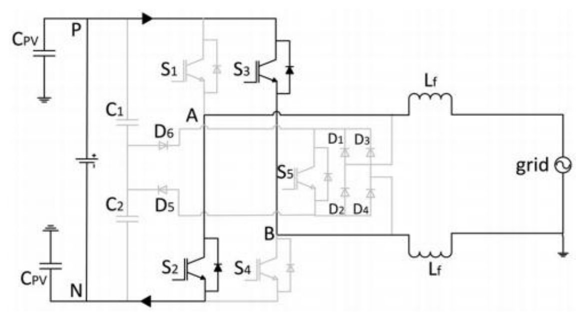

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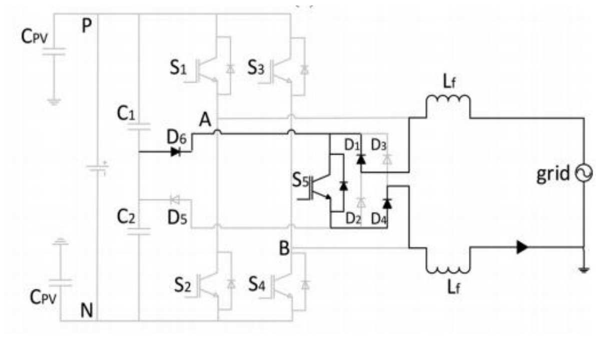

(d)

Fig. 6. Operation modes of proposed HBZVR-D topology. (a) Mode 1—conduction mode and (b) Mode 2—freewheeling mode during positive half cycle. (c) Mode 3—conduction mode and (d) Mode 4—freewheeling mode during negative half cycle.

patterns of the proposed HBZVR-D. Switches *S*1−*S*4 commutate at switching frequency to generate unipolar output voltage. *S*5 commutates complementarily to *S*1−*S*4 to create freewheeling path. All the four operation modes are shown in Fig. 6 to generate unipolar output voltage. In mode 1, *S*1 and *S*4 are ON while *S*2,*S*3 and *S*5 are OFF. Current increases and flows through *S*1 and *S*4. ***VAB*** = +***VDC*** . The CMV becomes

$$V_{CM} = \frac{V_{AN}+V_{BN}}{2} = \frac{1}{2}(V_{DC}+0) = \frac{V_{DC}}{2}. \quad \textbf{(8)}$$

In mode 2, *S*1−*S*4 are OFF. *S*5 is ON to create a freewheeling path. Current decreases and freewheels through diodes *D*3,*D*2, and the grid. The voltage ***VAN*** decreases and ***VBN*** increases until their values reach the common point, ***VDC*** /2, such that ***VAB*** = 0. The CMV is

$$V_{CM} = \frac{V_{AN}+V_{BN}}{2} = \frac{1}{2}\left(\frac{V_{DC}}{2}+\frac{V_{DC}}{2}\right) = \frac{V_{DC}}{2}. \quad \textbf{(9)}$$

In mode 3, *S*2 and *S*3 are ON, while *S*1,*S*4 and *S*5 are OFF. Current increases and flows through *S*2 and *S*3. ***VAB*** = −***VDC*** . The CMV becomes

$$V_{CM} = \frac{V_{AN}+V_{BN}}{2} = \frac{1}{2}(0+V_{DC}) = \frac{V_{DC}}{2}. \quad \textbf{(10)}$$

In mode 4, *S*1−*S*4 are OFF. *S*5 is ON to create freewheeling path. Current decreases and freewheels through diodes *D*1,*D*4, and the grid. The voltage ***VAN*** decreases and ***VBN*** increases until their values reach the common point, ***VDC*** /2, and ***VAB*** = 0. The CMV is as derived in (10). Obviously, modulation techniques are designed to generate constant CMV in all four operation modes. All the research works are designed based on the principles above. Practically, ***VAN*** and ***VBN*** do not reach common point during the freewheeling period (mode 2 and mode 4). It is shown in simulation and experimental results later that the CMV is not constant without clamping branch. During the freewheeling period, both ***VAN*** and ***VBN*** are not clamped to ***VDC*** /2 and is oscillating with amplitude depending on the parasitic parameters and junctions' capacitance of those topologies. The improved clamping branch of HBZVR-D ensures the complete clamping of CMV to ***VDC*** /2 during the freewheeling period. It is well noted that the output current flows through only two switches in every conduction period (mode 1 and mode 3) as shown in Fig. 6(a) and (c). This explains why HBZVR-D has relatively higher efficiency than those of dc-decoupling topologies.

C. Operation Principles of Improved Clamping Branch

During the freewheeling period, *S*5 is turned ON, connecting point A and B. Freewheeling path voltage ***VF P*** can be defined as ***VF P*** =***VAN*** ≈***VBN*** , since the voltage drops across diodes and *S*5 are small compared to ***VDC*** . There are two possible modes of operation (mode 2 and mode 4 as shown in Fig. 6) depending on whether *D*5 or *D*6 is forward biased. When ***VF P*** is greater than ***VDC*** /2, *D*5 is forward biased and *D*6 is reversed biased. Current flows from the freewheeling path to the midpoint of the dc-link via the clamping diode *D*5, as shown in Fig. 6(b), which completely clamps the ***VF P*** to ***VDC*** /2. On the other hands, when the ***VF P*** is less than ***VDC*** /2, *D*6 is forward biased and *D*5 is reversed biased. As shown in Fig. 6(d), current flows from the midpoint of the dc-link to the freewheeling path via the added clamping diode *D*6, to increase the ***VF P*** to ***VDC*** /2. It should be noted that during the dead time between the conduction period and freewheeling period, the freewheeling path is not well-clamped and the CMV can be oscillating with the grid voltage. Nevertheless, with proper selection of dead time, this effect can be minimized. In HBZVR, the clamping branch consists of *D*5 only. Thus, the clamping of the freewheeling path is limited only for the period when ***VF P*** is more than ***VDC*** /2. When ***VF P*** is less than ***VDC*** /2, the clamping branch does not function because *D*5 is reversing biased. During such condition, the CMV in HBZVR will oscillate, causing the flow of leakage current. This setback is rectified by adding a fast-recovery diode *D*6 in the proposed HBZVR-D topology. With both *D*5 and *D*6, the improved clamping branch guarantees the complete clamping of the CMV to ***VDC*** /2 throughout the freewheeling period. As a result, leakage current, which is very much dependent on CMV, is completely eliminated.

IV. SIMULATION RESULTS

A) Simulation block diagram:

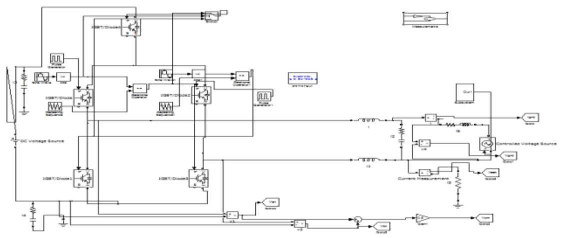

Fig 7 Matlab/Simulation circuit of single-phase full bridge controller

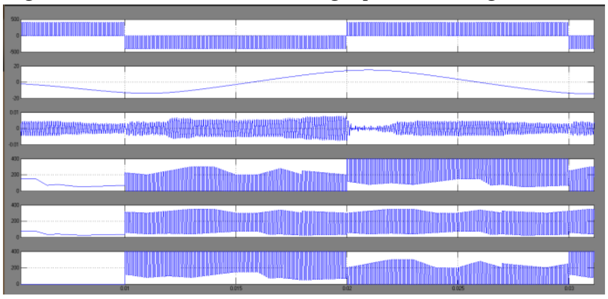

Fig 8 simulation wave form of grid voltage and current leakage current, neutral line voltage

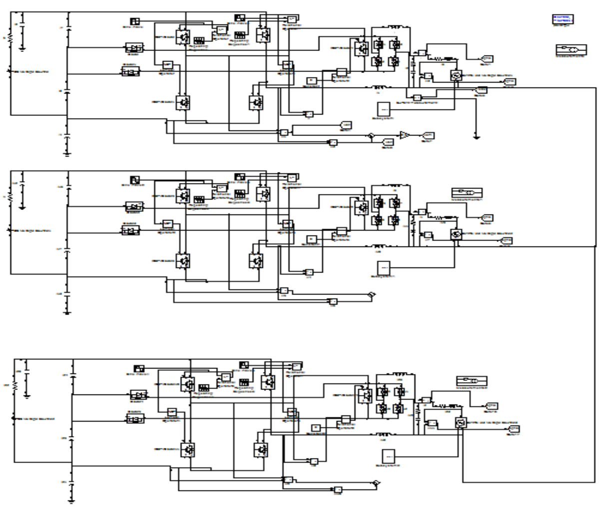

Fig.9. Matlab/simulation proposed circuit of three-phase controller

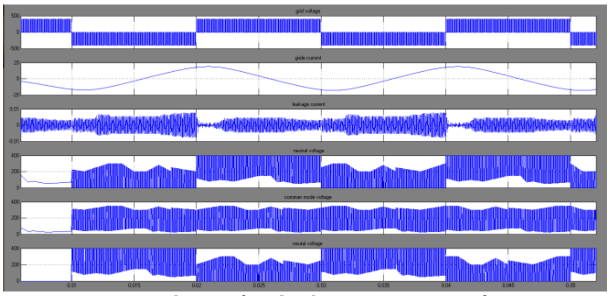

Fig 10.simulation of grid voltage, current wave forms

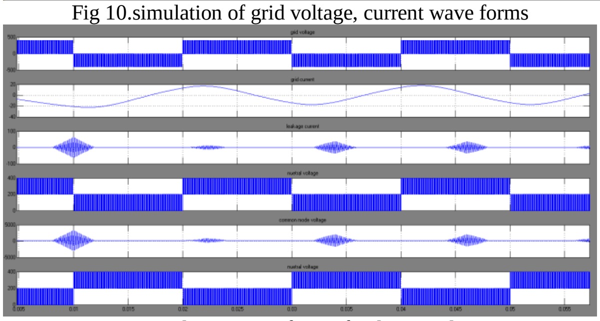

Fig 11.simulation wave form of voltage and current

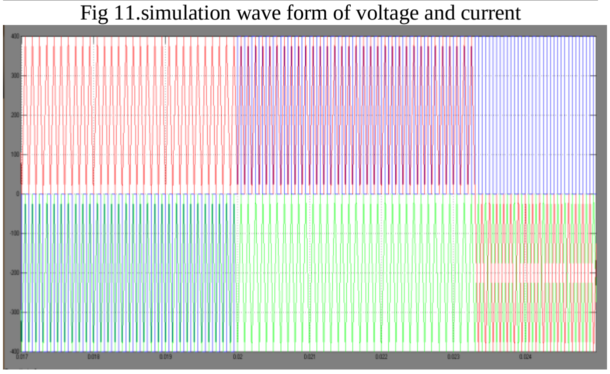

Fig 12.simulation wave form of three-phase grid voltage,

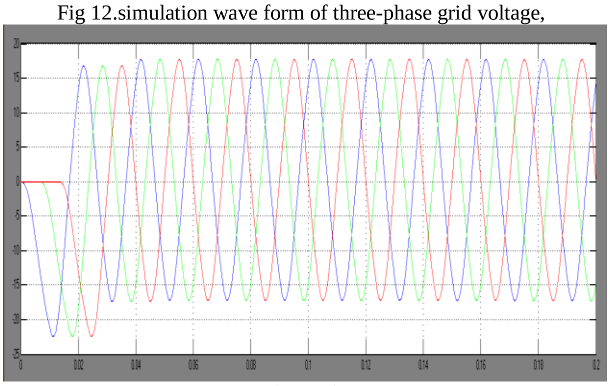

Fig 13. Simulation wave form of three-phase grid current

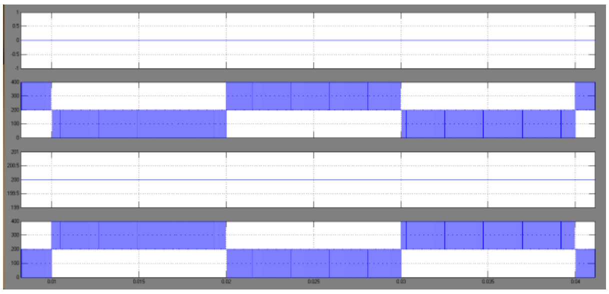

Fig 14.simulation wave form of three-phase current and voltage

V. CONCLUSION

This paper presents the speed control of Three-Phase using Anti-windup PI controller, and Hybrid Controller.

p-ISSN: 2348-6848
e-ISSN: 2348-795X
Volume 03 Issue 14
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The simulation results are compared with Hybrid controller results. Anti-windup PI controller, results are slower compared to Three-Phase. From the simulation results, it is clear that for the load variation and speed variation hybrid controller gave better response than Anti-windup PI controller. Hence hybrid controller is found to be more suitable for Three-Phase during speed variation and load variation.

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AUTHORS:

Uppala Naresh received B-tech from Ellnnki College of Engineering in the year 2013 and now pursuing M.Tech in the stream of Electrical power systems at Anurag College of Engineering

SaralaSandolu received M.TECH degree from JNTU Kakinada in the year 2011 and received M.Tech in the stream of advanced Power Systems Currently working as a Assistant Professor in Anurag College Of Engineering.