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Seventeen-Level Inverter Formed by Cascading Flying Capacitor and Floating Capacitor H-Bridges

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***Abstract*—A multilevel inverter for generating 17 voltage levels using a three-level flying capacitor inverter and cascaded H-bridge modules with floating capacitors has been proposed. Various aspects of the proposed inverter like capacitor voltage balancing have been presented in the present paper. Experimental results are presented to study the performance of the proposed converter. The stability of the capacitor balancing algorithm has been verified both during transients and steady-state operation. All the capacitors in this circuit can be balanced instantaneously by using one of the pole voltage combinations. Another advantage of this topology is its ability to generate all the voltages from a single dc-link power supply which enables back-to-back operation of converter. Also, the proposed inverter can be operated at all load power factors and modulation indices. Additional advantage is, if one of the H-bridges fail, the inverter can still be operated at full load with reduced number of levels. This configuration has very low dv/dt and common-mode voltage variation.**

***Index Terms*—Cascaded H-bridge, flying capacitor, multilevel inverter, 17-level inverter.**

I. INTRODUCTION

WITH the advent of multilevel inverters, the performance of medium and high-voltage drives have changed drastically [1]–[3]. As the number of voltage levels increases, the output voltage is closer to sine wave with reduced harmonic content, improving the performance of the drive greatly as presented in [4] and [5]. One of the pioneering works in the field of multilevel inverters is the neutral point clamped inverter [6]. On the other hand, the use of multiple isolated dc sources using H-bridges for plasma stabilization generating multiple voltage levels was presented in [7]. The work presented in [8] analyzes the issues with the scheme of cascading multiple rectifiers and proposes a solution for balancing the capacitors. The work presented in [9] generates multiple voltage levels by switching the load current through capacitors. Here, the voltage through the capacitors can be maintained at desired value by changing the direction of load current through the capacitor by choosing the redundant states for the same pole voltage. The work presented in [10] combines the concepts of work presented in [9] and [7]. Here, the floating capacitor H-bridges are used to generate multiple output voltages. The voltages of the capacitors are maintained at their intended values by switching through redundant states for the same voltage level. The works presented in [11]–[15] address aspects of using cascaded H-bridges and propose various efficient control algorithms.

Modular multi- level converters which are very popular in HVDC applications are another genre of multilevel converters which can be used for motor drive applications as presented in [16]–[18]. The concept of cascading flying capacitor inverter with neutral point clamped inverter is presented in [19]. Similar concept has been made available commercially as ABB ACS 2000. The concept of increasing the number of levels using flying capacitor inverter with cross connected capacitors has been presented in [20]. An interesting configuration to generate 17 voltage levels using multiple capacitors is presented in [21]. However in [20] and [21], the capacitor voltages cannot be balanced instantaneously. They can be balanced only at the fundamental frequency. A single-phase seventeen-level inverter configuration is presented in [22] uses large number of power supplies and has a floating load. This is more suitable for STATCOM applications. An attractive algorithm for operating seventeen level inverter has been presented in [23].

In the present paper, we propose a new 17-level inverter formed by cascading three-level flying capacitor inverter with floating capacitor H-bridges which uses a single dc supply and derives all the required voltage levels from it. The performance of the proposed configuration is experimentally verified both for steady state operation and during transients and the results are presented.

II. POWER CIRCUIT TOPOLOGY

The proposed converter is a hybrid multilevel topology employing a three-level flying capacitor inverter and cascading it with three floating capacitor H-Bridges. The three-phase power schematic is shown in Fig. 1. The voltages of capacitors AC1, BC1, and CC1 are maintained at Vdc/2. Capacitors AC2, BC2, and CC2 are maintained at voltage level of Vdc/4. Similarly capacitors AC3, BC3, and CC3 are maintained at voltage level of Vdc/8 and capacitors AC4, BC4, and CC4 are maintained at voltage level of Vdc/16. Each cascaded H-bridge can either add or subtract its voltage to the voltage generated by its previous stage. In addition to that, the CHBs can also be bypassed. The resulting

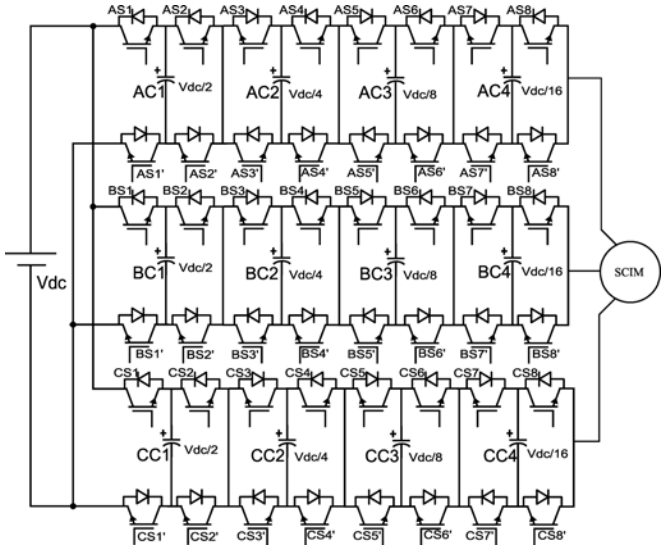


Fig. 1. Three-phase power schematic of the proposed seventeen-level inverter configuration formed by cascading three-level flying capacitor inverter with three H-bridges using a single dc link.

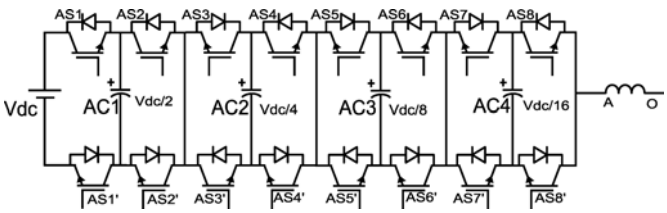


Fig. 2. One phase of the proposed 17-level inverter configuration formed by cascading three-level flying capacitor inverter with three H-bridges using a single dc link.

inverter pole voltage is the arithmetic sum of voltages of each stage. The schematic diagram for one phase of the proposed converter is shown in Fig. 2. The switch pairs (AS1, AS1'), (AS2, AS2'), (AS3, AS3'), (AS4, AS4'), (AS5, AS5'), (AS6, AS6'), (AS7, AS7'), and (AS8, AS8') are switched in complementary fashion with appropriate dead time. Each switch pair has two distinct logic states, namely top device is ON (denoted by 1) or the bottom device is ON (denoted by 0). Therefore, there are 256 (2^8) distinct switching combinations possible. Each voltage level can be generated using one or more switching states (pole voltage redundancies). By switching through the redundant switching combinations (for the same pole voltage), the current through capacitors can be reversed and their voltages can be controlled to their prescribed values. This method of balancing the capacitor voltages at all load currents and power factors instantaneously has been observed for 17 pole voltage levels. They are 0, Vdc/16, Vdc/8, 3 Vdc/16, Vdc/4, 5 Vdc/16, 3 Vdc/8, 7 Vdc/16, Vdc/2, 9 Vdc/16, 5 Vdc/8, 11 Vdc/16, 3 Vdc/4, 13 Vdc/16, 7 Vdc/8, 15 Vdc/16, and Vdc. However, by switching through all the possible pole voltage switching combinations, 31 distinct pole voltage levels can be generated using the proposed topology. In the additional 14 levels, the voltages of capacitors can be balanced only in a fundamental cycle.

There are 82 switching combinations (see Table I) that can be used to generate the above mentioned 17 pole voltage levels where instantaneous capacitor voltage balancing is possible. The effect of 82 switching combinations on every capacitor's charge state (charge or discharge) for positive direction of current (i.e., when the pole is sourcing current as marked in Fig. 3) is shown in Table I. For negative direction of current, the effect of the switching state on the capacitor is reversed. For example, when the controller demands a pole voltage of Vdc/16, there are five different redundant switching combinations to generate it. Each switching combination has a different effect on the state of charge of the capacitors. When the switching state (0, 0, 0, 0, 0, 0, 0, 1) (see Table I) is applied, the capacitor C4 discharges when the pole is sourcing current as [see Fig. 3(a)]. To balance the capacitor C4 and to bring its voltage back to the prescribed value (Vdc/16), one of the other four switching combinations is applied Fig. 3(b)–(e). It can be observed that when switching state (0, 0, 0, 0, 0, 1, 1, 0) is applied, the direction of current in the capacitor C4 is reversed [see Fig. 3(b)] and the capacitor C4 charges. However in this process, the capacitor C3 is discharged. If the capacitor C3 needs charging, switching state redundancy of (0, 0, 0, 1, 1, 0, 1, 0) is applied [see Fig. 3(c)] which discharges C2. To charge C2 one of the switching redundancies shown in Fig. 3(d) and (e) is applied based on the state of charge of capacitor C1. If switching state (0, 1, 1, 0, 1, 0, 1, 0) is applied, the capacitor C1 is discharged and this state charges all the other capacitors as shown in Fig. 3(d). Finally, when switching state of (1, 0, 1, 0, 1, 0, 1, 0) is applied, all the four capacitors are charged for positive direction of current as shown in Fig. 3(e). By switching through the redundant pole voltage combinations, it can be observed that the all the capacitors' voltages can be maintained at their prescribed values while generating pole voltage of Vdc/16 for positive direction of current. If all the capacitors need discharging, the capacitor C4 is discharged first and the remaining capacitors can be discharged during subsequent switching cycles when C4 needs to be charged. For negative direction of current, the effect of the capacitor voltages is the opposite. The entire process of capacitor voltage balancing for pole voltage of Vdc/16 that has been explained is illustrated in Fig. 4. Here, the capacitor voltage variation with application of various redundant states for pole voltage of Vdc/16 has been shown for positive direction of current. For other pole voltages namely, Vdc/8, 3 Vdc/16, Vdc/4, 5 Vdc/16, 3 Vdc/8, 7 Vdc/16, Vdc/2, 9 Vdc/16, 5 Vdc/8, 11 Vdc/16, 3 Vdc/4, 13 Vdc/16, 7 Vdc/8, 15 Vdc/16, and Vdc, a similar strategy can be used to balance all the capacitor voltages. The switching frequency of any CHB module is at most the PWM switching frequency of the converter. This is due to the synchronization of application of the switching state with every PWM transition (the switching state is latched till the next PWM transition). Moreover in this scheme, only the capacitors that contribute to the output pole voltages are switched.

III. Space Vector Control Region

Each pole of the three-phase inverter can generate one of the 17 discrete pole voltage levels namely 0, Vdc/16, Vdc/8,

TABLE I
POLE VOLTAGE REDUNDANCIES AND CAPACITOR STATES FOR VARIOUS SWITCHING COMBINATIONS WHEN POLE SOURCES CURRENT

S. No.	Pole Voltage	Switch State (S1, S2, S3, S4, S5, S6, S7, S8)	C1[a]	C2[a]	C3[a]	C4[a]	S.No	Pole Voltage	Switch State (S1, S2, S3, S4, S5, S6, S7, S8)	C1[a]	C2[a]	C3[a]	C4[a]
1	0	(0, 0, 0, 0, 0, 0, 0, 0)	0	0	0	0	42	Vdc/2	(1, 0, 0, 0, 0, 0, 0, 0)	+	0	0	0
2	Vdc/16	(0, 0, 0, 0, 0, 0, 0, 1)	0	0	0	−	43	9 Vdc/16	(0, 1, 0, 0, 0, 0, 0, 1)	−	0	0	−
3		(0, 0, 0, 0, 0, 1, 1, 0)	0	0	−	+	44		(0, 1, 0, 0, 0, 1, 1, 0)	−	0	−	+
4		(0, 0, 0, 1, 1, 0, 1, 0)	0	−	+	+	45		(0, 1, 0, 1, 1, 0, 1, 0)	−	−	+	+
5		(0, 1, 1, 0, 1, 0, 1, 0)	−	+	+	+	46		(1, 0, 0, 0, 0, 0, 0, 1)	+	0	0	−
6		(1, 0, 1, 0, 1, 0, 1, 0)	+	+	+	+	47		(1, 0, 0, 0, 0, 1, 1, 0)	+	0	−	+
7	Vdc/8	(0, 0, 0, 0, 0, 1, 0, 0)	0	0	−	0	48		(1, 0, 0, 1, 1, 0, 1, 0)	+	−	+	+
8		(0, 0, 0, 1, 1, 0, 0, 0)	0	−	+	0	49		(1, 1, 1, 0, 1, 0, 1, 0)	0	+	+	+
9		(0, 1, 1, 0, 1, 0, 0, 0)	−	+	+	0	50	5 Vdc/8	(0, 1, 0, 0, 0, 1, 0, 0)	−	0	−	0
10		(1, 0, 1, 0, 1, 0, 0, 0)	+	+	+	0	51		(0, 1, 0, 1, 1, 0, 0, 0)	−	−	+	0
11	3 Vdc/16	(0, 0, 0, 0, 0, 1, 0, 1)	0	0	−	−	52		(1, 0, 0, 0, 0, 1, 0, 0)	+	0	−	0
12		(0, 0, 0, 1, 0, 0, 1, 0)	0	−	0	+	53		(1, 0, 0, 1,1, 0,0, 0)	+	−	+	0
13		(0, 0, 0, 1, 1, 0, 0, 1)	0	−	+	−	54		(1, 1, 1, 0, 1, 0, 0, 0)	0	+	+	0
14		(0, 1, 1, 0, 0, 0, 1, 0)	−	+	0	+	55	11 Vdc/16	(0, 1, 0, 0, 0, 1,0, 1)	−	0	−	−
15		(0, 1, 1, 0, 1, 0, 0, 1)	−	+	+	−	56		(0, 1, 0, 1, 0, 0, 1, 0)	−	−	0	+
16		(1, 0, 1, 0, 0, 0, 1, 0)	+	+	0	+	57		(0, 1, 0, 1, 1, 0, 0, 1)	−	−	+	−
17		(1, 0, 1, 0, 1, 0, 0, 1)	+	+	+	−	58		(1, 0, 0, 0, 0, 1, 0, 1)	+	0	−	−
18	Vdc/4	(0, 0, 0, 1, 0, 0, 0, 0)	0	−	0	0	59		(1, 0, 0, 1, 0, 0, 1, 0)	+	−	0	+
19		(0, 1, 1, 0, 0, 0, 0, 0)	−	+	0	0	60		(1, 0, 0, 1, 1, 0, 0, 1)	+	−	+	−
20		(1, 0, 1, 0, 0, 0, 0, 0)	+	+	0	0	61		(1, 1, 1, 0, 0, 0, 1, 0)	0	+	0	+
21	5 Vdc/16	(0, 0, 0, 1, 0, 0, 0, 1)	0	−	0	−	62		(1, 1, 1, 0, 1, 0, 0, 1)	0	+	+	−
22		(0, 0, 0, 1, 0, 1, 1, 0)	0	−	−	+	63	3 Vdc/4	(0, 1, 0, 1, 0, 0, 0, 0)	−	−	0	0
23		(0, 1, 0, 0, 1, 0, 1, 0)	−	0	+	+	64		(1, 0, 0, 1, 0, 0, 0, 0)	+	−	0	0
24		(0, 1, 1, 0, 0, 0, 0, 1)	−	+	0	−	65		(1, 1, 1, 0, 0, 0, 0, 0)	0	+	0	0
25		(0, 1, 1, 0, 0, 1, 1, 0)	−	+	−	+	66	13 Vdc/16	(0, 1, 0, 1, 0, 0, 0, 1)	−	−	0	−
26		(1, 0, 0, 0, 1, 0, 1, 0)	+	0	+	+	67		(0, 1, 0, 1, 0, 1, 1, 0)	−	−	−	+
27		(1, 0, 1, 0, 0, 0, 0, 1)	+	+	0	−	68		(1, 0, 0, 1, 0, 0, 0, 1)	+	−	0	−
28		(1, 0, 1, 0, 0, 1, 1, 0)	+	+	−	+	69		(1, 0, 0, 1, 0, 1, 1, 0)	+	−	−	+
29	3 Vdc/8	(0, 0, 0, 1, 0, 1, 0, 0)	0	−	−	0	70		(1, 1, 0, 0, 1, 0, 1, 0)	0	0	+	+
30		(0, 1, 0, 0, 1, 0, 0, 0)	−	0	+	0	71		(1, 1, 1, 0, 0, 0, 0, 1)	0	+	0	−
31		(0, 1, 1, 0, 0, 1, 0, 0)	−	+	−	0	72		(1, 1, 1, 0, 0, 1, 1, 0)	0	+	−	+
32		(1, 0, 0, 0, 1, 0, 0, 0)	+	0	+	0	73	7 Vdc/8	(0, 1, 0, 1, 0, 1, 0, 0)	−	−	−	0
33		(1, 0, 1, 0, 0, 1, 0, 0)	+	+	−	0	74		(1, 0, 0, 1, 0, 1, 0, 0)	+	−	−	0
34	7 Vdc/16	(0, 0, 0, 1, 0, 1, 0, 1)	0	−	−	−	75		(1, 1, 0, 0, 1, 0, 0, 0)	0	0	+	0
35		(0, 1, 0, 0, 0, 0, 1, 0)	−	0	0	+	76		(1, 1, 1, 0, 0, 1, 0, 0)	0	+	−	0
36		(0, 1, 0, 0, 1, 0, 0, 1)	−	0	+	−	77	15 Vdc/16	(0, 1, 0, 1, 0, 1, 0, 1)	−	−	−	−
37		(0, 1, 1, 0, 0, 1, 0, 1)	−	+	−	−	78		(1, 0, 0, 1, 0, 1, 0, 1)	+	−	−	−
38		(1, 0, 0, 0, 0, 0, 1, 0)	+	0	0	+	79		(1, 1, 0, 0, 0, 0, 1, 0)	0	0	0	+
39		(1, 0, 0, 0, 1, 0, 0, 1)	+	0	+	−	80		(1, 1, 0, 0, 1, 0, 0, 1)	0	0	+	−
40		(1, 0, 1, 0, 0, 1, 0, 1)	+	+	−	−	81		(1, 1, 1, 0, 0, 1, 0, 1)	0	+	−	−
41	Vdc/2	(0, 1, 0, 0, 0, 0, 0, 0)	−	0	0	0	82	Vdc	(1, 1, 0, 0, 0, 0, 0, 0)	0	0	0	0

Symbols of +, −, and 0 indicates the capacitor is charging, discharging, and no effect respectively for positive direction of current.

3 Vdc/16, Vdc/4, 5 Vdc/16, 3 Vdc/8, 7 Vdc/16, Vdc/2, 9 Vdc/16, 5 Vdc/8, 11 Vdc/16, 3 Vdc/4, 13 Vdc/16, 7 Vdc/8, 15 Vdc/16, and Vdc. For the proposed three-phase inverter, there is a total of 4913 (17^3) pole voltage combinations. Each pole voltage combination generates a voltage space vector $\boldsymbol{V}_{SV}$ as given in the following equation:

$$\boldsymbol{V}_{SV} = V_{AN} + V_{BN} \angle 120^\circ + V_{CN} \angle 240^\circ \qquad (1)$$

where V_{AN}, V_{BN} and V_{CN} are the three-phase voltages. These 4193 pole voltage combinations when marked on a space vector plane spread across 817 distinct space vector locations. Each of the 817 space vector locations can have more than one pole voltage combination (phase voltage redundancy) with different common mode voltages. In addition, each pole voltage can have one or more redundant switching combination (pole voltage redundancy which can be used to balance the capacitor voltages of that particular phase) as described in the previous section. The diagram of the space vector polygon formed by these 817 locations is shown in Fig. 5. There 16 concentric hexagons that form the space vector control region of the proposed seventeen-level inverter. The space vectors on the outer hexagon do not have any phase voltage redundancies. The locations on the second largest hexagon have double redundancy and can be generated with two sets of pole voltages with different common mode voltages. For the smaller inner hexagons, the number of pole voltage combinations for generating the space vector locations increases. There are 16 redundant pole voltage combinations each with a different common mode voltage for each space vector location on the innermost hexagon. Therefore, the zero state at the center has a total of seventeen pole voltage combinations all of which generate zero differential mode voltage.

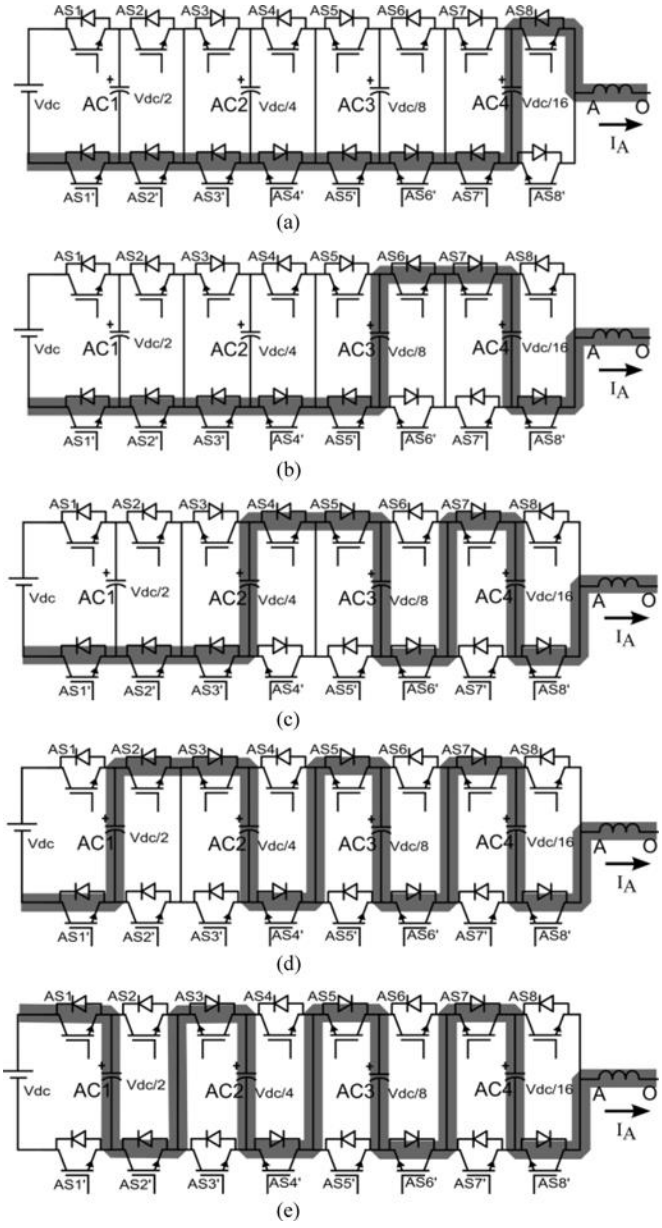


Fig. 3. Switching Redundancies for pole voltage of Vdc/16. (a) Current path for switching state (0, 0, 0, 0, 0, 0, 0, 1). (b) Current path for switching state (0, 0, 0, 0, 0, 1, 1, 0). (c) Current path for switching state (0, 0, 0, 1, 1, 0, 1, 0). (d) Current path for switching state (0, 1, 1, 0, 1, 0, 1, 0). (e) Current path for switching state (1, 0, 1, 0, 1, 0, 1, 0).

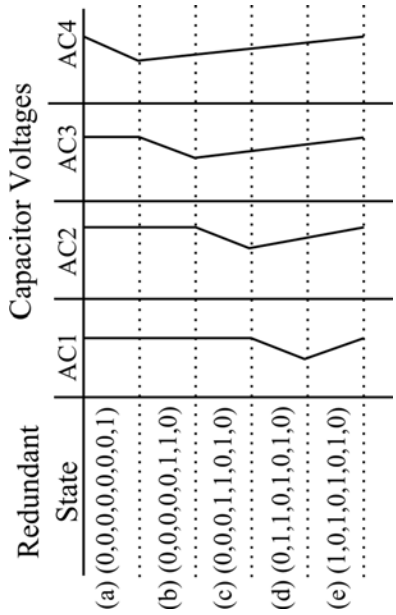


Fig. 4. Capacitor voltage variation with application of redundant states for pole voltage of Vdc/16 for positive current.

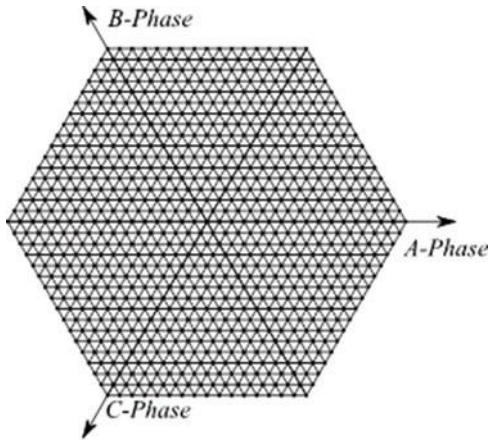


Fig. 5. Space vector polygon formed with the proposed five-level inverter.

IV. Implementation

The block diagram of the controller to generate the switching signals for the inverter is presented in Fig. 6. The control algorithm can be anything like V/f or vector control or any other algorithm which demands a particular set of reference voltage levels for the three phases. These voltage levels are sent to level-shifted carrier based space vector PWM generation algorithm implemented in DSP as described in [24], the output of which is (fed to FPGA) a set of level data and the PWM signal for each phase. This data is fed to a level synthesizer which generates the instantaneous level based on the PWM signal and the level data. The instantaneous level data is fed to a switching state generator which generates an appropriate switching state based on the demanded level, the state of capacitor voltages and current. This is achieved by implementing the logic described in Table I as a look up table in FPGA. This switching state is fed to a dead time generation circuit which generates the gating signals for the top and bottom devices which have complementary operation with suitable dead time. The dead time generation circuit is also implemented in FPGA thereby avoiding any need for external hardware and providing consistent dead band.

V. Experimental Results

The proposed 17-level inverter is realized using Semikron SKM75GB12T4 IGBT modules. Mitsubishi M57962L hybrid drivers are used to drive the IGBT modules. Twelve capacitor banks of 2.2 mF are used to realize the 12 capacitors for the

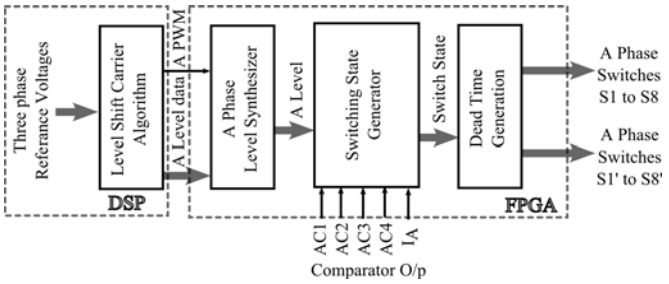


Fig. 6. Block diagram of controller for one phase of the proposed converter.

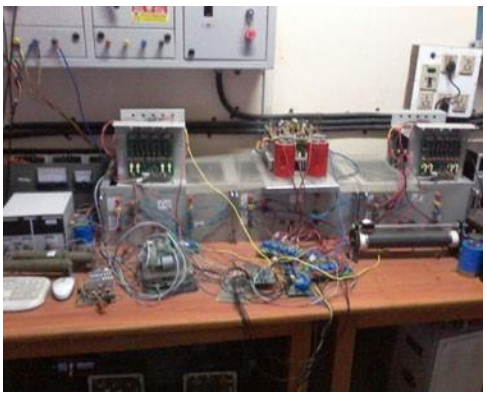
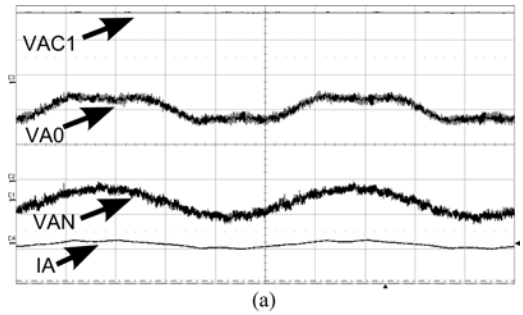
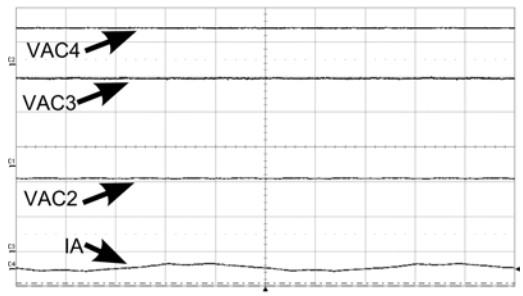


Fig. 7. Experimental setup of the proposed 17-level inverter configuration.

17-level inverter. The dc bus is fed by a three-phase auto transformer feeding a rectifier. A capacitor bank of 1.1 mF is used to realize the dc bus. The image of the experimental setup is shown in Fig. 7. The controller is realized by using a combination of a Texas Instruments DSP TMS320F2812 and Xilinx SPARTAN-3 XC3S200 FPGA. The motor control algorithm along with the level-shifted carrier based space vector PWM generation logic (by addition of common mode voltage to reference voltages [24]) has been implemented in DSP. The DSP feeds the three-phase voltage level data along with the PWM signals to the FPGA which has the capacitor balancing logic and switching state generation scheme. The dead band generation scheme has been implemented in FPGA itself. Each phase has total of 16 devices and there are total of 48 (16 × 3) IGBT gating signals routed from the FPGA to the inverter modules. All the capacitor voltages are sensed using LEM LV20-P hall-effect based voltage sensors. The sensed voltages are compared with a set of reference voltages using hysteresis comparators (implemented using LM339), the output of which is fed to the FPGA. The inverter is switched at 1 kHz. Precise dead time of 2 μs is provided between the complementary signals by using a timing logic implemented in FPGA. The dc bus is scaled to 200 V dc. A three-phase four pole, 415 V, 50 Hz, Y connected squirrel cage induction motor is run in open loop V/f method to test the performance of the inverter. The motor is run at various frequencies and modulation indices so as to test the performance of the proposed inverter configuration at various instants. The motor is run at frequency of 10 Hz and with modulation index of 0.2.

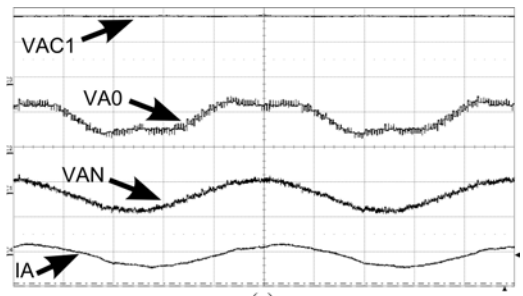


(a)

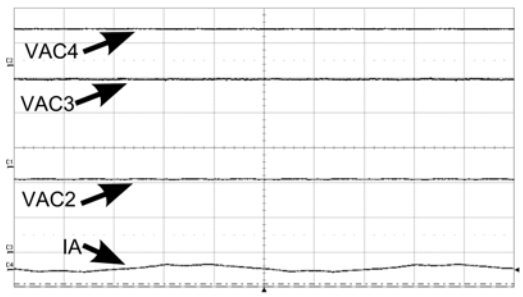


(b)

Fig. 8. Pole, Phase, capacitor voltages along with current for 10-Hz operation of converter. VAC1(50 V/div),VAO: Pole voltage (100 V/div), VAN: Phase Voltage (100 V/div), VAC4: (100 V/div),VAC3: (10 V/div),VAC2: (25 V/div), IA:2 A/div, Timescale: (20 mS/div).



(a)



(b)

Fig. 9. Pole, Phase, capacitor voltages along with current for 20-Hz operation of the converter. VAC1: (50 V/div),VAO: Pole voltage(100 V/div), VAN: Phase Voltage (100 V/div), VAC4: (20 V/div),VAC3: (10 V/div),VAC2: (25 V/div), IA:2 A/div, Timescale: 10 mS/div.

The motor pole voltage, phase voltage, capacitor voltages along with the motor current are presented in Fig. 8. It can be observed that the capacitor voltages are stable and the magnitude of output voltage steps is very low. Similarly the motor is run at a modulation index of 0.4 at 20 Hz, 0.6 at 30 Hz, and 0.8 at 40 Hz (see Figs. 9–11). It can be observed that during steady-state

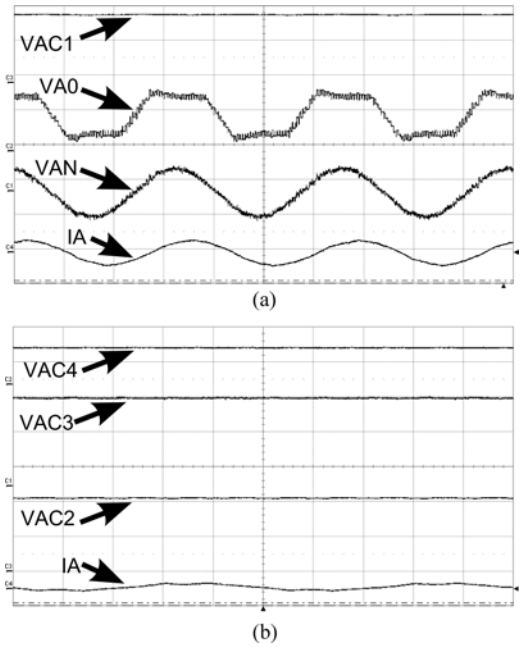


Fig. 10. Pole, Phase, capacitor voltages along with current for 30-Hz operation of the converter. VAC1:(50 V/div), VAO: Pole voltage(100 V/div), VAN: Phase Voltage (100 V/div), VAC4: (20 V/div), VAC3: (10 V/div), VAC2: (25 V/div), IA:2 A/div, Timescale: 10 mS/div.

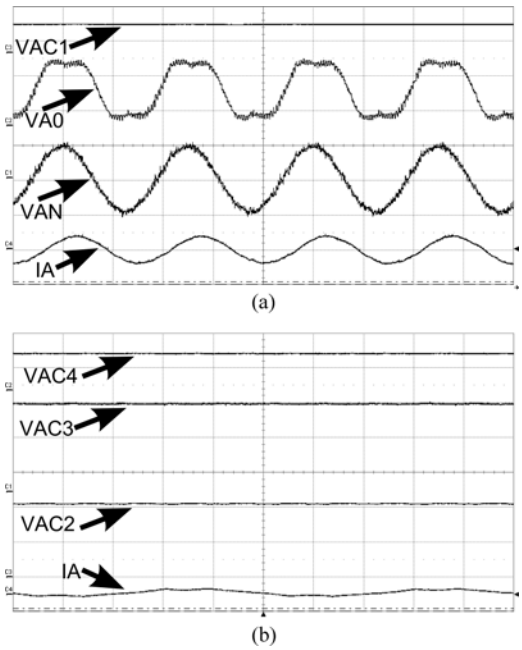
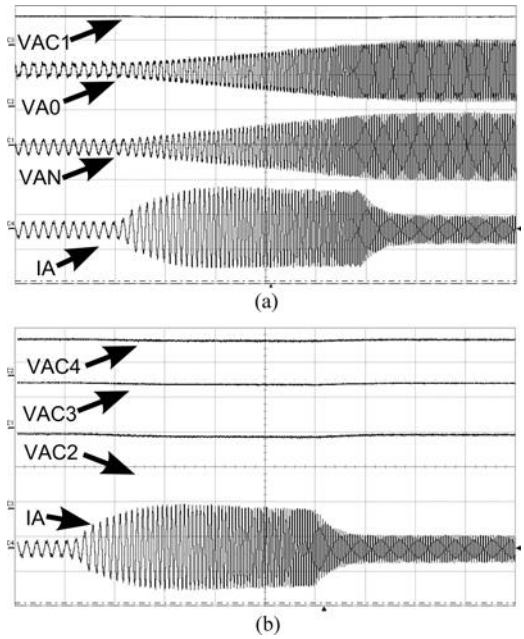


Fig. 11. Pole, Phase, capacitor voltages along with current for 40-Hz operation of the converter. VAC1:(50 V/div), VAO: Pole voltage(100 V/div), VAN: Phase Voltage (100 V/div), VAC4: (10 V/div), VAC3: (10 V/div), VAC2: (100 V/div), IA:2 A/div, Timescale: 5 mS/div.

operation at various modulation indices and frequencies, the controller was able to balance all the capacitor voltages at their prescribed values. And the load current is closer to sinusoid with very low ripple. To test the performance of the capacitor



balancing algorithm, the motor is accelerated from 10 to 40 Hz.

Fig. 12. Pole, Phase, capacitor voltages along with current during sudden acceleration. VAC1:Cap AC1 voltage(100 V/div), VAO: Pole Voltage(100 V/div), VAN: Phase Voltage(100 V/div), VAC4:Cap AC4 voltage(10 V/div), VAC3:Cap AC3 voltage (20 V/div), VAC2:Cap AC2 voltage (20 V/div), IA: Phase current (2 A/div) Timescale: 500 mS/div.

at no load in 2.5 s. The three-phase voltage reference traverses all the inner hexagons and reaches the outer most hexagon gradually. The pole voltage and phase voltage along with the motor current for this acceleration operation are presented in Fig. 12. Here, it can be observed from the experiment that in spite of the machine drawing high currents during acceleration, the voltages of all the capacitors are steady and the inverter is able to produce the voltage demanded by the controller faithfully with low ripple. It can also be noted that the capacitor voltage ripple is close to 5% under sudden transients even when the motor draws huge current from the inverter. From the aforementioned experimental results, it can be noted that the inverter is able to generate the demanded voltage levels faithfully both under steady state and during transients.

VI. Salient Features

Realization of the proposed 17-level inverter needs total of 12 switches rated at Vdc/2 (4 × 3 phases), 12 switches rated at Vdc/4 (4 × 3 phases), 12 switches rated at Vdc/8 (4 × 3 phases), and 12 switches rated at Vdc/16 (4 ×3 phases) with a total of 48 switches. Also, the proposed inverter configuration has a flying capacitor stage and three cascaded floating capacitor H-bridge stages. Hence, each phase of the proposed converter requires one capacitor rated at Vdc/2 and three capacitors each rated at Vdc/4, Vdc/8, and Vdc/16 with a total of 12 capacitors. Compared to flying capacitor inverter and neutral point clamped inverter for same number of levels, the proposed configuration does not require any clamping diodes and has optimum number of stages. When compared to the number of capacitors require for a flying capacitor inverter with instantaneous capacitor bal-

ancing, the proposed configuration has lesser number of capacitors. Also, the proposed converter requires only a single dc-link power source as compared to the conventional cascaded H-bridge configuration which needs many isolated dc power supplies. The proposed configuration has optimal distribution of components in a modular fashion as compared to conven- tional configurations where the number of devices increases exponentially as the number of levels of the inverter increase. As all the required voltage levels are generated by using floating capacitor H-bridges, the proposed configuration can be used in a back-to-back converter configuration where the inverter can be interfaced with other dc sources like active front-end convert- ers which enable bidirectional power flow. It can be connected in back-to-back configuration to enable controlled power flow between grids running at different frequencies. In the proposed configuration if any of the devices in any of the H-bridges fail, the faulty H-bridge can be bypassed and the inverter can be operated at reduced number of levels at full power. If a failure of the Vdc/16 H-bridge occurs, the inverter can be operated as a nine-level inverter by bypassing the faulty H-bridge for that particular phase. Similarly, if the Vdc/8 H-bridge fails, the pro- posed inverter can be operated as a five-level inverter. Even if the Vdc/4 H-bridge fails, the inverter can still be operated as a three-level flying capacitor inverter by bypassing the faulty H- bridges at full power level in each case. The proposed inverter can be used in applications like traction and marine drives where reliability is of highest concern and the proposed configuration can operate at full power even during the failure of devices with reduced number of levels.

VII. CONCLUSION

A new 17-level inverter configuration formed by cascading a three-level flying capacitor and three floating capacitor H-bridges has been proposed for the first time. The voltages of each of the capacitors are controlled instantaneously in few switching cycles at all loads and power factors obtaining high performance output voltages and currents. The proposed configuration uses a single dc link and derives the other voltage levels from it. This enables back-to-back converter operation where power can be drawn and supplied to the grid at prescribed power factor. Also, the proposed 17-level inverter has improved reliability. In case of failure of one of the H-bridges, the inverter can still be operated with reduced number of levels supplying full power to the load. This feature enables it to be used in critical applications like marine propulsion and traction where reliability is of highest concern. Another advantage of the proposed configuration is modularity and symmetry in structure which enables the inverter to be extended to more number of phases like five-phase and six-phase configurations with the same control scheme. The proposed inverter is analyzed and its performance is experimentally verified for various modulation indices and load currents by running a three-phase 3-kW squirrel cage induction motor. The stability of the capacitor balancing algorithm has been tested experimentally by suddenly accelerating the motor at no load and observing the capacitor voltages at various load currents.

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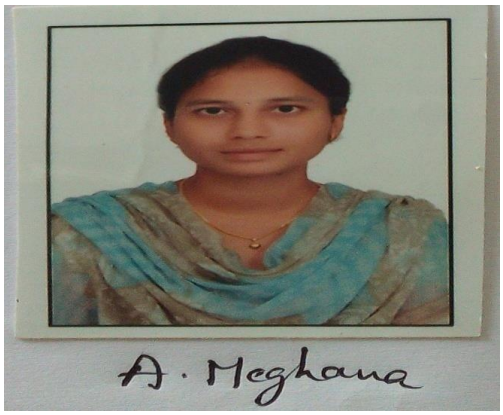

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