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# Fpga Realisation of Multiplierless Fir Filter Architectures

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**Abstract**
In this paper, FPGA realization of MUX based multiplier and odd multiple scheme architectures are proposed for FIR filter and discussed in terms of complexity. In digital filter implementation, the multiplier usage is avoided by using MUX based multiplier and Look Up Table (LUT) based multiplier. These multipliers are used for constructing direct form FIR filters with signed number representation. The two architectures have been implemented using Verilog and synthesized using A1tera Cyclone II EP2C35F672C6. The performance is analyzed for 4,8,16 tap filters. The results show that for a MUX based multiplier architecture occupies '14th area compared with Odd multiple scheme LUT based filters.

Keywords- FIR filter, Look-up Table, Reconfigurable

## .INTRODUCTION

Recently there has been a trend to implement DSP functions using field programmable gate arrays (FPGAs). While application specific integrated circuits (ASICs) are the traditional solution to high performance applications, the high development costs and time-to-market factors prohibit the deployment of such solutions for certain cases. DSP processors offer high programmability, but the sequential execution nature of their architecture can adversely affect their throughput performance. As such, the reason for the rising popularity of the FPGA is due to the balance that FPGAs provide the designer in terms of flexibility, cost, and time-to-market. Digital filter structures, which are extensively used in applications such as speech processing, image and video processing, and telecommunications to name a few, are commonly implemented using FPGAs.

## MOTIVATION OF THE PROJECT:

Multiplication is the key in arithmetic operation and multiplier plays an important role in digital signal Processing. Unfortunately, the major source of power dissipation in digital signal processors is multipliers. In the past decade researchers developed multipliers with the help of CMOS logic which has all the disadvantages as discussed earlier. Therefore the design of multipliers for digital signal processing applications should be efficient while still being able to handle low-power applications. So the proposed work is designed using pass logic principles, which shows improvements over CMOS designs. Pass logic principle based circuits are able to achieve better performance in area, power and speed when implemented in VLSI[1]

### Frequency response

Simple filters are usually defined by their responses to the individual frequency components that constitute the input signal. There are three

different types of responses. A filter's response to different frequencies is characterized as passband, transition band, or stopband. The passband response is the filter's effect on frequency components that are passed through (mostly) unchanged.

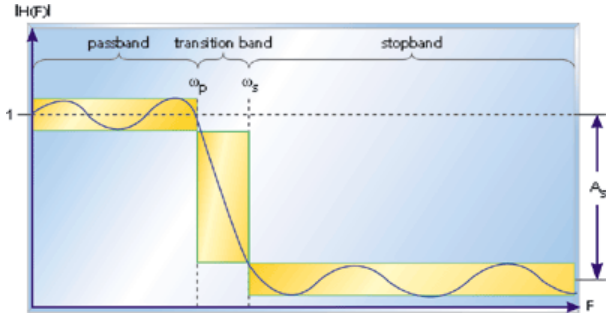



**Figure: The response of a lowpass filter to various input frequencies**

## INTRODUCTION TO VLSI DOMAIN

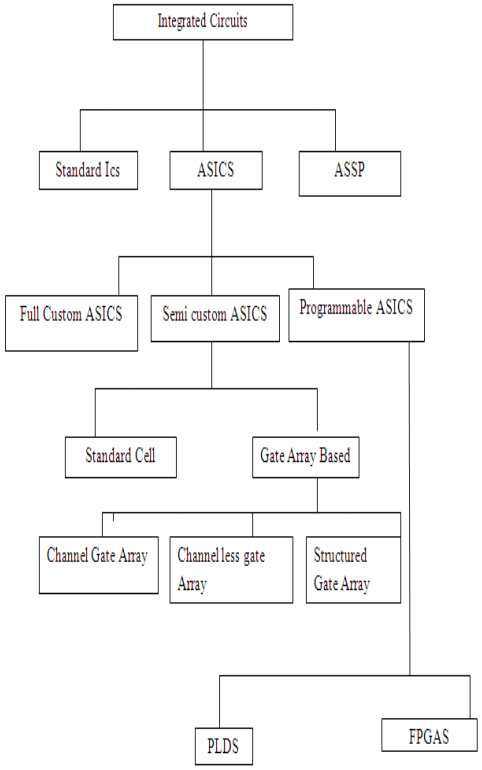
**Very-large-scale integration** (**VLSI**) is the process of creating integrated circuits by combining thousands of transistors into a single chip. VLSI began in the 1970s when complex semiconductor and communication technologies were being developed. The microprocessor is a VLSI device. VLSI began in the 1970s when complex semiconductor and communication technologies were being developed. The microprocessor is a VLSI device. The term is no longer as common as it once was, as chips have increased in complexity into the hundreds of millions of transistors. This is the field which involves packing more and more logic devices to smaller and smaller areas. VLSI circuits can now be put into a small space few millimeters across VLSI circuits are everywhere our computer, our car, our brand new state-of-the-art digital camera, the cell-phones

### Various Levels of Integrations

Over time, millions, and today billions of transistors could be placed on one chip, and to make a good design became a task to be planned thoroughly. In the early days of integrated circuits, only a few transistors could be placed on a chip as the scale used was large because of the contemporary technology and manufacturing yields were low by today's standards. As the degree of integration was small, the design was done easily. Over time, millions, and today billions of transistors could be placed on one chip, and to make a good design became a task to be planned thoroughly.

### VLSI Design Process

VLSI technology thus provides a platform for developing systems for various applications. The integrated circuits so developed can be further classified as shown in below figure 2.1



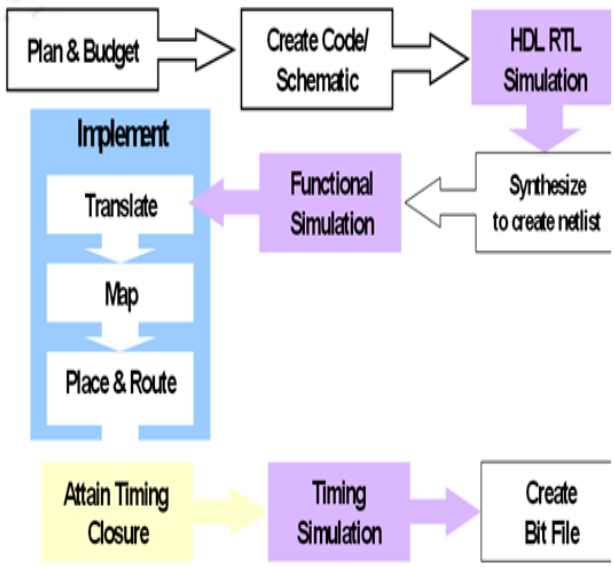

### ASIC Design Flow

An Application Specific Integrated Circuit (ASIC) is a semiconductor device designed especially for a particular customer (versus a

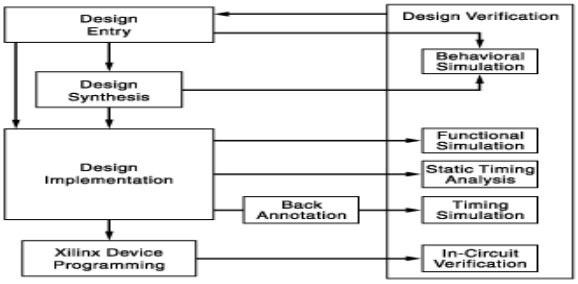
Standard Product, which is designed for general Use by any customer) The three major categories of ASIC Technology are:

- Gate Array-Based
- Standard Cell-Based
- Full custom

**Xilinx Design Flow**




The AISE® design flow comprises the following steps: design entry, design synthesis, design implementation, and Xilinx® device programming. Design verification, which includes both functional verification and timing verification, takes places at different points during the design flow See fig.




**FPGA Design Flow**

## PROJECT IMPLEMENTATION

Finite Impulse Response (FIR) digital filter is widely used as a basic block in signal and image processing applications. The number of multiply-accumulate (MAC) operations required per filter output increases linearly with the order of filter, but implementation of higher order filters in real-time is another challenging task. Recently with the advent of software defined radio (SDR), the research has been concentrated on realization of FIR filters mainly due to its high flexibility and low complexity.

The digit-based reconfigurable architecture presented in provides a flexible and low power solution with a wide range of precision and tap length of FIR filters. Conventionally, the FIR filters are designed based on programmable multiply-accumulate [MAC] architecture and systolic architecture. The performances of the designs are analyzed in terms of hardware complexity, power consumption and throughput. In the programmable MAC architectures consume low power with reduced supply voltage and it requires large area. In even though systolic based architecture reduces the complexity, it increases the latency when the order of the filter increases. Several attempts have been made and it continued to develop low-complexity dedicated VLSI systems for these filters. There are several issues in the hardware implementation of Digital

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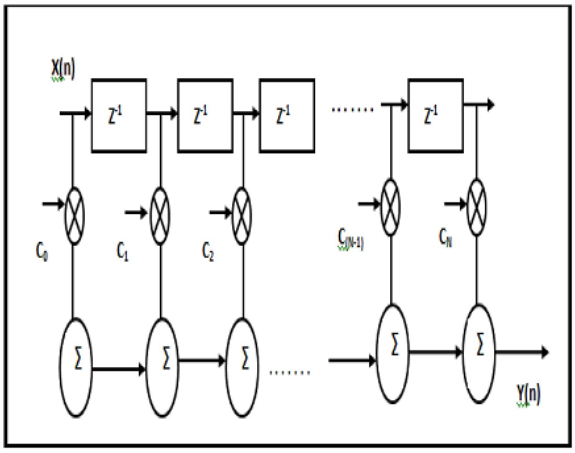
filters. The direct implementation of N-tap FIR filters which requires N MAC operations are too expensive to implement in hardware due to its logic complexity and area requirement.

**MULT1PLIER LESS STRUCTURES BASED FOR FIR FILTER**




an implementation of N tap FIR filter with the usage of three elements namely adders, multipliers and delay elements.Let X(n) and Y(n) be the input and output sequences of the FIR filter respectively. Consider an N-tap FIR filter that can be formulated as

$$Y(n)=\sum_{k=0}^{N-1} h_k X(n-k)$$

# ADDERSINTRODUCTION

**Binary Adders**

In this set of slides, we present the two basic types of adders:

1. Half adders
2. Full adders.

Each type of adder functions to add two binary bits. In order to understand the functioning of either of these circuits, we must speak of arithmetic in terms that I learned in the second grade. In the first grade, I learned by "plus tables", specifically the sum of adding any two one digit numbers: 2 + 2 = 4, 2 + 3 = 5, etc.

In the second grade, I learned how to add numbers that had more than one digit each 23 + 34 = 57, but 23 + 38 = 61. This adaptation of addition to multiple digit numbers gives rise to the full adder. The half adder takes two single bit binary numbers and produces a sum and a carry–out, called "carry". Here is the truth table 3.1 description of a half adder. We denote the sum A + B.

**Ripple-carry adder**

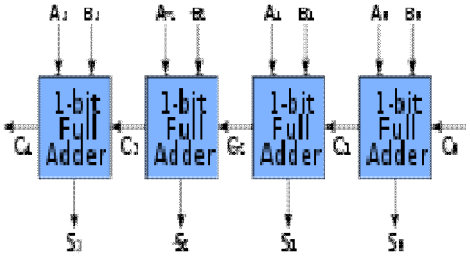



**Fig 3.3: 4-bit Ripple-carry adder with logic gates**

It is possible to create a logical circuit using multiple full adders to add N-bit numbers. Each full adder inputs a $C_{in}$, which is the $C_{out}$ of the previous adder. This kind of adder is called a ripple-carry adder, since each carry bit "ripples" to the next full adder. Shown in fig 3.3, 4-bit adder with logic gates, Note that the first (and only the first) full adder may be replaced by a half adder.

# PROJECTMODIFICATION

**D**ESIGN of area- and power-efficient high-speed data path logic systems are one of the most substantial areas of research in VLSI system design. In digital adders, the speed of addition is limited by the time required to propagate a carry through the adder. The sum for each bit position in an elementary

adder is generated sequentially only after the previous bit position has been summed and a carry propagated into the next position.

The CSLA is used in many computational systems to alleviate the problem of carry propagation delay by independently generating multiple carries and then select a carry to generate the sum . However, the CSLA is not area efficient because it uses multiple pairs of Ripple Carry Adders (RCA) to generate partial sum and carry by considering carry input 0 and 1, then the final sum and carry are selected by the multiplexers (mux). The basic idea of this work is to use Binary to Excess-1 Converter (BEC) instead of RCA with 1 in the regular CSLA to achieve lower area and power consumption.

The main advantage of this BEC logic comes from the lesser number of logic gates than the 2-bit Full Adder (FA) structure. The details of the BEC logic are discussed. This brief is structured as follows. The delay and area evaluation methodology of the basic adder blocks. SQRT CSLA has been chosen for comparison with the proposed design as it has a more balanced delay, and requires lower power and area.

Addition is the most common and often used arithmetic operation on microprocessor, digital signal processor, especially digital computers. Also, it serves as a building block for synthesis all other arithmetic operations. Therefore, regarding the efficient implementation of an arithmetic unit, the binary adder structures become a very critical hardware unit. In any book on computer arithmetic, someone looks that there exists a large number of different circuit architectures with different performance characteristics and widely used in the practice. Although many researches dealing with the binary adder structures have been done, the studies based on their comparative performance analysis are only a few.

**CARRY SELECT ADDERS**

In Carry select adder scheme, blocks of bits are added in two ways: one assuning a carry-in of 0 and the other with a carry-in of 1.This results in two precomputed sum and carry-out signal pairs **(s0i-1:k , c0i ; s1i-1:k , c1i) ,** later as the block's true carry-in (**ck**) becomes known , the correct signal pairs are selected. Generally multiplexers are used to propagate carries.

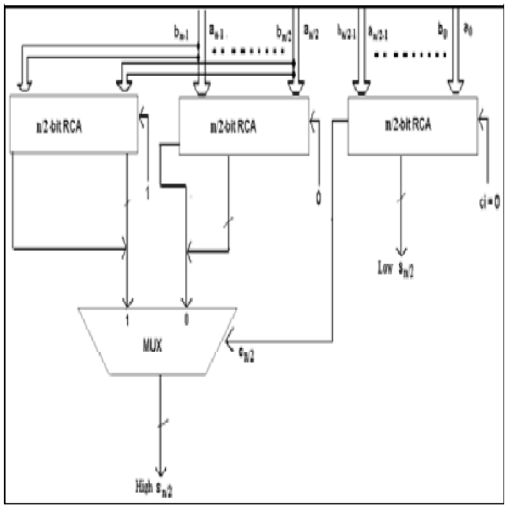



FIGURE 2.2 A Carry Select Adder with 1 level using n/2- bit RCA

**ANALYSIS OF ADDERS**

In our project we compared 3- different adders **Ripple Carry Adders**, **Carry Select Adders** and **the Carry Look Ahead Adders**. The basic purpose of our experiment was to know the time and power trade-offs between different adders whish will give us a clear picture of which adder suits best in which type of situation during design process. Hence below we present both the theoretical and practical comparisons of all the three adders whish were taken into consideration.

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**DELAY AND AREA EVALUATION METHODOLOGY OF THE BASICADDER BLOCKS**

The AND, OR, and Inverter (AOI) implementation of an XOR gate is shown in Fig. 1. The gates between the dotted lines are performing the operations in parallel and the numeric representation of each gate indicates the delay contributed by that gate. The delay and area evaluation methodology considers all gates to be made up of AND, OR, and Inverter, each having delay equal to 1 unit and area equal to 1 unit.

We then add up the number of gates in the longest path of a logic block that contributes to the maximum delay. The area evaluation is done by counting the total number of AOI gates required for each logic block. Based on this approach, the CSLA adder blocks of 2:1 mux, Half Adder (HA), and FA are evaluated and listed

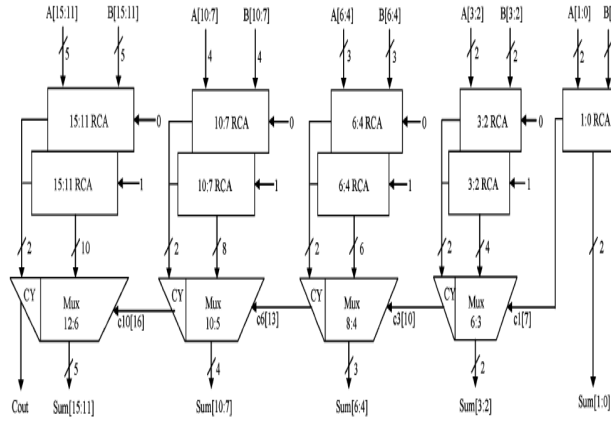


Fig. 4. Regular 16-b SQRT CSLA.

**TOOLS AND HDL USED**

An HDL provides the framework for the complete logical design of the ASIC. All the activities coming under the purview of an HDL are shown enclosed in bold dotted lines . Verilog and VHDL are the two most commonly used HDLs today. Both have constructs with which the design can be fully described at all the levels. There are additional constructs available to facilitate setting up of the test bench, spelling out test vectors for them and "observing" the outputs from the designed unit

**DIFFERENT VERSIONS OF VERILOG**

- Verilog-95
- Verilog 2001
- Verilog 2005
- SystemVerilog

**SOFTWARE TOOL-XILINX:**

Xilinx ISE is a software tool produced by Xilinx for synthesis and analysis of HDL designs, which enables the developer to synthesize ("compile") their designs, perform timing analysis, examine RTL diagrams, simulate a design's reaction to different stimuli, and configure the target device with the programmer. Xilinx was founded in 1984 by two semiconductor engineers, Ross Freeman and Bernard Vonderschmitt, who were both working for integrated circuit and solid-state device manufacturer Zilog Corp.

While working for Zilog, Freeman wanted to create chips that acted like a blank tape, allowing users to program the technology themselves. At the time, the concept was paradigm-changing. "The concept required lots of transistors and, at that time, transistors were considered extremely precious – people thought that Ross's idea was pretty far out", said Xilinx Fellow Bill Carter, who when hired in 1984 as the first IC designer was the company's eighth employee.

Xilinx is a software tool, which is used to run the programs in VHDL language. It has various versions like Xilinx 92.1, Xilinx 10.1, Xilinx 10.5 etc. Xilinx has various pre-defined libraries ,packages.

**HARDWARE TOOLS**

A field-programmable gate array (FPGA) is a semiconductor device that can be configured by the customer or designer after manufacturing—hence the name "field-programmable". FPGAs are programmed using a logic circuit diagram or a source code in a hardware description language (HDL) to specify how the chip will work. They can be used to implement any logical function that an application-specific integrated circuit (ASIC) could perform, but the ability to update the functionality after shipping offers advantages for many applications.

FPGAs contain programmable logic components called "logic blocks", and a hierarchy of reconfigurable interconnects that allow the blocks to be "wired together"—somewhat like a one-chip programmable breadboard. Logic blocks can be configured to perform complex combinational functions, or merely simple logic gates like AND and XOR. In most FPGAs, the logic blocks also include memory elements, which may be simple flip-flops or more complete blocks of memory.

## CONCLUSION

In this paper an efficient Low complexity based FIR filter architecture usillg MUX based multiplier and odd multiple scheme have been discussed and implemented effectively. The results of FIR filter architectures are analyzed and compared with respect to area and power. It is found that odd multiple scheme occupies twice the area compared to MUX based FIR Filter architecture. Thus the proposed FIR filter architecture achieves low area and more flexibility and hence it is wellsuitable for VLSI implementation.

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