International Journal of Research
Available at https://edupediapublications.org/journals
p-ISSN: 2348-6848
e-ISSN: 2348-795X
Volume 03 Issue 14
October 2016

Analysis and Design of Grid Synchronization for DGS under Critical Fault Conditions

[#1] **G.Jaswanth**, M.Tech Student
#2 **M.DILIP KUMAR,** Associate Professor& HOD

Department of EEE
K.V.SUBBA REDDY COLLEGE OF ENGINEERING AND TECHNOLOGY, KURNOOL,A.P,INDIA

ABSTRACT: Grid synchronization algorithms are of great importance in the control of grid-connected power converters, as fast and accurate detection of the grid voltage parameters is crucial in order to implement stable control strategies under generic grid conditions. This paper presents a new grid synchronization method for three-phase three-wire networks, namely dual second-order generalized integrator (SOGI) frequency-locked loop. The method is based on two adaptive filters, implemented by using a SOGI on the stationary αβ reference frame, and it is able to perform an excellent estimation of the instantaneous symmetrical components of the grid voltage under unbalanced and distorted grid conditions. This paper analyzes the synchronization capability of three advanced synchronization systems: the decoupled double synchronous reference frame phase-locked loop (PLL), the dual second order generalized integrator PLL, and the three-phase enhanced PLL, designed to work under such conditions. Although other systems based on frequency-locked loops have also been developed, PLLs have been chosen due to their link with dq0 controllers. In the following, the different algorithms will be presented and discretized, and their performance will be tested in an experimental setup controlled in order to evaluate their accuracy and implementation features.

Index Terms—Electric variable measurements, electrical engineering, frequency estimation, frequency-locked loops, harmonic analysis, monitoring, synchronization.

INTRODUCTION: The high penetration of renewable energy sources such as wind power and photovoltaic, experienced in the last decades is a good example, as both generation systems are connected to the grid by means of power electronics- based power processors, that should not only control the power delivered to the network, but also contribute to the grid stability, supporting the grid services voltage/frequency under generic conditions, even under grid faults. One of the most important issues in the connection of power converters to the grid is the synchronization with the grid voltage at the point of common coupling (PCC) .Although thegrid voltage waveforms are sinusoidal and balanced under regular operating conditions, they can easily become unbalanced and distorted due to the effect of grid faults and nonlinear loads. Under these conditions, grid-connected converters should be properly synchronized with the grid in order to stay actively connected, supporting the grid services and keeping the generation up and running .Actually, these are currently former requirements in all grid codes (GCs) for the connection of distributed generation systems to the network, where the criteria for the injection of active and reactive power during either balanced or unbalanced grid fault conditions are also provided. Despite the fact that the dynamics of grid synchronization are not established in the GC, requirements are needed in order to achieve a certain dynamical response in the synchronization. Algorithms based on the implementation of phase locked loops (PLL) have traditionally been used for synchronizing the control system of power converters with the grid voltage. In Fig. 1, the layout of a generic control structure for a three phase power converter connected to the grid is shown. As depicted in Fig. 1, the grid synchronisation block is responsible for estimating the magnitude frequency and phase angle of the positive- and the negative- sequence components of the grid voltage, v±, ω, and θ ±, respectively. These estimated values are later used at the current controller block, which settles finally the voltage waveform to be modulated v∗ c as well as at the reference generator, responsible of determining the current reference to be tracked. This last block will vary if the power converter is acting as an active filter, a STATCOM, or a power processor belonging to a power generation plant. In three-phase systems, a PLL based on a synchronous reference frame (SRF-PLL) has become a conventional grid synchronization technique. Nevertheless, the response of the SRF-PLL is unacceptably deficient when the grid voltage is unbalanced due to the appearance of a negative-sequence component that the SRF-PLL is unable to process properly. In the actual grid code

requirements (GCRs), special constraints for the operation of such plants under grid voltage fault conditions have gained a great importance. These requirements determine the fault boundaries among those through which a grid-connected generation system shall remain connected to the network, giving rise to specific voltage profiles that specify the depth and clearance time of the voltage sags that they must withstand. Such requirements are known as low voltage ride through (LVRT) and are described by a voltage versus time characteristic [7]. Although the LVRT requirements in the different standards are very different, as shown in [8], the first issue that generation systems must afford when voltage sag occurs is the limitation of their transient response, in order to avoid its protective disconnection from the network. This is the case, for instance, of fixed speed wind turbines based on squirrel cage induction generators, where the voltage drop in the stator windings can conduct the generator to an over speed tripping, as shown in [9]. Likewise, variable speed wind power systems may lose controllability in the injection of active/reactive power due to the disconnection of the rotor side converter under such conditions [10], [11]. Likewise, PV systems would also be affected by the same lack of current controllability. Solutions based on the development of auxiliary systems, such as STATCOMs and dynamic voltage regulators (DVRs), have played a decisive role in enhancing the fault ride through (FRT) capability of distributed generation systems, as demonstrated in [12]–[16]. Likewise, advanced control functionalities for the power converters have also been proposed [17], [18]. In any case, a fast detection of the fault contributes to improving the effects of these solutions; therefore, the synchronization algorithms are crucial. In certain countries, the TSOs also provide the active/reactive power pattern to be injected into the network during voltage sag; this is the case for the German E-on [2] and the Spanish Red Electrical Espanola (REE) [3]. This trend has been followed by the rest of the TSOs; moreover, it is believed that this operation requirement will be extended, and specific demands for balanced and unbalanced sags will arise in the following versions of the grid codes worldwide. Regarding the operation of the distributed generation systems under balanced and unbalanced fault conditions, relevant contributions, such as [20]–[29], can be found in the literature. These solutions are based on advanced control systems that need to have accurate information of the grid voltage variables in order to work properly, something that has prompted the importance of grid synchronization algorithms. In power systems, the synchronous reference frame PLL (SRF PLL) is the most extended technique for synchronizing with three-phase systems [30]. Nevertheless, despite the fact that the performance of SRF PLL is satisfactory under balanced conditions, its response can be inadequate under unbalanced, faulty, or distorted conditions [31]–[33]. In this paper, three improved and advanced grid synchronization systems are studied and evaluated: the decoupled double synchronous reference frame PLL (DDSRF PLL) [34], the dual second order generalized integrator PLL (DSOGI PLL), [35] and the three-phase enhanced PLL (3phEPLL) [36]. Their performance, computational cost, and reliability of the amplitude and phase detection of the positive sequence of the voltage, under unbalanced and distorted situations, have been evaluated according to experimental grid fault patterns extracted from [37] and [38], which have been reproduced in a real scaled electrical network.

DESCRIPTION OF THE THREE SYNCHRONIZATION SYSTEMS:

Many of the positive sequence detection algorithms are based on synchronous reference frame PLL's (SRF PLL) [32]. Despite having a good response under balanced conditions, their performance become insufficient in unbalanced faulty grids (95% of cases) and their good operation is highly conditioned to the frequency stability, something incompatible with the idea of a robust synchronization system. Many authors have been discussing about different advanced models, able to overcome the problems of the classical PLL, by means of building frequency, and amplitude adaptive structures, able to deal with unbalanced, faulty and harmonic polluted grids. In the framework of these topologies we could find the three PLLs discussed in this paper.

A. Decoupled Double synchronous reference frame PLL (DDSRF PLL)

The DDSRF-PLL, published in [34], [41], stems from improving the conventional SRF-PLL. This synchronization system exploits two synchronous reference frames rotating at the fundamental utility frequency, one counter-clockwise and another one clockwise, in order to achieve an accurate detection of the positive and negative sequence components of the grid voltage vector when it is affected by unbalanced grid faults. The diagram of the DDSRF-PLL is shown in Fig.1. When the three-phase grid voltage is unbalanced, the fundamental positive-sequence voltage vector appears as a DC voltage on the 1 dq+ axes of the

positive-sequence SRF and as ac voltages at twice the fundamental utility frequency on the 1 dq– axes of the negative-sequence SRF. On the contrary, the negative-sequence voltage vector will cause a dc component on the negative-sequence SRF and an ac oscillation on the positive-sequence SRF. Since the amplitude of the oscillation on the positive-sequence SRF matches to the DC level on the negative-sequence SRF, and vice versa, a decoupling network is applied to signals on the dq positive/negative SRF axes in order to cancel out such ac oscillations. Low-pass filters in Fig.1 are in charge of extracting the DC component from the signal on the decoupled SRFs axes. These DC components collect the information about the amplitude and phase-angle of the positive- and negative-sequence components of the grid voltage vector. The loop controller of the DDSRF-PLL works on the decoupled q-axis signal of the positive-sequence SRF (1 * q v +). This signal is free of ac components due to the effect of the decoupling cells and the bandwidth of the loop controller can be consequently increased.

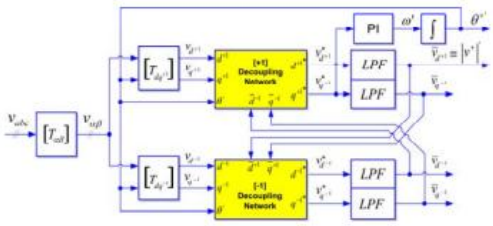

Fig. 1. DDSRF PLL block diagram

B. Dual SOGI PLL (DSOGI PLL)

The operating principle of the DSOGI-PLL for estimating the positive and negative-sequence components of the grid voltage vectors is based on using the instantaneous symmetrical components (ISC) method on the αβ stationary reference frame, as explained in [35]. The diagram of the DSOGI-PLL is shown in Fig.4. As it can be noticed in this figure, the ISC method is implemented by the positive sequence calculation block (PSC).To apply the ISC method, it is necessary to have a set of signals v vα–β representing the input voltage vector on the αβ stationary reference frame together with another set of signals qv qvα–β which are in-quadrature and lagged respect to v vα–β . In the DSOGI-PLL, these signals to be supplied to the ISC method are obtained by using a dual second order generalized integrator (DSOGI) which is an adaptive band pass filter based on the generalized integrator concept [42]. The DSOGI provides at its output four signals, namely, ' vα and ' vβ which are filtered versions of vα and vβ , respectively, and ' qvα and ' qvβ which are the in-quadrature versions of ' vα and ' vβ . A conventional synchronous reference frame phase-locked loop (SRF-PLL) is applied on the estimated positive-sequence voltage vector, vαβ+ , to make this synchronization system frequency adaptive. In particular, the vαβ+ voltage vector is translated to the rotating SRF and the signal on the q axis, q v+ , is applied at the input of the loop controller. As a consequence, the fundamental grid frequency (ω') and the phase-angle of the positive-sequence voltage vector ('θ+) are estimated by this loop. The estimated frequency for the fundamental grid component is feedback to adapt the centre frequency of the DSOGI.

C. Three phase enhanced PLL (3phEPLL PLL)

The enhanced phase locked loop (EPLL) is a synchronization system that had proven to perform good results in one-phase synchronization systems [43]. An EPLL is essentially an adaptive band pass filter, able to adjust the cut off frequency in function of the input signal. Its structure was later adapted for the three phase case [44], in order to detect the positive sequence vector of a three phase signals, obtaining the 3phEPLL PLL that is represented in Fig.3. In this case, each input phase voltage is being processed independently by an EPLL. This block filters the input signal and generates two sinusoidal outputs of the same amplitude and frequency, ' n v and ' n jv , being the second one 90º leaded with respect ' n v . The resulting signals constitute the input for the computational unit. This block implements the ISC method on the 'abc' stationary reference frame for extracting the positive-sequence voltage component, abc v+ .

DISCRETE IMPLEMENTATION:

The reliability of a discretized system depends upon the approximation made to their continuous equations [45]. Some methods, as the Forward Euler, the Backward Euler and the Tustin (Trapezoidal) numerical integration offer a good performance when used for discretizing other synchronization systems, as shown in [46]-[47], however the Euler methodscan be inadequate under certain conditions, due to the need of introducing additional sample delays [48]. Therefore, and according to the specific needs of the presented topologies, in this section the discrete representation of each PLL will be described

independently. In order to facilitate the comprehension of the process the different building blocks that appear at Fig.1, Fig.2 and Fig.3 will be referenced. The values of the different parameters used in each case are summarized in an appendix at the end of this paper.

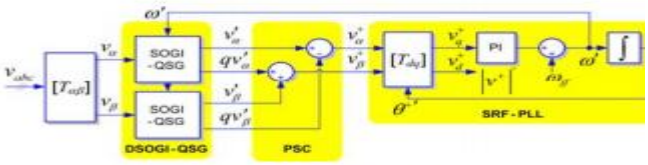

Fig. 2. DSOGI PLL block diagram

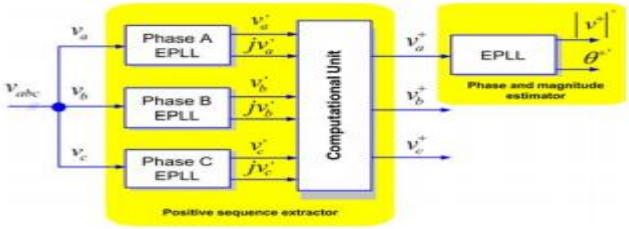

Fig. 3. 3ph EPLL PLL block diagram

A. DDSRF PLL discretization

The discrete model of this PLL can be easily obtained, since the continuous representation of several parts does not change in the discrete domain. This is obviously the case of the transformation blocks: Tαβ , 1 dq T + and 1 dqT – , whose description can be found in previous papers and general scope bibliography [49].

1. Positive and negative sequence decoupling networks

The decoupling network constitutes one of the most important contributions of this synchronization tool. The discrete equations of these blocks are shown in (1), being almost the same as in the continuous domain [41]. It is just necessary to consider the one sample delay of θ ' , 1 d v – , 1 q v – , 1 d v + and 1 q v + in order to avoid algebraic loops.

2. Phase and magnitude estimator discretization

In the DDSRF-PLL the decoupling network appears embedded in the classical SRF-PLL loop (Fig.4). However this does not affect the discretization of the phase and magnitude estimator, since 1 * d v + and 1 * q v + act as the input of this block.

$$\begin{bmatrix} v^{+}_{d^{+1}}[n+1] \\ v^{+}_{q^{+1}}[n+1] \end{bmatrix} = \begin{bmatrix} 1 & 0 \\ 0 & 1 \end{bmatrix} \cdot \begin{bmatrix} v_{d^{+1}}[n+1] \\ v_{q^{+1}}[n+1] \end{bmatrix} + \begin{bmatrix} -\cos(2\theta'[n]) & -\sin(2\theta'[n]) \\ \sin(2\theta'[n]) & -\cos(2\theta'[n]) \end{bmatrix} \cdot \begin{bmatrix} \bar{v}_{d^{+1}}[n] \\ \bar{v}_{q^{+1}}[n] \end{bmatrix}$$
$$\begin{bmatrix} v^{-}_{d^{-1}}[n+1] \\ v^{-}_{q^{-1}}[n+1] \end{bmatrix} = \begin{bmatrix} 1 & 0 \\ 0 & 1 \end{bmatrix} \cdot \begin{bmatrix} v_{d^{-1}}[n+1] \\ v_{q^{-1}}[n+1] \end{bmatrix} + \begin{bmatrix} -\cos(-2\theta'[n]) & -\sin(-2\theta'[n]) \\ \sin(-2\theta'[n]) & -\cos(-2\theta'[n]) \end{bmatrix} \cdot \begin{bmatrix} \bar{v}_{d^{-1}}[n] \\ \bar{v}_{q^{-1}}[n] \end{bmatrix} \quad (1)$$

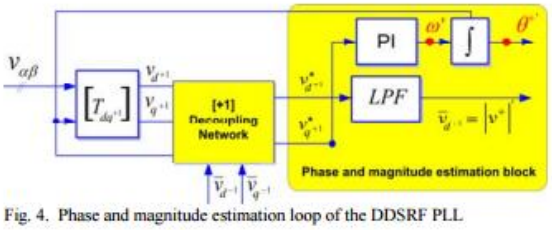

Fig. 4. Phase and magnitude estimation loop of the DDSRF PLL

The discrete controller and the integrator can be build using a backward numerical approximation. The frequency and phase can be then represented in the z-domain (2) considering 1 * q v + as the error to be minimized. In this equation a feed forward of the nominal frequency is given by means of ωff .

3. Low pass filter block discretization

The amplitude of the dq positive and negative sequence components are the outputs of the decoupling networks. However, four IIR low pass filters extract the ripple from each sequence estimation, in order to reinforce the performance of the PLL in case of harmonic pollution. A first order filter with a cut off frequency, ωf , equal to the half of the grid one was originally proposed in [41], hence the same transfer function has been implemented in this work for evaluation purposes in

$$y[n] = \frac{1}{T_s \cdot \omega_f + 1} \cdot x[n] + \frac{T_s \cdot \omega_f}{T_s \cdot \omega_f + 1} \cdot u[n]$$
$$x[n+1] = y[n] \quad (4)$$

B. DSOGI PLL discretization

1. DSOGI-QSG block discretization

As it was previously mentioned in §II, the DSOGI based quadrature signal generator of Fig. 4 consist of two independent and decoupled SOGIs. Therefore each SOGI based quadrature signal generator can be discretized individually, facilitating thus its mathematical description. In

Fig.5 the block diagram of the SOGI implemented in this work is shown.

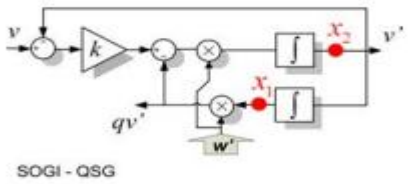

Fig.5. Quadrature signal generator based on a second order generalized integrator (SOGI-QSG)

This QSG is a linear system itself; therefore a discrete representation can be systematically obtained if the continuous state space is previously deducted. The equations of the SOGI state space appear detailed in (5) where v constitutes the input while v' and qv' are the two in-quadrature output signals.

$$\left.\begin{aligned}\dot{x}_n &= A\cdot x_n + B\cdot v\\ y_n &= C\cdot x_n\end{aligned}\right\};\quad x_n=\begin{bmatrix}x_1\\x_2\end{bmatrix} y_n=\begin{bmatrix}v'\\qv'\end{bmatrix}$$
$$A=\begin{bmatrix}0 & 1\\ -\omega'^2 & -k\cdot\omega'\end{bmatrix} B=\begin{bmatrix}0\\k\cdot\omega'\end{bmatrix} C=\begin{bmatrix}0 & 1\\ \omega' & 0\end{bmatrix} \quad (5)$$

The discretization of this system has been performed using trapezoidal integrators, as they offer a better detection of the phase, something important when dealing with sinusoidal signals [22]. The symbolic values of each matrix of (7) are detailed in (6), where Ts is the sampling time of the discrete

$$A'=\gamma\begin{bmatrix}4+2T_s\cdot k\cdot\omega'[n]-T_s^2\cdot\omega'[n]^2 & 4T_s\\ -4T_s\cdot\omega'[n]^2 & 4-2T_s\cdot k\cdot\omega'[n]-T_s^2\cdot\omega'[n]^2\end{bmatrix};B'=\gamma\begin{bmatrix}2T_s\cdot k\cdot\omega'[n]\\ 4k\cdot\omega'[n]\end{bmatrix}$$
$$C'=\gamma\begin{bmatrix}-2T_s^2\cdot\omega'[n]^2 & 4T_s\\ 2T_s\cdot\omega'[n]\cdot(2+T_s\cdot k\cdot\omega'[n]) & 2T_s^2\cdot\omega'[n]\end{bmatrix};D'=\gamma\begin{bmatrix}2T_s\cdot k\cdot\omega'[n]\\ k\cdot T_s^2\cdot\omega'[n]^2\end{bmatrix} \quad (6)$$
$$\gamma=\frac{1}{4+2\cdot T_s\cdot k\cdot\omega'[n]+T_s^2\cdot\omega'[n]^2}$$

System whiles the value of ω '[n] and the k constant come from the estimation made at the SRF-PLL block in each computation step, and the SOGI gain respectively.

2. **SRF PLL discretization**

The frequency and phase detection are obtained by means of the SRF PLL shown in Fig.6 The discretization of the controller and the integrator has been performed, in this case, using the backward numerical approximation.

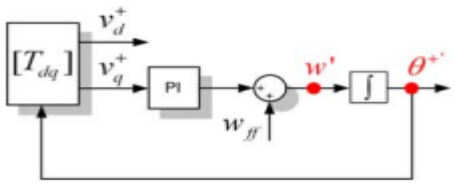

Fig. 6. State variables of the SRF PLL block

C.**3phEPLL PLL discretization**

This three-phase grid synchronization system exploits the EPLL as a quadrature signal generator. An independent EPLL is used for processing each one of the three phase voltages. The same EPLL structure is applied again to detect the magnitude and phase of the positive-sequence voltage component.

1. **QSG block - EPLL discretization**

The block diagram of the EPLL implemented in this paper is presented in Fig.7.

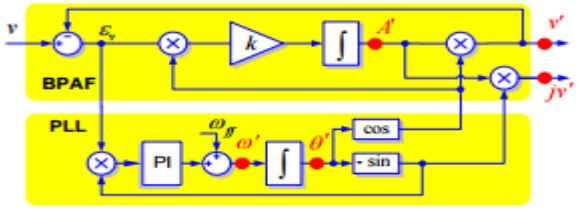

Fig.7. QSG based on an EPLL structure

Simulation results:

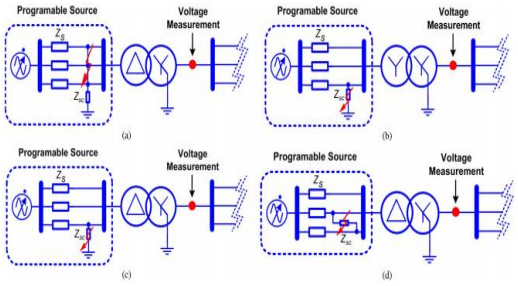

Fig8: Generation of grid voltage sags in the experimental setup. (a) Generation of a Type "A" voltage sag. (b) Generation of a Type "B" voltage sag. (c) Generation of a Type "C" voltage sag. (d) Generation of Type "D" voltage sag.

Behaviour in Case of Voltage Sags

1) Type "A" Sag Test: This kind of voltage sag appears as a consequence of three-phase faults that give rise to high short circuit currents and, hence, to a balanced voltage drop in the network. As Fig. 12(e) and (i) shows, the DDSRF PLL and the DSOGI PLL produce a good response, as both

systems achieve a very fast detection (20 ms) of the positive-sequence components (less than two cycles). The response of the 3phEPLL, depicted in Fig. 12(m), also shows a good response, but with a larger transient in the positive-sequence estimation.

2) **Type "B" Sag Test:** This kind of fault permits analyzing the behaviour of the PLLs under test in the presence of zero sequence components at the input. The Clarke transformation used in DSOGI PLL and DDSRF PLL to extract the αβ components enhances the response of this synchronization system when the faulty grid voltage presents zero-sequence components. Their responses, as shown in Fig. 12(f) and (j), are fast and accurate. On the other hand, the 3phEPLL does not cancel out the zero-sequence component from the input voltage, something which may affect the dynamics of the positive-sequence estimation loop.

3**) Type "C" and "D" Sag Tests:** These kinds of sags appear due to phase-to-ground and phase-to-phase short circuits at the primary winding of the transformer, respectively, as shown in Table I. In a distribution network, these distortions are more common than the previous ones, as they are the typical grid faults caused by lightning storms.

B. Frequency Changes (50–60 Hz)

In this experiment, similar results are obtained with the DDSRF and the DSOGI PLL, as can be seen in Fig. 13(a)–(d). The low overshooting in the amplitude estimation in both cases [see Fig. 13(a) and (c)] assists the good phase and frequency detection, as shown in Fig. 13(b) and (d). Likewise, the response of the 3phEPLL shows a similar settling time, as shown in Fig. 13(e); however, the initial oscillation in theamplitude estimation of the voltage contributes to slightly delay the stabilization of the frequency magnitude, as displayed.

B. Polluted Grids (THD = 8%)

The 3phEPLL behaves as a band pass filter for the input signal, something that permits filtering the input without adding extra filters. As can be seen in Fig. 14(d), the 3phEPLL offers the best filtering capability among the PLLs under test, with a clear and undistorted estimation of the magnitude and phase of the input.

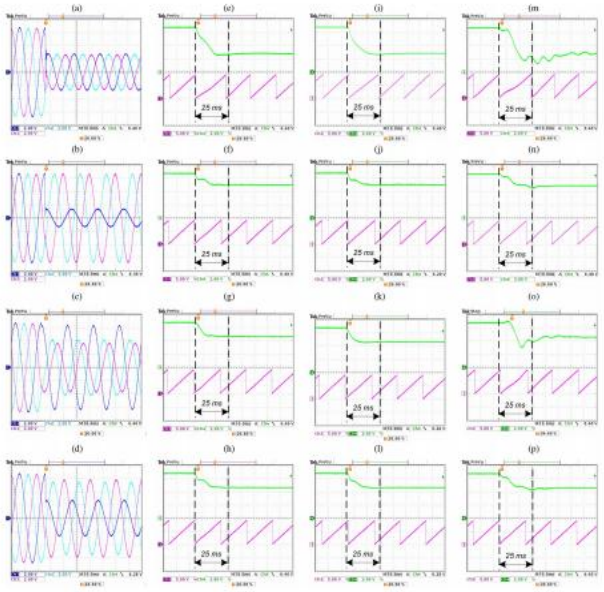

Fig9: Amplitude and phase estimation of the three tested PLLs in case of four types of sag. (a)–(d) Input signal (V). (e)–(h) Amplitude (V) and phase (rad) detection for the DSRF PLL. (i)–(l) Amplitude (V) and phase (rad) detection for the DSOGI PL. (m)–(o) Amplitude (V) and phase (rad) detection for the 3phEPLL. Scaling factors: Amplitude = 1 : 150; phase =1:7.

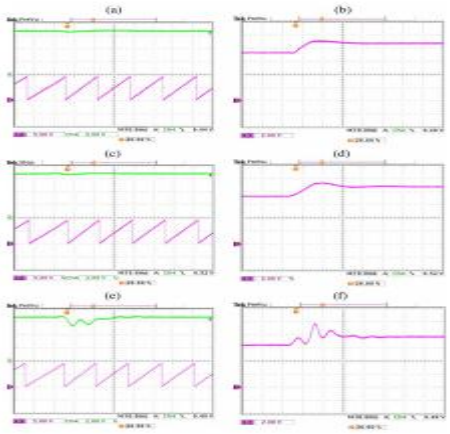

Fig10: Amplitude, phase, and frequency estimation of the three tested PLLs in a frequency jump. (a) and (b) Amplitude (V), phase (rad), and frequency detection for the DDSRF PLL. (c) and (d) Amplitude (V), phase (rad), and frequency detection for the DSOGI PLL. (e) and (f) Amplitude (V), phase (rad), and frequency detection for the 3phEPLL. Scaling factors: Amplitude =1: 150, phase =1:7, and frequency 1 : 70

CONCLUSION:

This paper studied the behaviour of three advanced grid synchronization systems. Their structures have been presented, and their discrete algorithms have been detailed. Moreover, their performances have been tested in an experimental setup, where these algorithms have been digitally implemented in a commercial DSP, allowing proof of their satisfactory response under balanced and distorted grid conditions. The DDSRF PLL and the

DSOGI PLL allow estimating the ISCs of a three-phase system working in the αβ reference frame, while the 3phEPLL uses the "abc" reference frame, thus working with three variables. As has been shown, this feature simplifies the structure of the DSOGI PLL and the DDSRF PLL, which allows reducing the computational burden, as compared to the 3phEPLL, without affecting its performance. The synchronization capability of the three PLLs under test has been shown to be fast and accurate under faulty scenarios, allowing the detection of the positive sequence of the voltage in 20–25 ms in all cases; however, the simpler structure of the DDSRF and the DSOGI affords an easier tuning of their control parameters and, therefore, a more accurate control of their transient response. The immunity of the analyzed PLLs in the possibility of a polluted network is better when using the 3phEPLL and the DDSRF, due to their greater band pass and low-pass filtering capabilities. Although the DSOGI also gives rise to reasonably good results, due to its inherent band pass filtering structure, its response is more affected by harmonics. Although all three have been shown to be appropriate for synchronizing with the network voltage in distributed power generation applications, mainly PV and wind power, the lower computational cost of the DDSRF PLL and the DSOGI PLL, together with their robust estimation of the voltage parameters, offers a better trade off between the presented systems, making them particularly suitable for wind power applications.

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AUTHORS

1 Mr. **G.Jaswanth,** received B.Tech degree in Electrical and Electronics Engineering from Sri Kottam Tulasi Reddy Memorial College of Engineering, Kurnool,A.P.. And currently pursuing M.Tech in Electrical Power Systems at K.V.SUBBA REDDY COLLEGE OF ENGINEERING AND TECHNOLOGY, Kurnool,a.p India, My areas of interest are Power Systems, and Power Electronics, Electrical Machines.

2. **Mr.M.DILIP KUMAR M.TECH (Ph.d)**, working as Associate Professor in K.V.SUBBA REDDY COLLEGE OF ENGINEERING AND TECHNOLOGY,Kurnool,A.P,India.